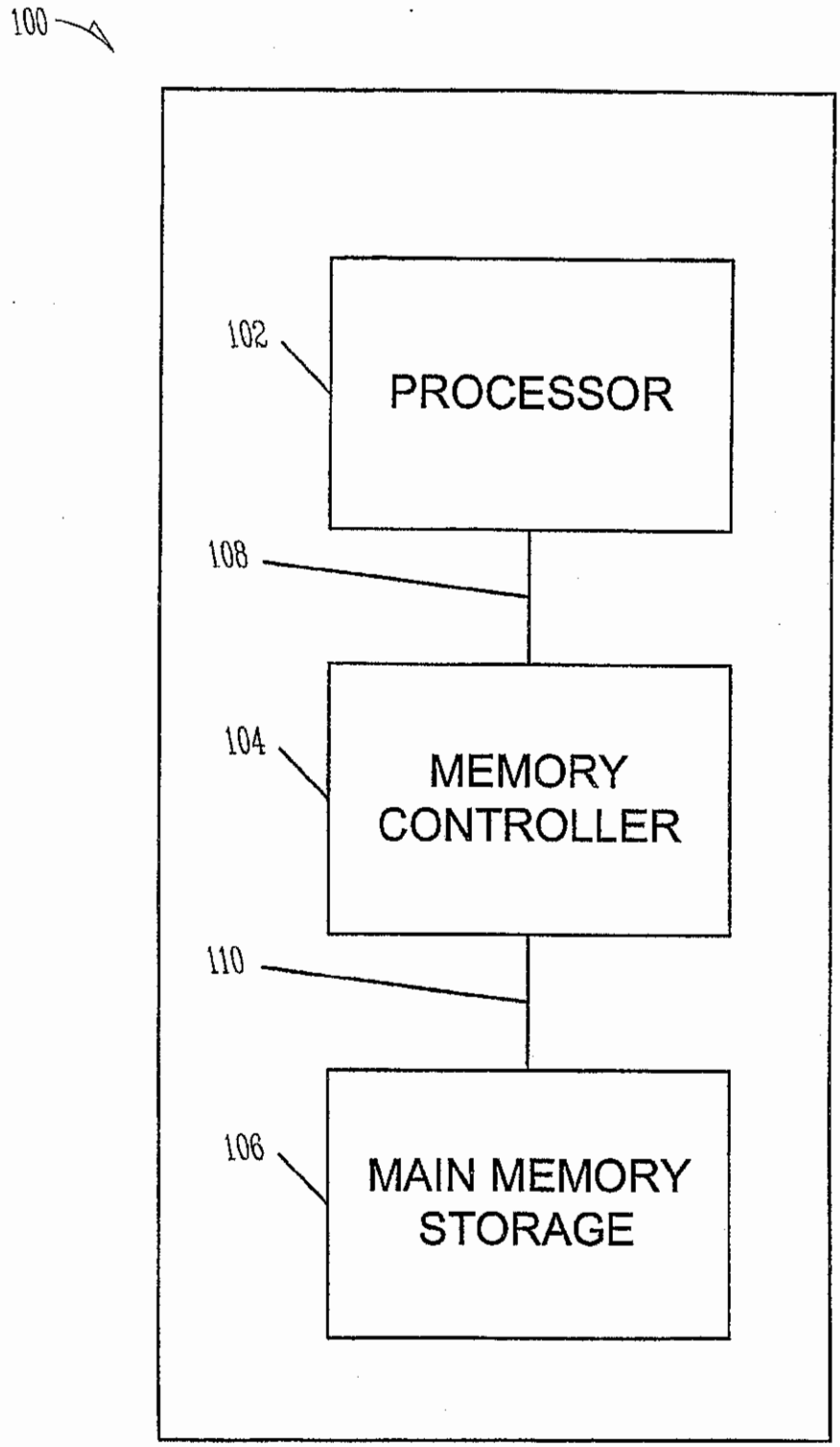


Fig. 1
(Prior Art)

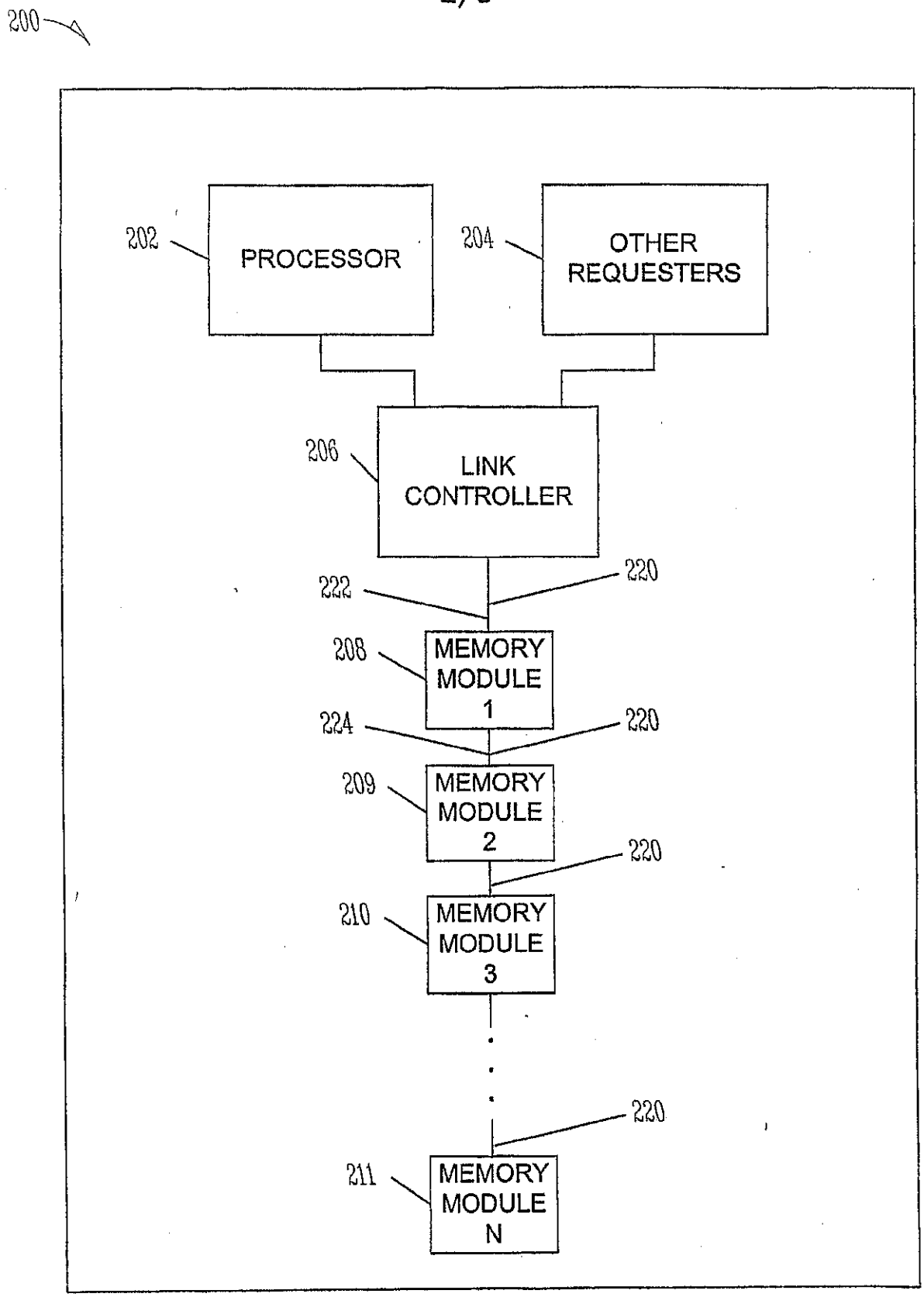

200
202
PROCESSOR
204
OTHER REQUESTERS
206
LINK CONTROLLER
222
220
208
MEMORY MODULE 1
224
220
209
MEMORY MODULE 2
220
210
MEMORY MODULE 3
220
211
MEMORY MODULE N

Fig.2

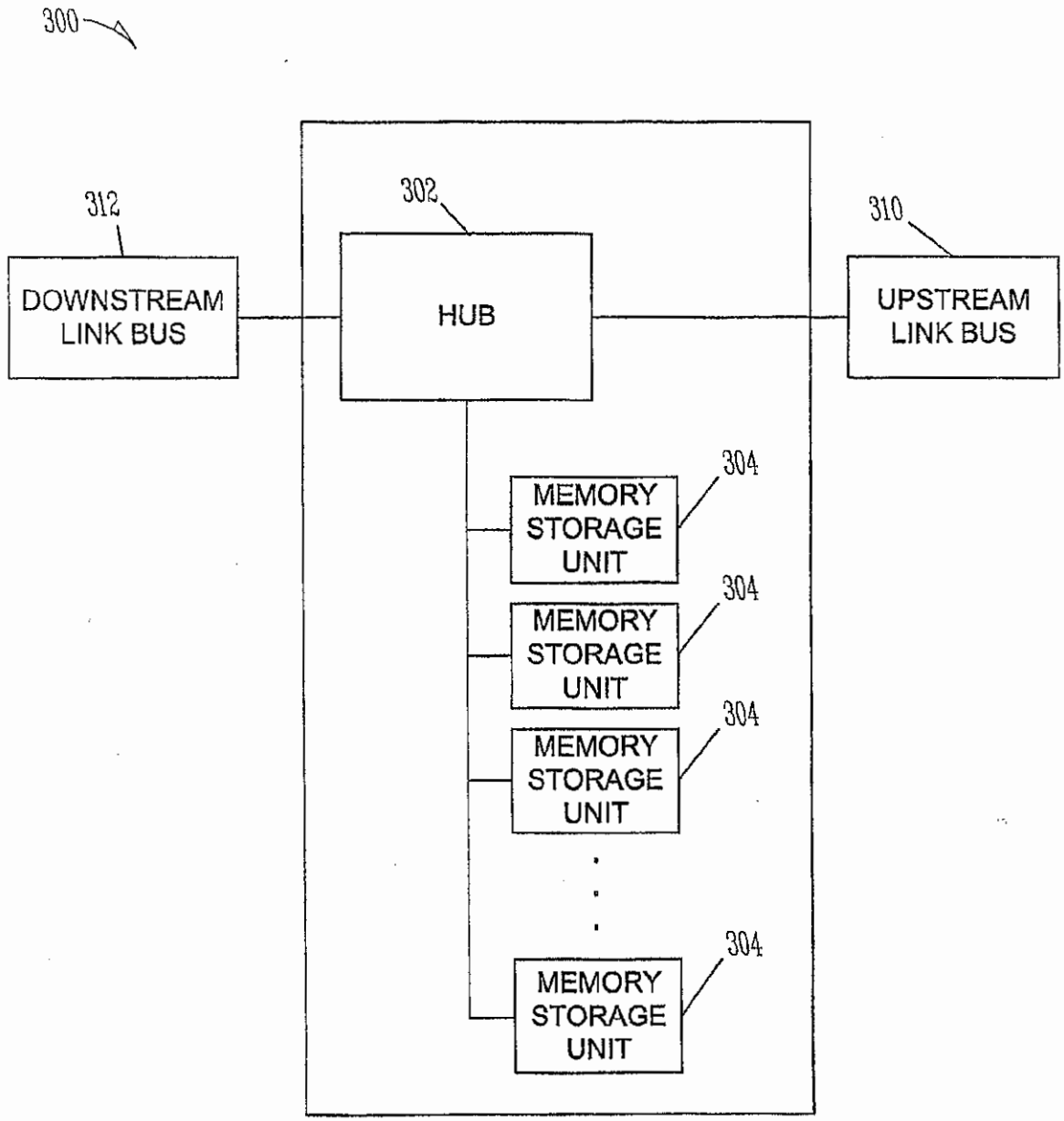

300
312
DOWNSTREAM LINK BUS
302
HUB
310
UPSTREAM LINK BUS
304
MEMORY STORAGE UNIT
304
MEMORY STORAGE UNIT
304
MEMORY STORAGE UNIT
304
MEMORY STORAGE UNIT

Fig. 3

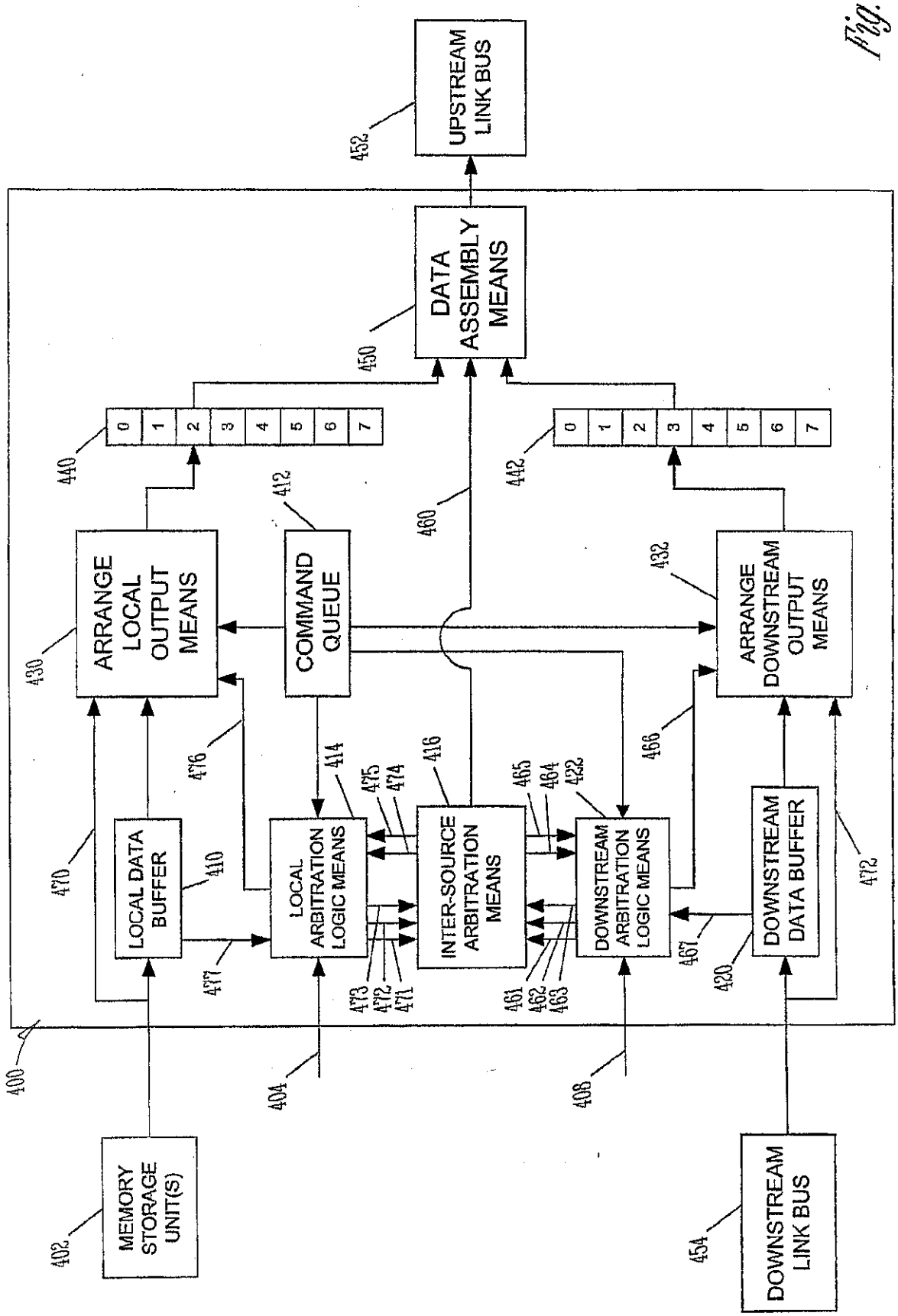

UPSTREAM LINK BUS
452
DATA ASSEMBLY MEANS
450
460
0 1 2 3 4 5 6 7
440
0 1 2 3 4 5 6 7
442
ARRANGE LOCAL OUTPUT MEANS
430
COMMAND QUEUE
412
ARRANGE DOWNSTREAM OUTPUT MEANS
432
LOCAL DATA BUFFER
410
LOCAL ARBITRATION LOGIC MEANS
414
INTER-SOURCE ARBITRATION MEANS
416
DOWNSTREAM ARBITRATION LOGIC MEANS
422
DOWNSTREAM DATA BUFFER
420
MEMORY STORAGE UNIT(S)
402
DOWNSTREAM LINK BUS
454
400
404
408
470
472
476
466
477
467
471 472 473
474 475
461 462 463
464 465

Fig. 4

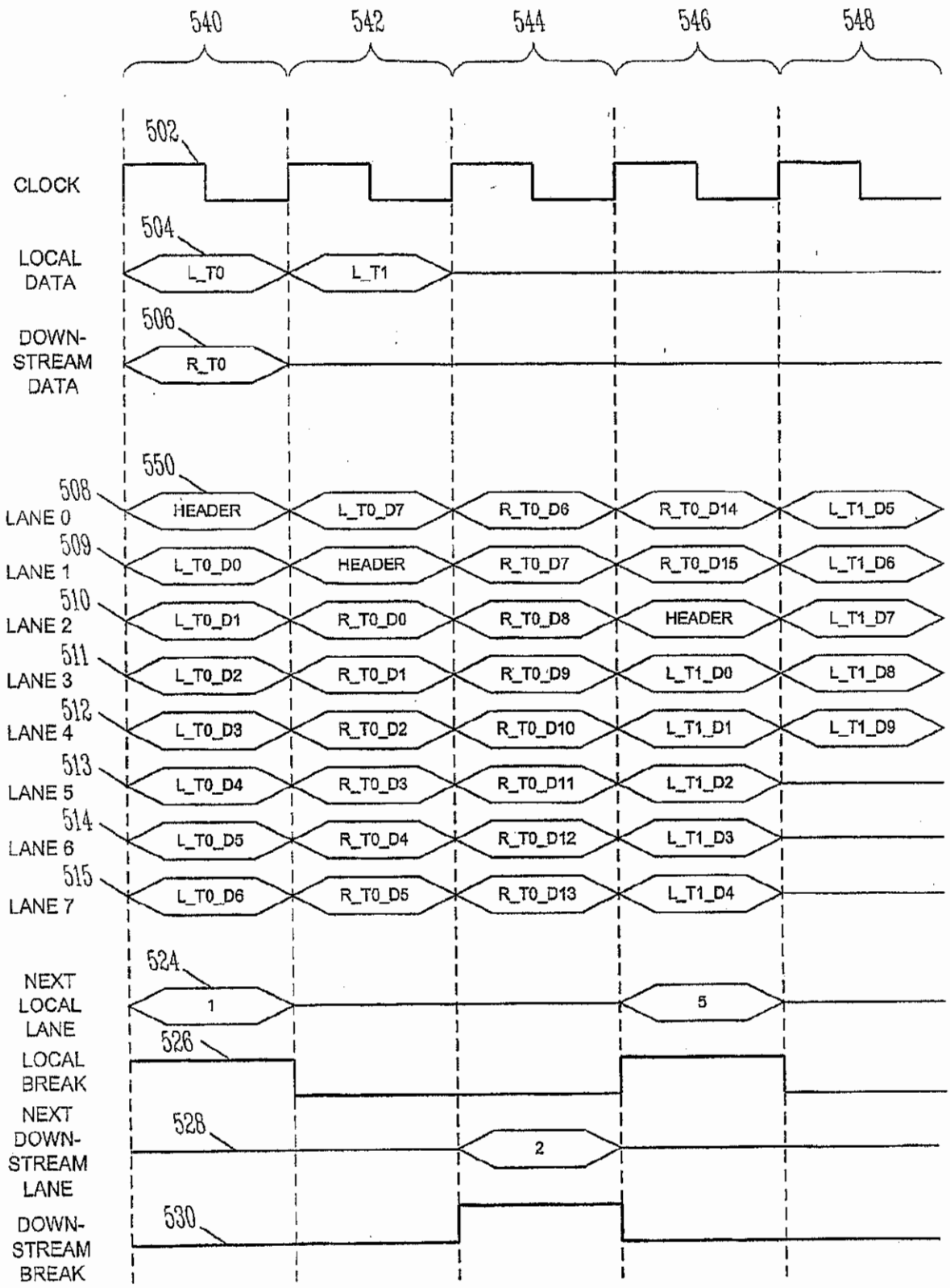

540
542
544
546
548
502
CLOCK
504
LOCAL DATA
L_T0
L_T1
506
DOWN-STREAM DATA
R_T0
550
508
LANE 0
HEADER
L_T0_D7
R_T0_D6
R_T0_D14
L_T1_D5
509
LANE 1
L_T0_D0
HEADER
R_T0_D7
R_T0_D15
L_T1_D6
510
LANE 2
L_T0_D1
R_T0_D0
R_T0_D8
HEADER
L_T1_D7
511
LANE 3
L_T0_D2
R_T0_D1
R_T0_D9
L_T1_D0
L_T1_D8
512
LANE 4
L_T0_D3
R_T0_D2
R_T0_D10
L_T1_D1
L_T1_D9
513
LANE 5
L_T0_D4
R_T0_D3
R_T0_D11
L_T1_D2
514
LANE 6
L_T0_D5
R_T0_D4
R_T0_D12
L_T1_D3
515
LANE 7
L_T0_D6
R_T0_D5
R_T0_D13
L_T1_D4
524
NEXT LOCAL LANE
1
5
526
LOCAL BREAK
528
NEXT DOWN-STREAM LANE
2
530
DOWN-STREAM BREAK

Fig.5

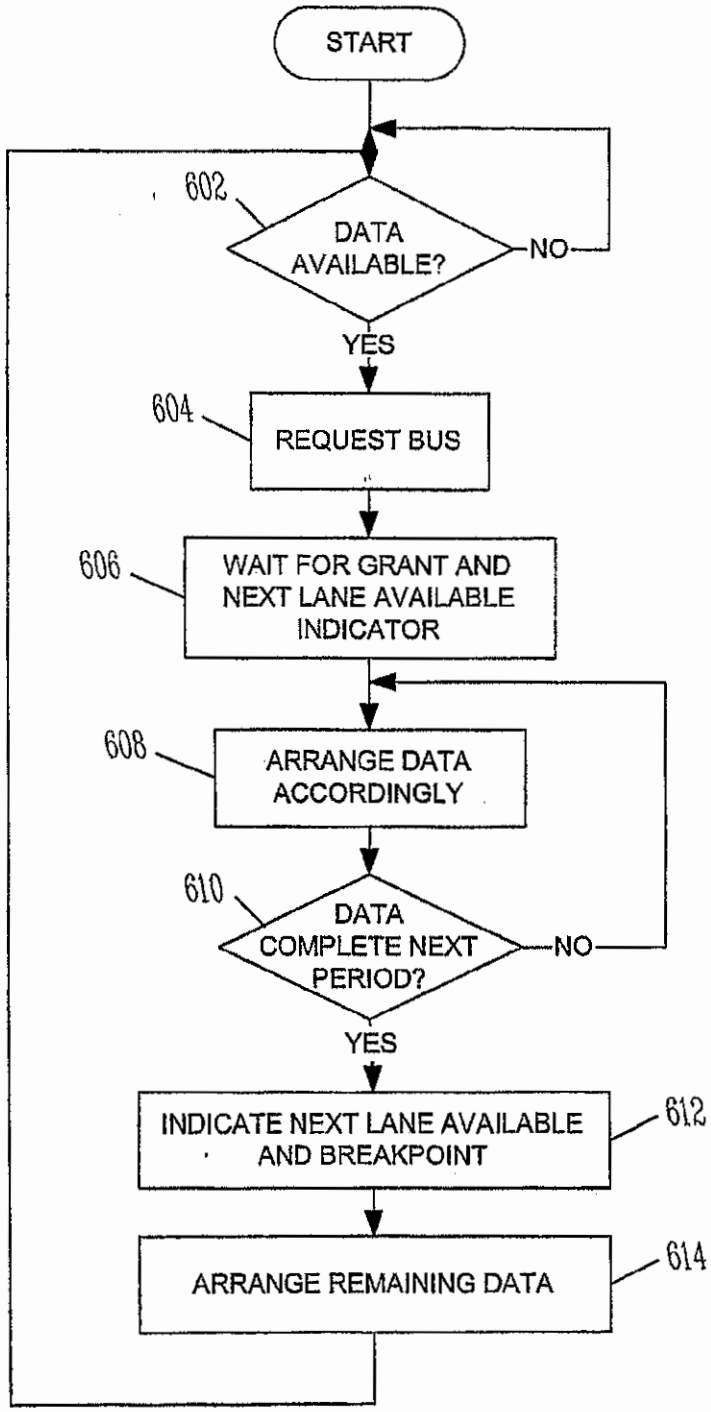

START
602
DATA AVAILABLE?
NO
YES
604
REQUEST BUS
606
WAIT FOR GRANT AND NEXT LANE AVAILABLE INDICATOR
608
ARRANGE DATA ACCORDINGLY
610
DATA COMPLETE NEXT PERIOD?
NO
YES
INDICATE NEXT LANE AVAILABLE AND BREAKPOINT
612
ARRANGE REMAINING DATA
614

Fig. 6

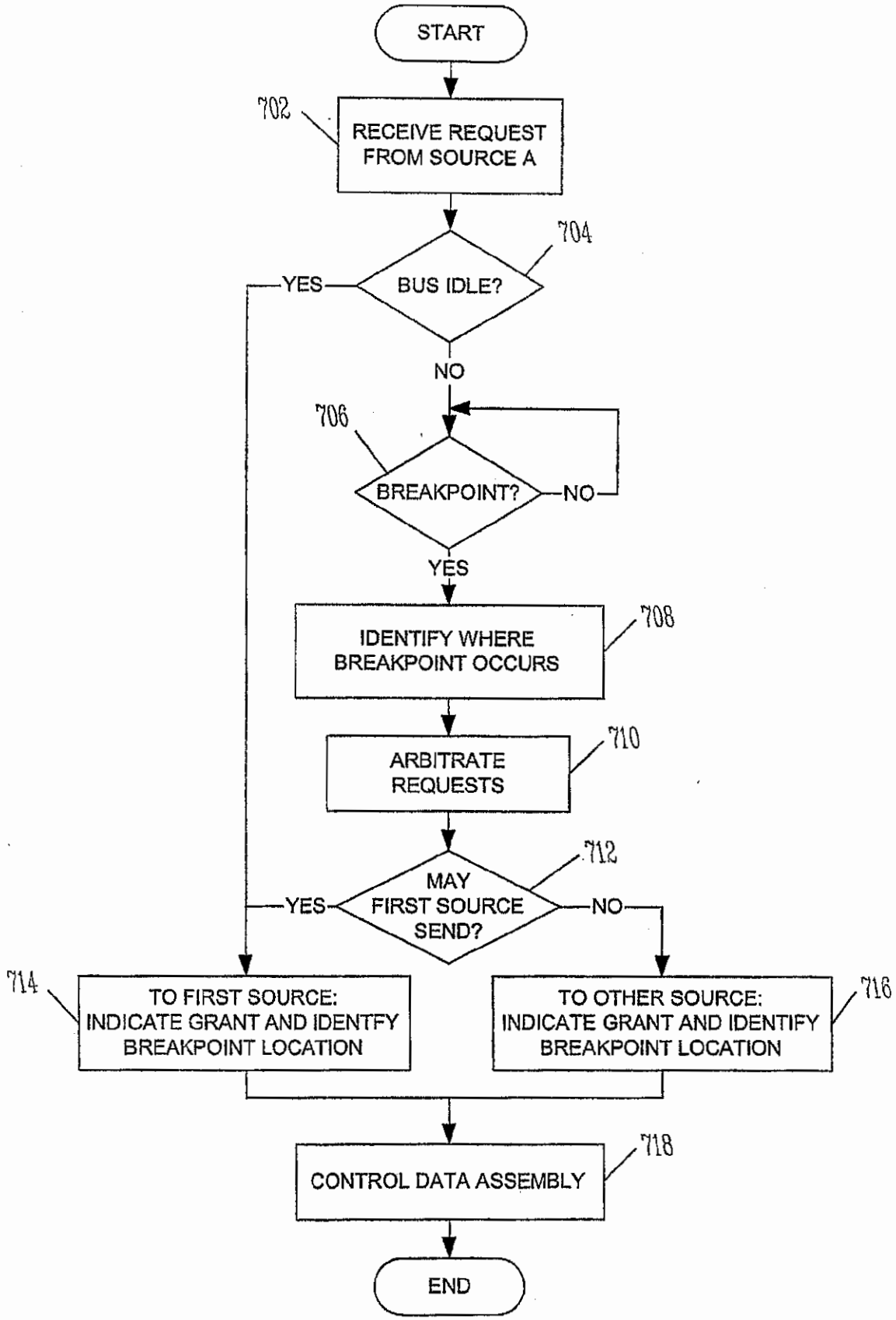

START
702
RECEIVE REQUEST FROM SOURCE A
704
BUS IDLE?
YES
NO
706
BREAKPOINT?
NO
YES
708
IDENTIFY WHERE BREAKPOINT OCCURS
710
ARBITRATE REQUESTS
712
MAY FIRST SOURCE SEND?
YES
NO
714
TO FIRST SOURCE: INDICATE GRANT AND IDENTFY BREAKPOINT LOCATION
716
TO OTHER SOURCE: INDICATE GRANT AND IDENTIFY BREAKPOINT LOCATION
718
CONTROL DATA ASSEMBLY
END

Fig. 7

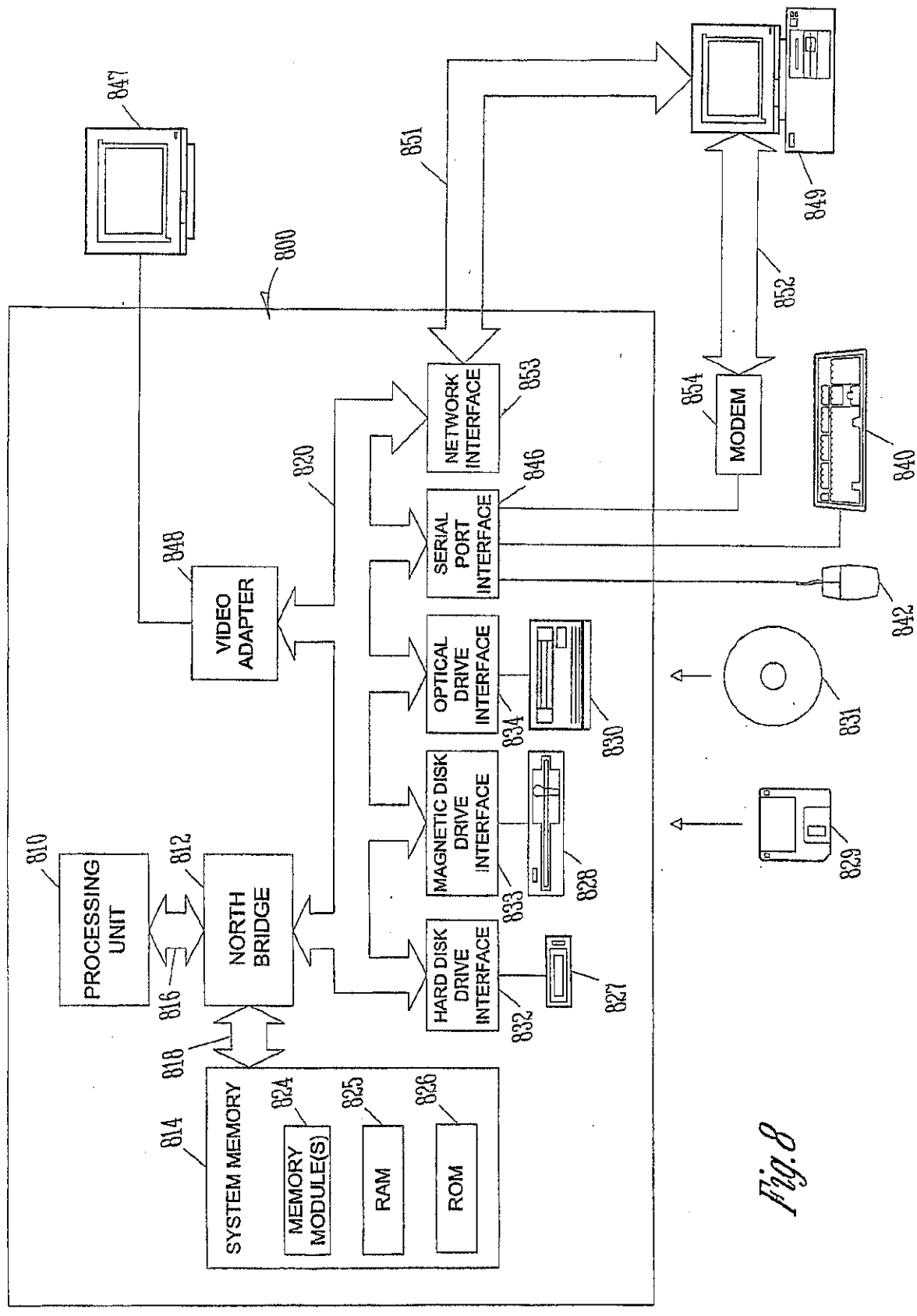

847
851
849
800
852
854
MODEM
840
NETWORK INTERFACE
853
820
846
SERIAL PORT INTERFACE
842
848
VIDEO ADAPTER
OPTICAL DRIVE INTERFACE
834
830
831
MAGNETIC DISK DRIVE INTERFACE
833
828
829
HARD DISK DRIVE INTERFACE
832
827
810
PROCESSING UNIT
812
NORTH BRIDGE
816
818
814
SYSTEM MEMORY
824
MEMORY MODULE(S)
825
RAM
826
ROM

Fig. 8