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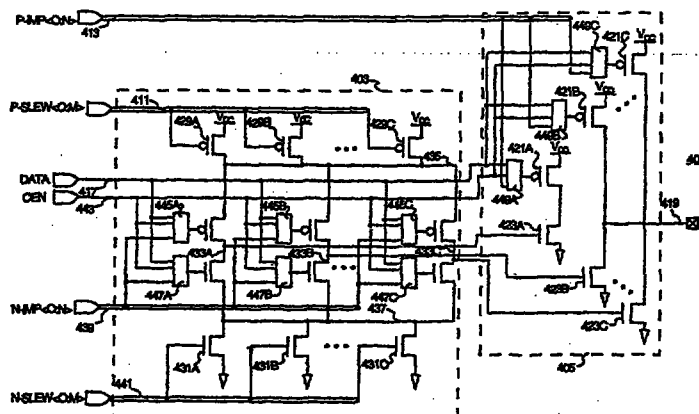
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(54) Title: METHOD AND APPARATUS FOR SLEW RATE AND IMPEDANCE COMPENSATING BUFFER CIRCUITS



(57) Abstract

A method and an apparatus for adjusting the slew rate and impedance of a buffer in an integrated circuitry. In one embodiment, an integrated circuit buffer includes a pre-driver circuit (403), which includes a slew rate compensation circuit, coupled to a driver circuit (405), which includes an impedance compensation circuit. The slew rate compensation circuit includes parallel connected p-channel transistors (429a...429c) to power and parallel connected n-channel transistors (431a...431c) to ground to provide a variable resistance to virtual rails for inverter circuits (443a...443c) that are included in the pre-driver circuit. The slew rate compensation circuit is digitally controlled with slew rate control signals (N-SLEW). The impedance compensation circuit includes parallel connected p-channel transistors (421a...421c) to power and parallel connected n-channel transistors (423a...423c) to ground from an output node (419) of the buffer. The parallel connected transistors of the impedance compensation circuit are digitally controlled with impedance control signals. The resistance to power and ground from the respective rails of the pre-driver circuit are controlled with the slew rate control signals to adjust the slew rate of data signals being driven by the buffer. The rails are shared among the inverters of the driver circuit to reduce the number of devices used by the buffer, thereby reducing the amount of circuit area and power used by the buffer.