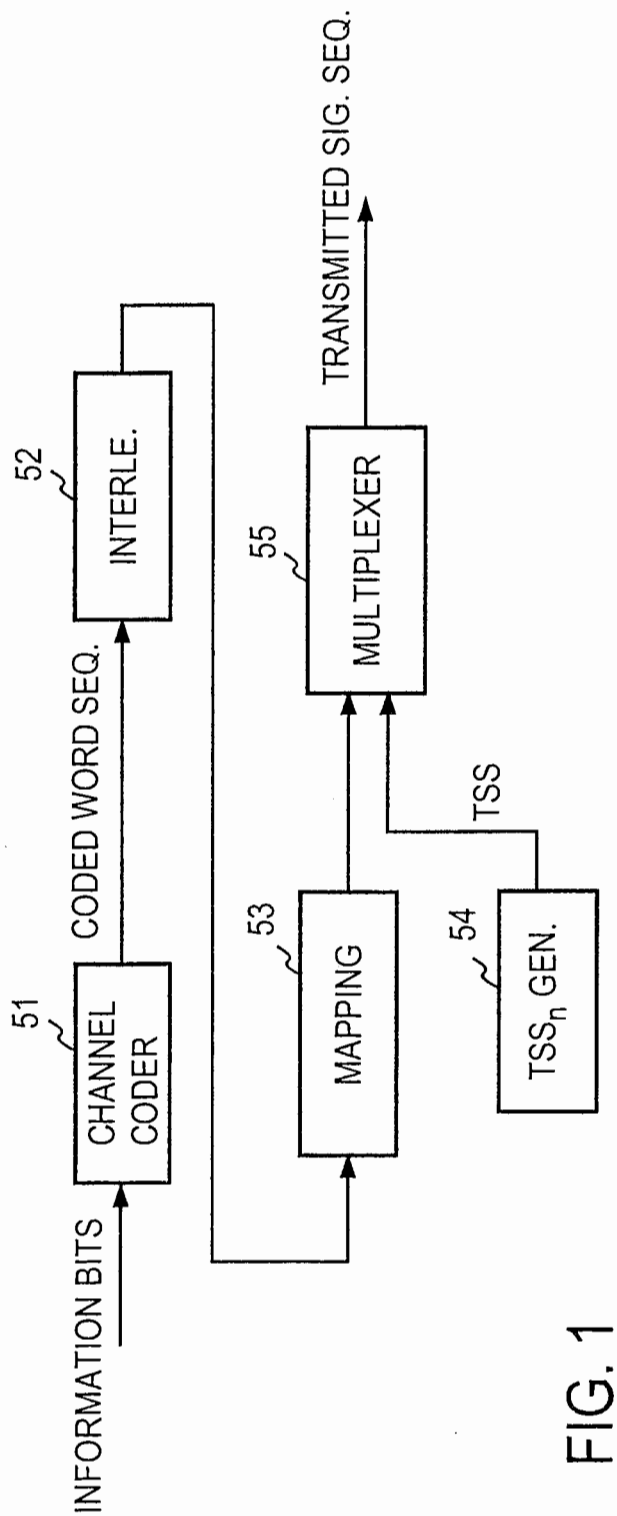

INFORMATION BITS
51
CHANNEL CODER
CODED WORD SEQ.
52
INTERLE.
53
MAPPING
54
TSS$_n$ GEN.
TSS
55
MULTIPLEXER
TRANSMITTED SIG. SEQ.

FIG. 1

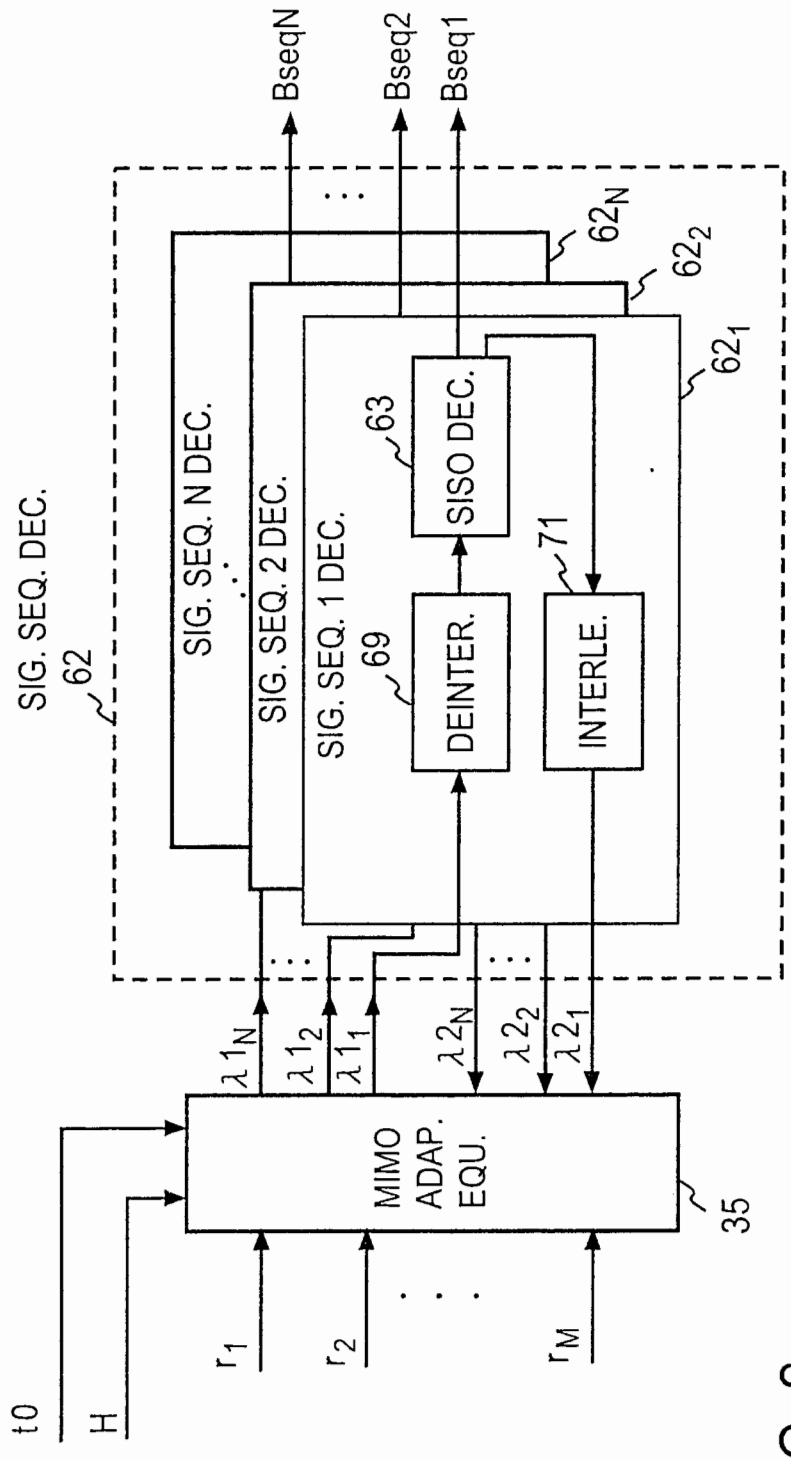
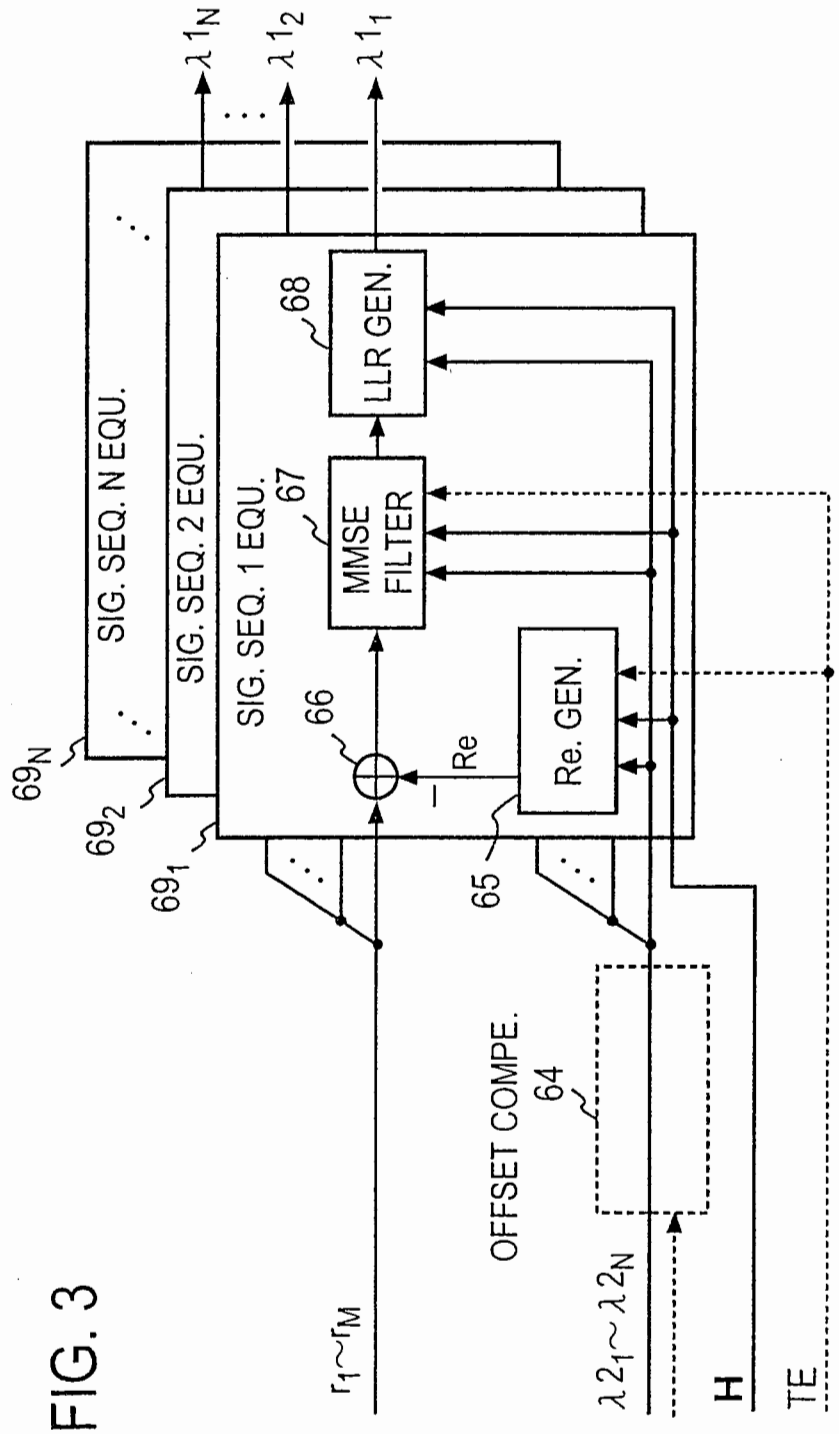

BseqN
Bseq2
Bseq1
SIG. SEQ. DEC.
62
SIG. SEQ. N DEC.
SIG. SEQ. 2 DEC.
SIG. SEQ. 1 DEC.
62N
62 2
62 1
63
SISO DEC.
69
DEINTER.
71
INTERLE.
λ1N
λ12
λ11
λ2N
λ22
λ21
MIMO
ADAP.
EQU.
35
r1
r2
rM
t0
H

FIG. 2

FIG. 3


λ1N
λ12
λ11
SIG. SEQ. N EQU.
SIG. SEQ. 2 EQU.
SIG. SEQ. 1 EQU.
69N
692
691
68
LLR GEN.
67
MMSE FILTER
66
Re
65
Re. GEN.
OFFSET COMPE.
64
r1~rM
λ21~λ2N
H
TE

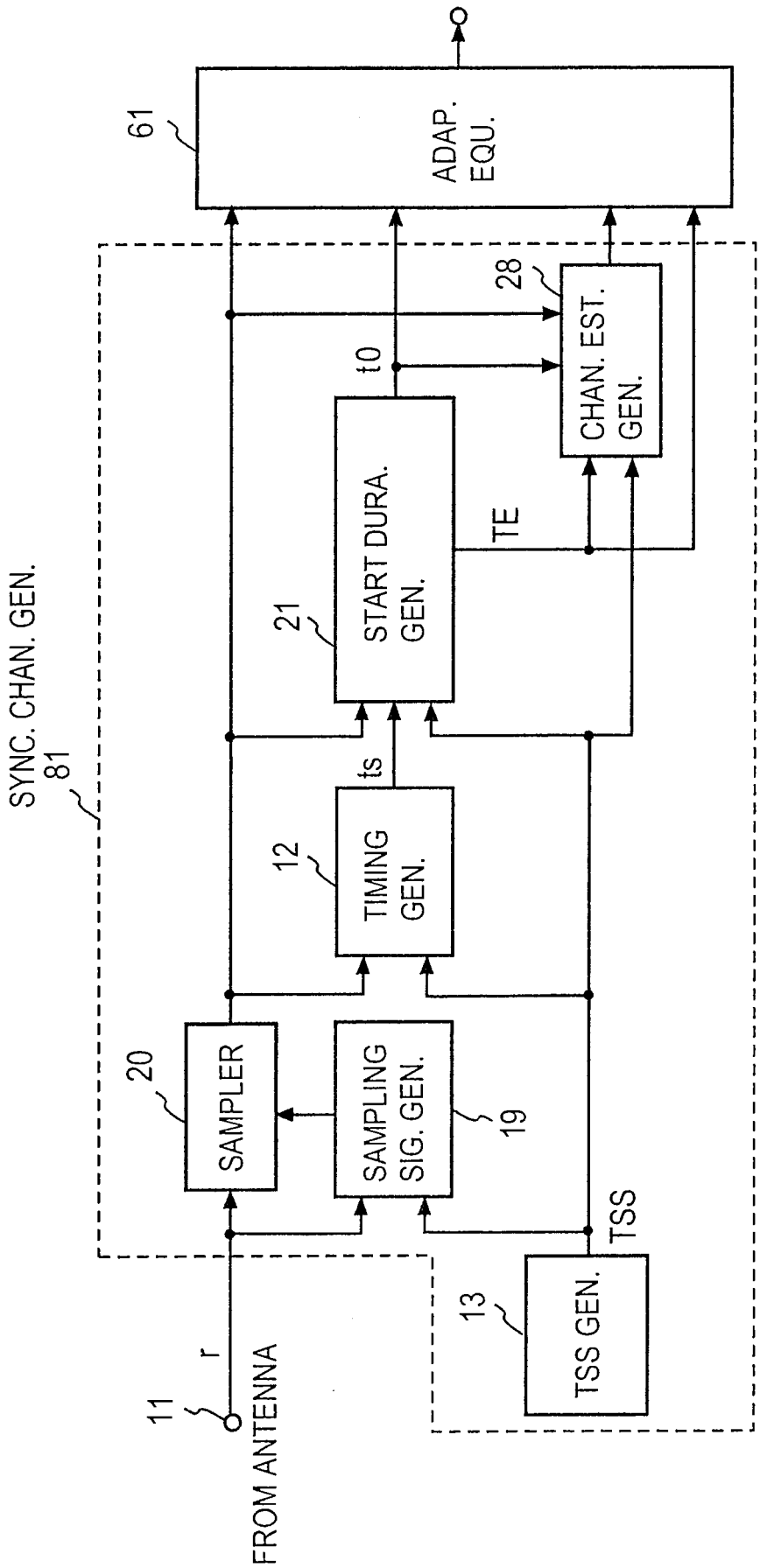

61
ADAP. EQU.
28
CHAN. EST. GEN.
t0
21
START DURA. GEN.
TE
SYNC. CHAN. GEN.
81
12
TIMING GEN.
ts
20
SAMPLER
SAMPLING SIG. GEN.
19
13
TSS GEN.
TSS
11
r
FROM ANTENNA

FIG. 4

FIG. 5A

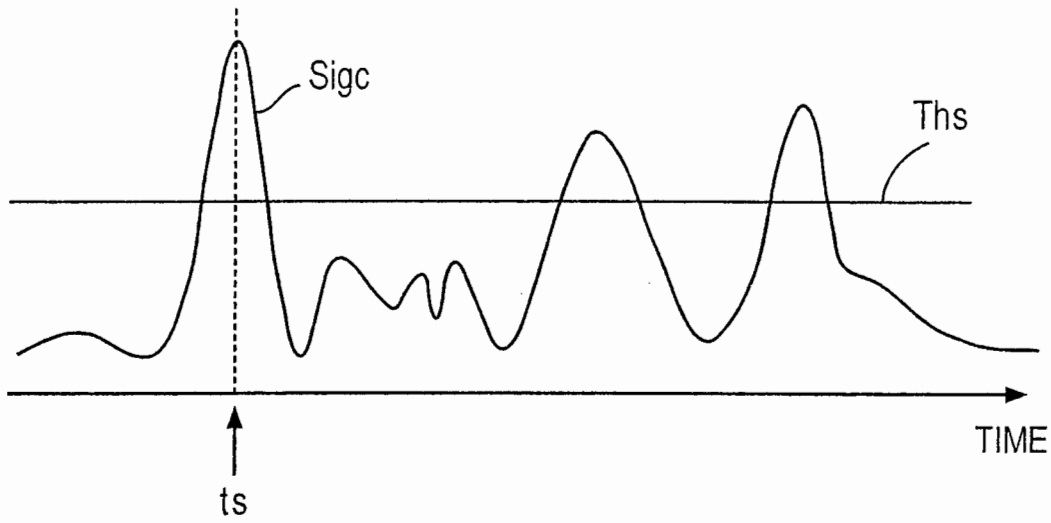
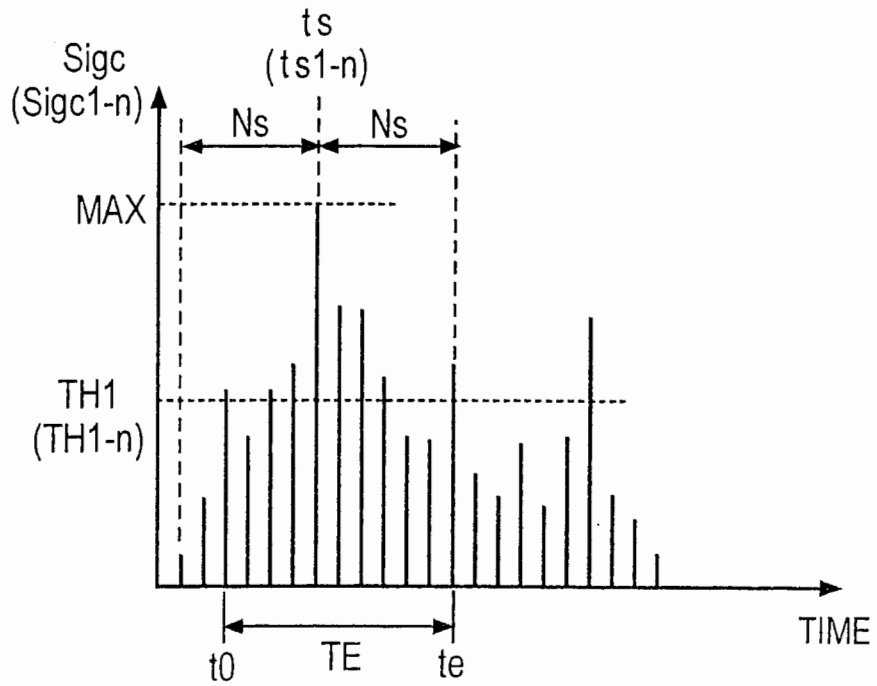

Sigc
Ths
TIME
ts

FIG. 5B


ts
(ts1-n)
Sigc
(Sigc1-n)
Ns
Ns
MAX
TH1
(TH1-n)
TIME
t0
TE
te

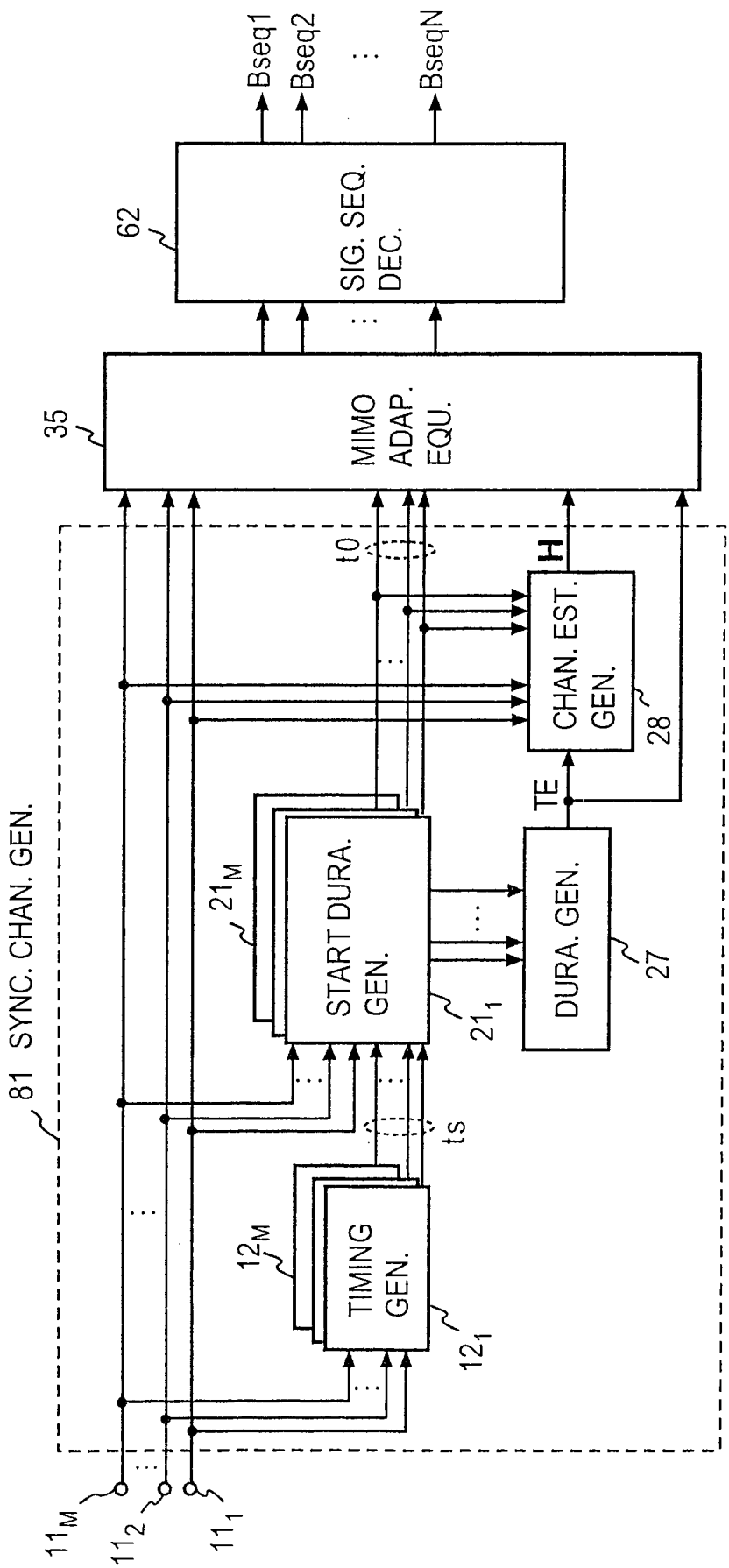

Bseq1
Bseq2
BseqN
62
SIG. SEQ. DEC.
35
MIMO ADAP. EQU.
81 SYNC. CHAN. GEN.
t0
H
CHAN. EST. GEN.
28
TE
DURA. GEN.
27
21_M
START DURA. GEN.
21_1
ts
12_M
TIMING GEN.
12_1
11_M
11_2
11_1

FIG. 6

FIG. 7

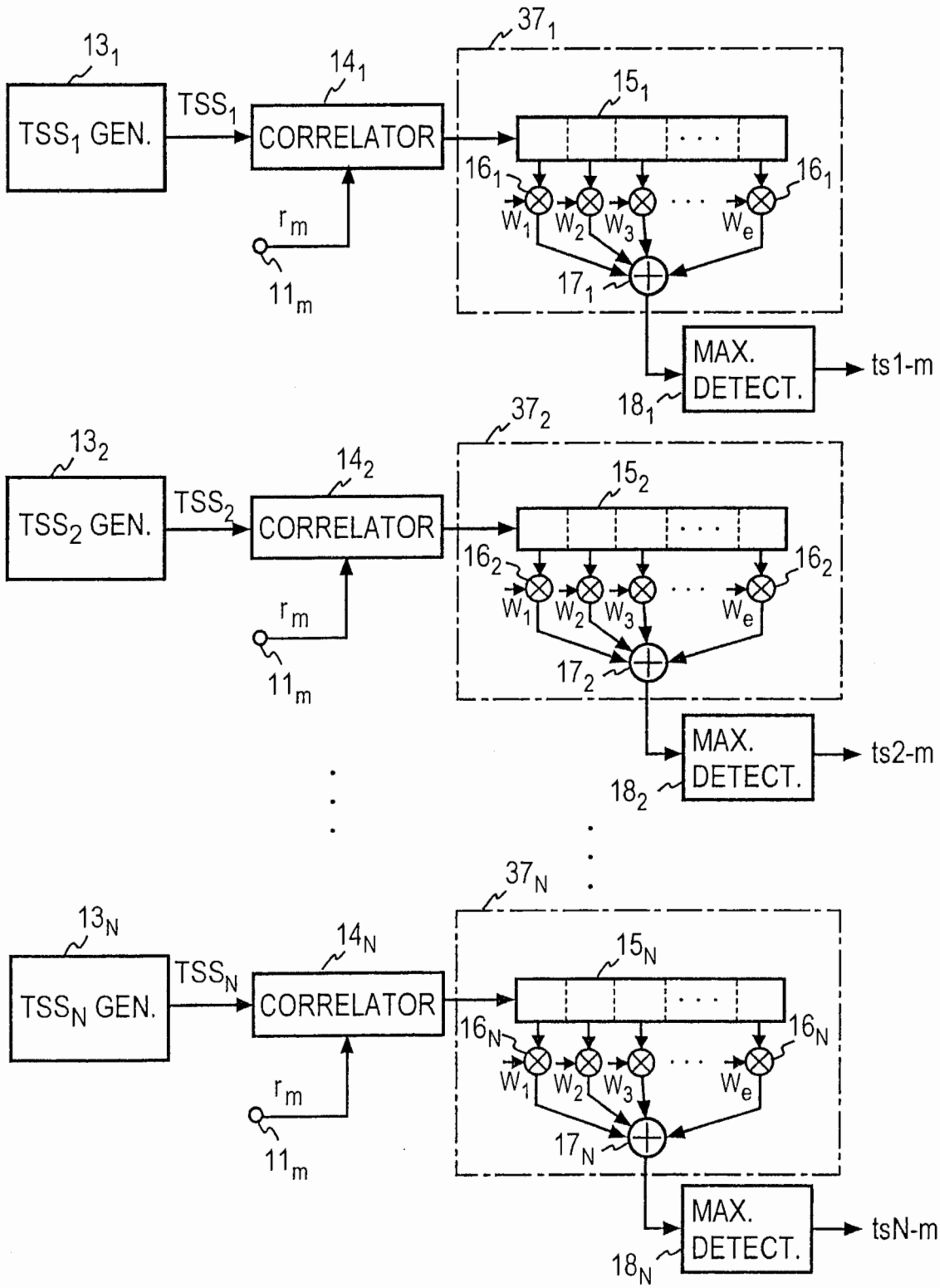

13_1
TSS_1 GEN.
TSS_1
14_1
CORRELATOR
r_m
11_m
37_1
15_1
16_1
W_1 W_2 W_3 W_e
17_1
18_1
MAX. DETECT.
ts1-m
13_2
TSS_2 GEN.
TSS_2
14_2
CORRELATOR
r_m
11_m
37_2
15_2
16_2
W_1 W_2 W_3 W_e
17_2
18_2
MAX. DETECT.
ts2-m
13_N
TSS_N GEN.
TSS_N
14_N
CORRELATOR
r_m
11_m
37_N
15_N
16_N
W_1 W_2 W_3 W_e
17_N
18_N
MAX. DETECT.
tsN-m

FIG. 8

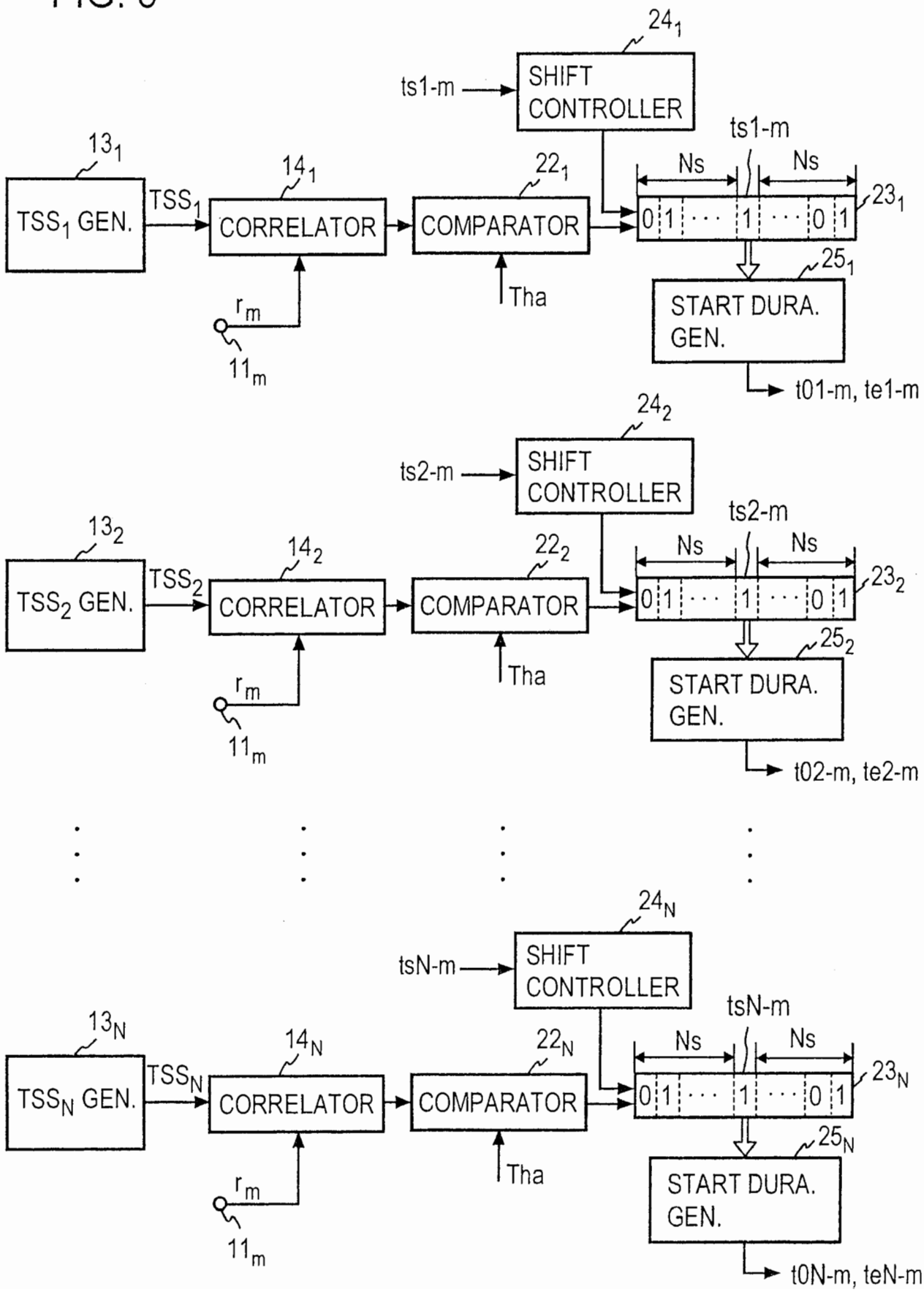
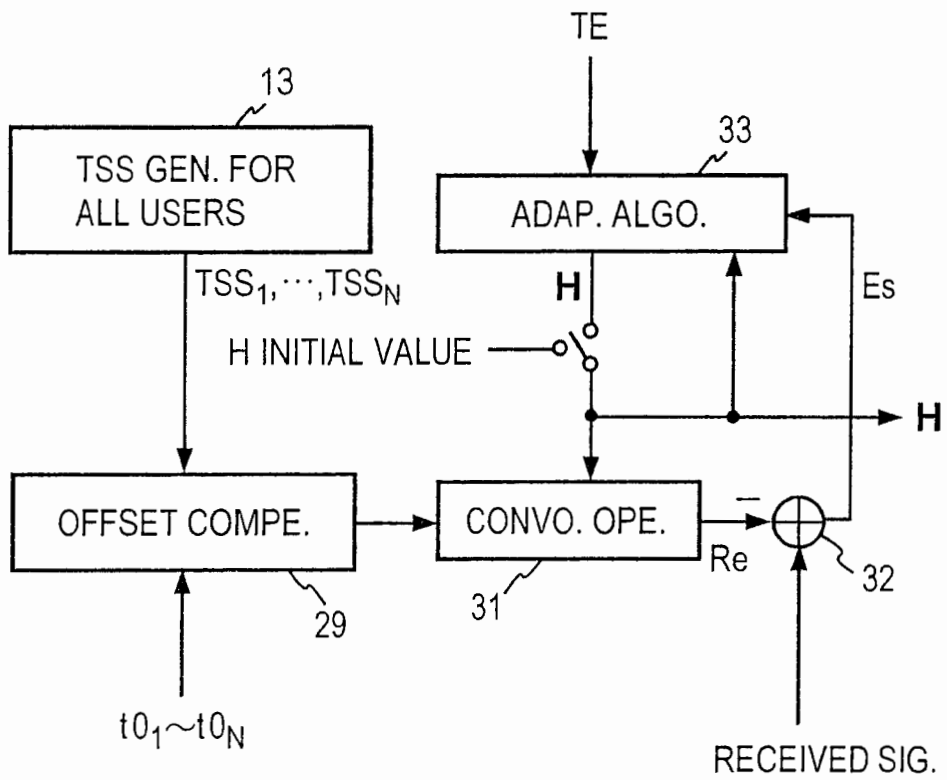

24_1
ts1-m
SHIFT CONTROLLER
ts1-m
13_1
14_1
22_1
Ns
Ns
23_1
TSS_1 GEN.
TSS_1
CORRELATOR
COMPARATOR
0 1 · · · 1 · · · 0 1
25_1
r_m
Tha
START DURA. GEN.
11_m
t01-m, te1-m
24_2
ts2-m
SHIFT CONTROLLER
ts2-m
13_2
14_2
22_2
Ns
Ns
23_2
TSS_2 GEN.
TSS_2
CORRELATOR
COMPARATOR
0 1 · · · 1 · · · 0 1
25_2
r_m
Tha
START DURA. GEN.
11_m
t02-m, te2-m
24_N
tsN-m
SHIFT CONTROLLER
tsN-m
13_N
14_N
22_N
Ns
Ns
23_N
TSS_N GEN.
TSS_N
CORRELATOR
COMPARATOR
0 1 · · · 1 · · · 0 1
25_N
r_m
Tha
START DURA. GEN.
11_m
t0N-m, teN-m

FIG. 9


TE
13
33
TSS GEN. FOR ALL USERS
ADAP. ALGO.
$TSS_1, \cdots, TSS_N$
H
Es
H INITIAL VALUE
H
OFFSET COMPE.
CONVO. OPE.
Re
32
29
31
$t0_1 \sim t0_N$
RECEIVED SIG.

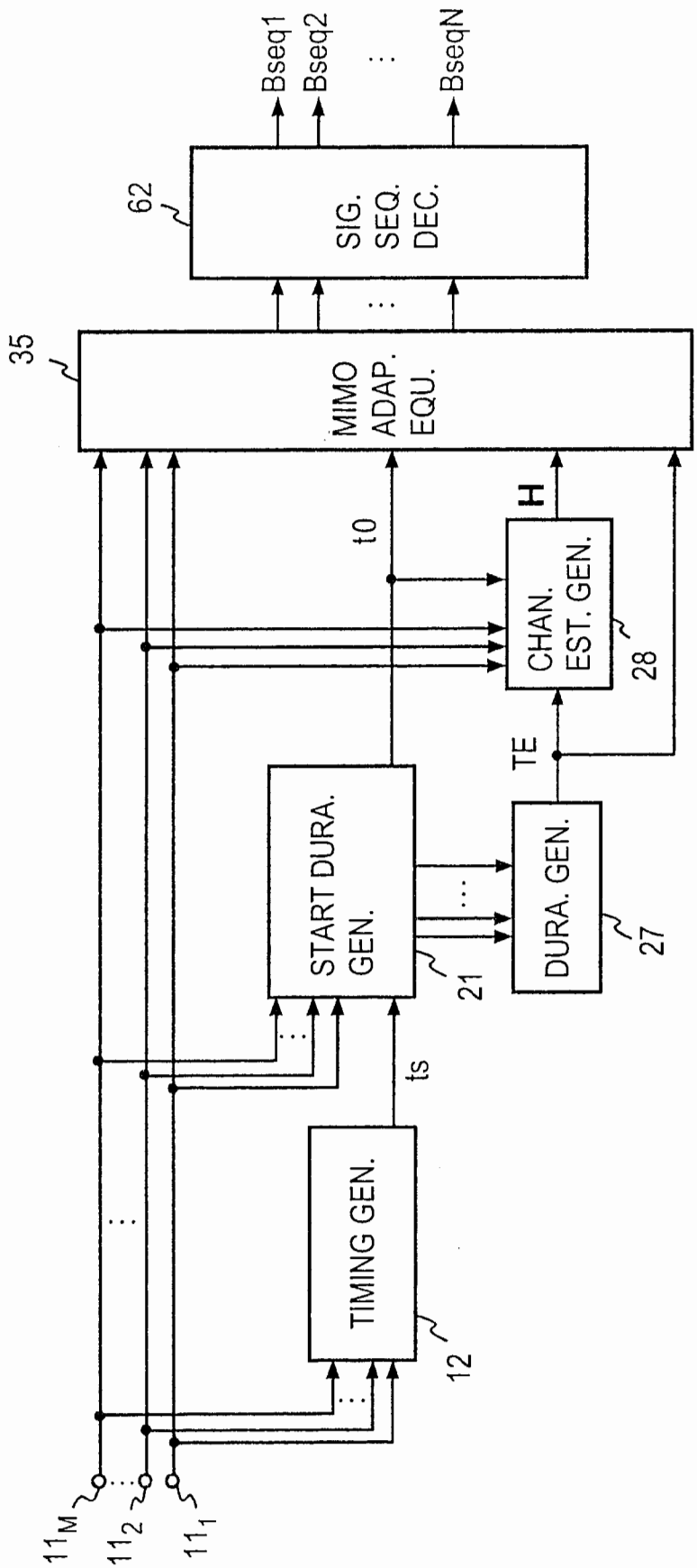

Bseq1
Bseq2
BseqN
62
SIG. SEQ. DEC.
35
MIMO ADAP. EQU.
t0
H
CHAN. EST. GEN.
28
TE
START DURA. GEN.
DURA. GEN.
21
27
ts
TIMING GEN.
12
11M
112
111

FIG. 10

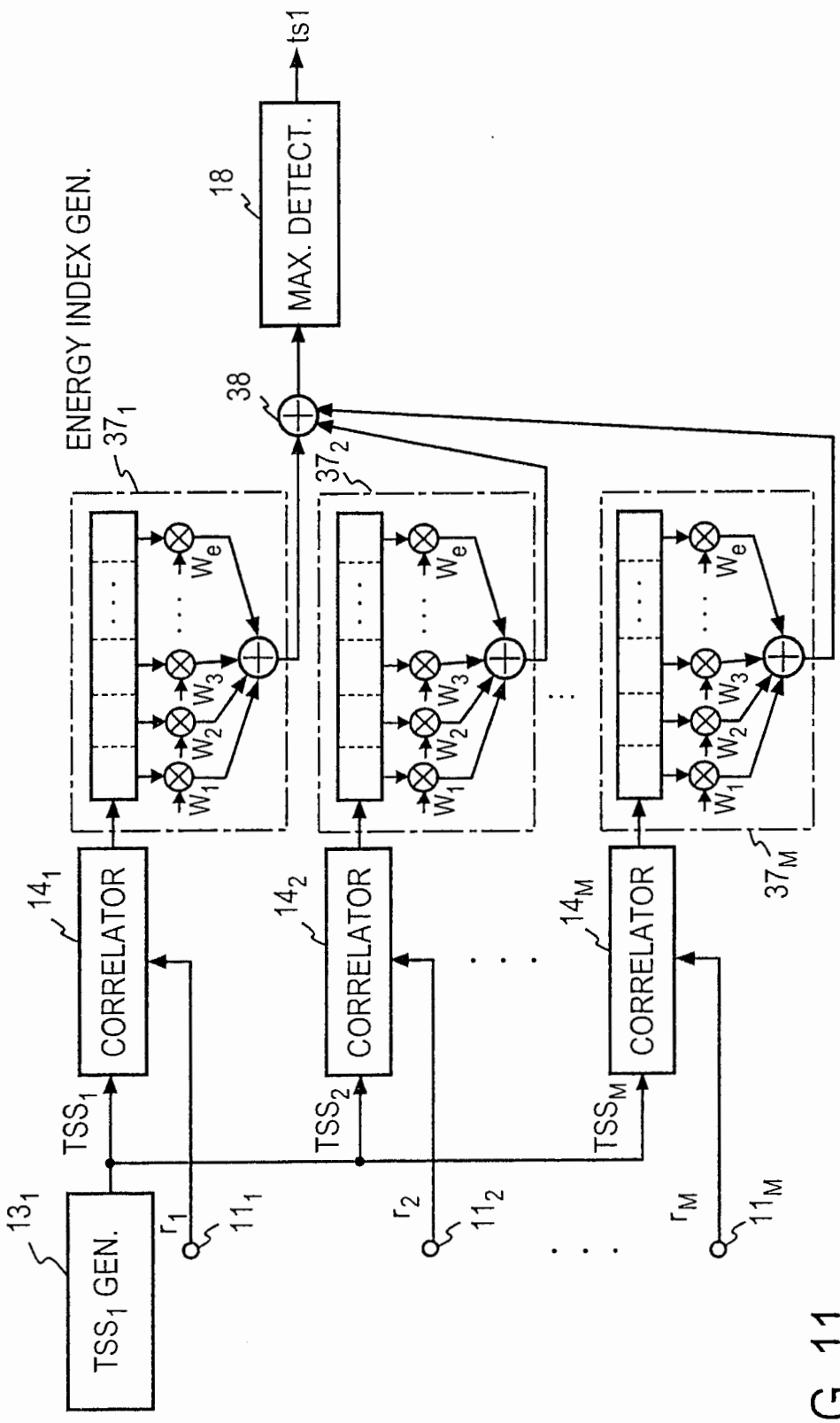

ts1
MAX. DETECT.
18
38
ENERGY INDEX GEN.
37_1
37_2
37_M
W_e
W_3
W_2
W_1
14_1
14_2
14_M
CORRELATOR
TSS_1
TSS_2
TSS_M
13_1
TSS_1 GEN.
r_1
r_2
r_M
11_1
11_2
11_M

FIG. 11

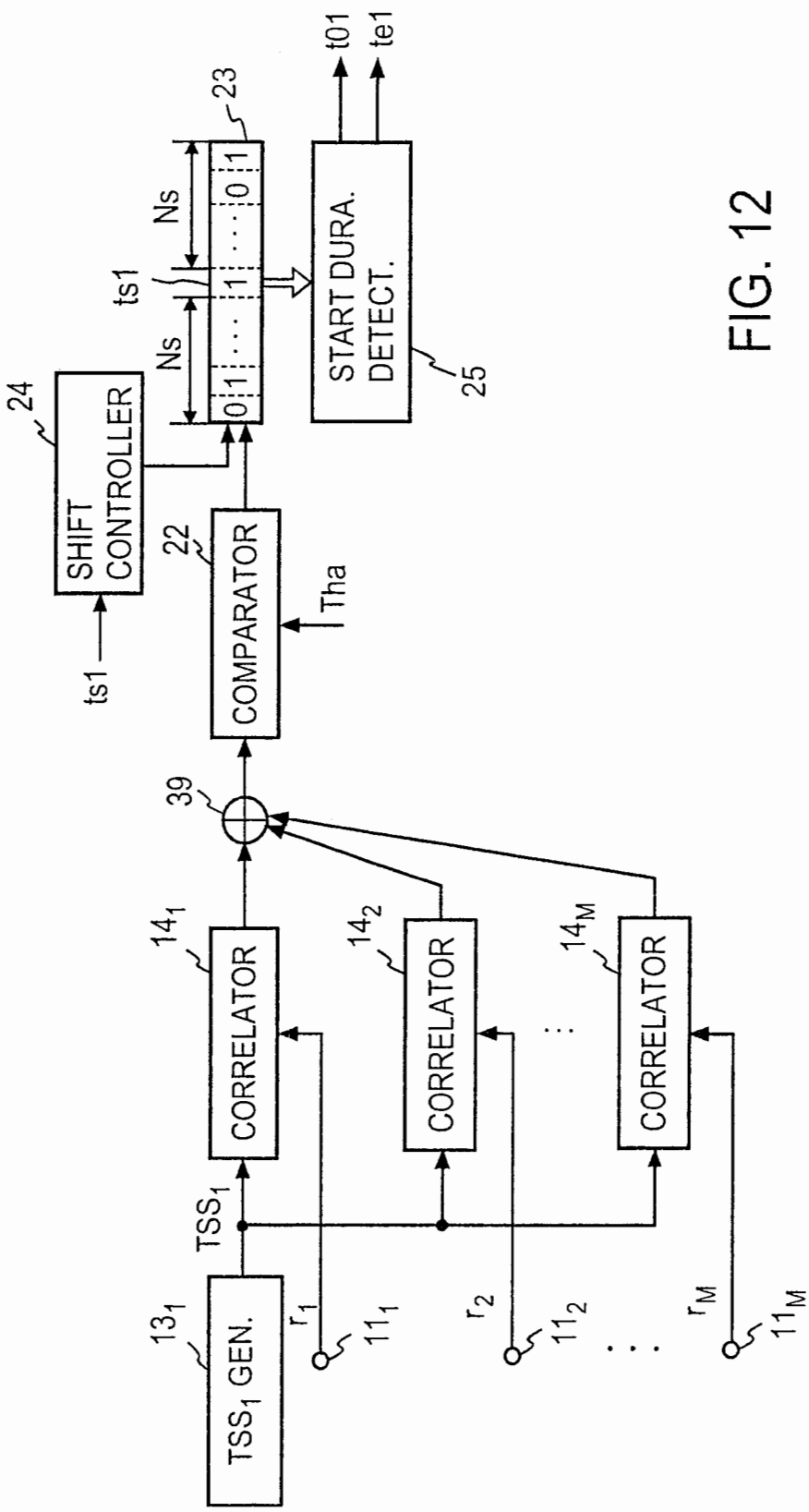

13_1
TSS_1 GEN.
TSS_1
14_1
CORRELATOR
14_2
CORRELATOR
14_M
CORRELATOR
r_1
11_1
r_2
11_2
r_M
11_M
39
22
COMPARATOR
Tha
ts1
24
SHIFT CONTROLLER
ts1
Ns
Ns
23
0 1 ... 1 0 1
START DURA. DETECT.
25
t01
te1

FIG. 12

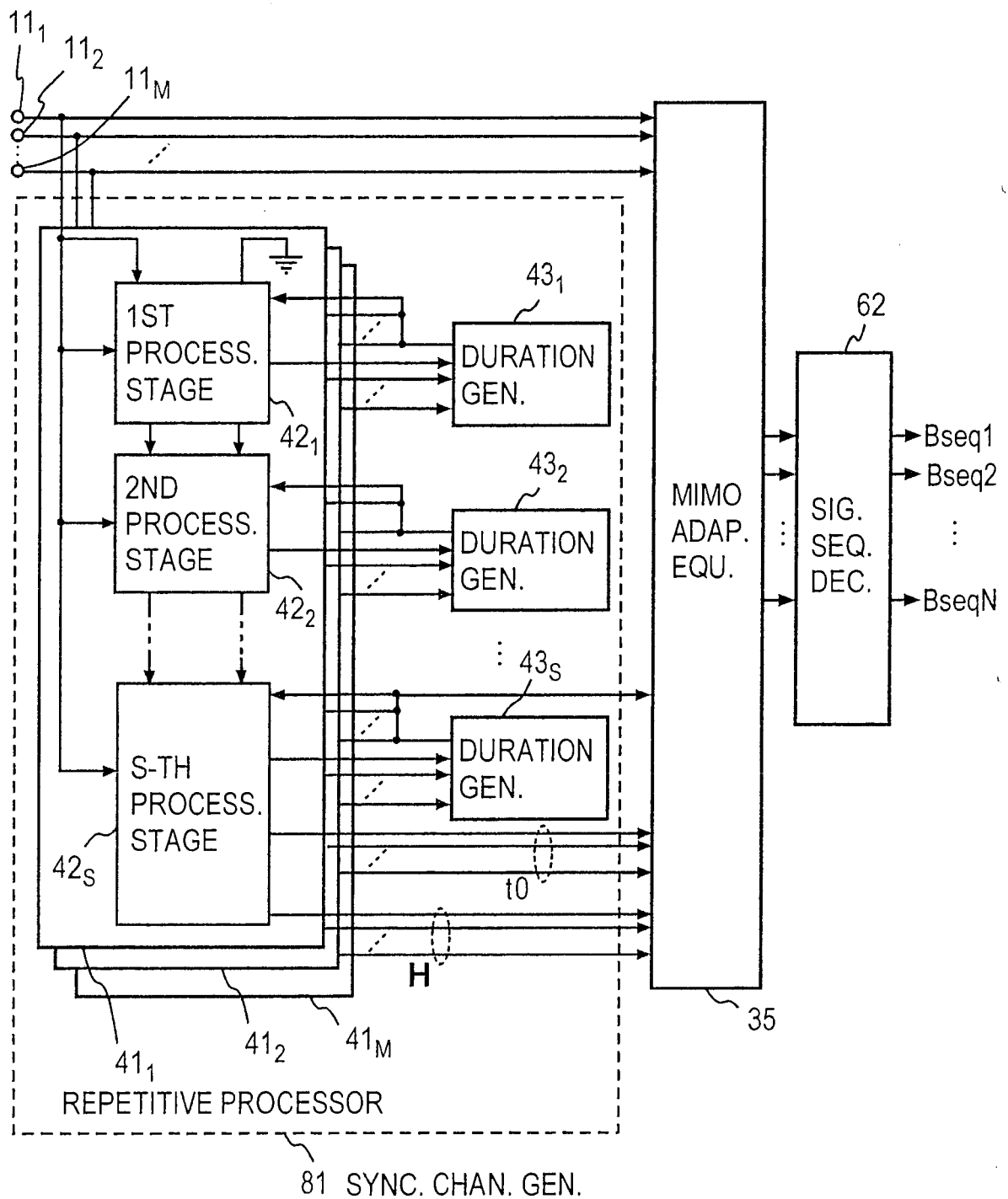

11_1
11_2
11_M
1ST PROCESS. STAGE
2ND PROCESS. STAGE
S-TH PROCESS. STAGE
42_1
42_2
42_S
43_1
43_2
43_S
DURATION GEN.
DURATION GEN.
DURATION GEN.
MIMO ADAP. EQU.
35
62
SIG. SEQ. DEC.
Bseq1
Bseq2
BseqN
t0
H
41_1
41_2
41_M
REPETITIVE PROCESSOR
81 SYNC. CHAN. GEN.

FIG. 13

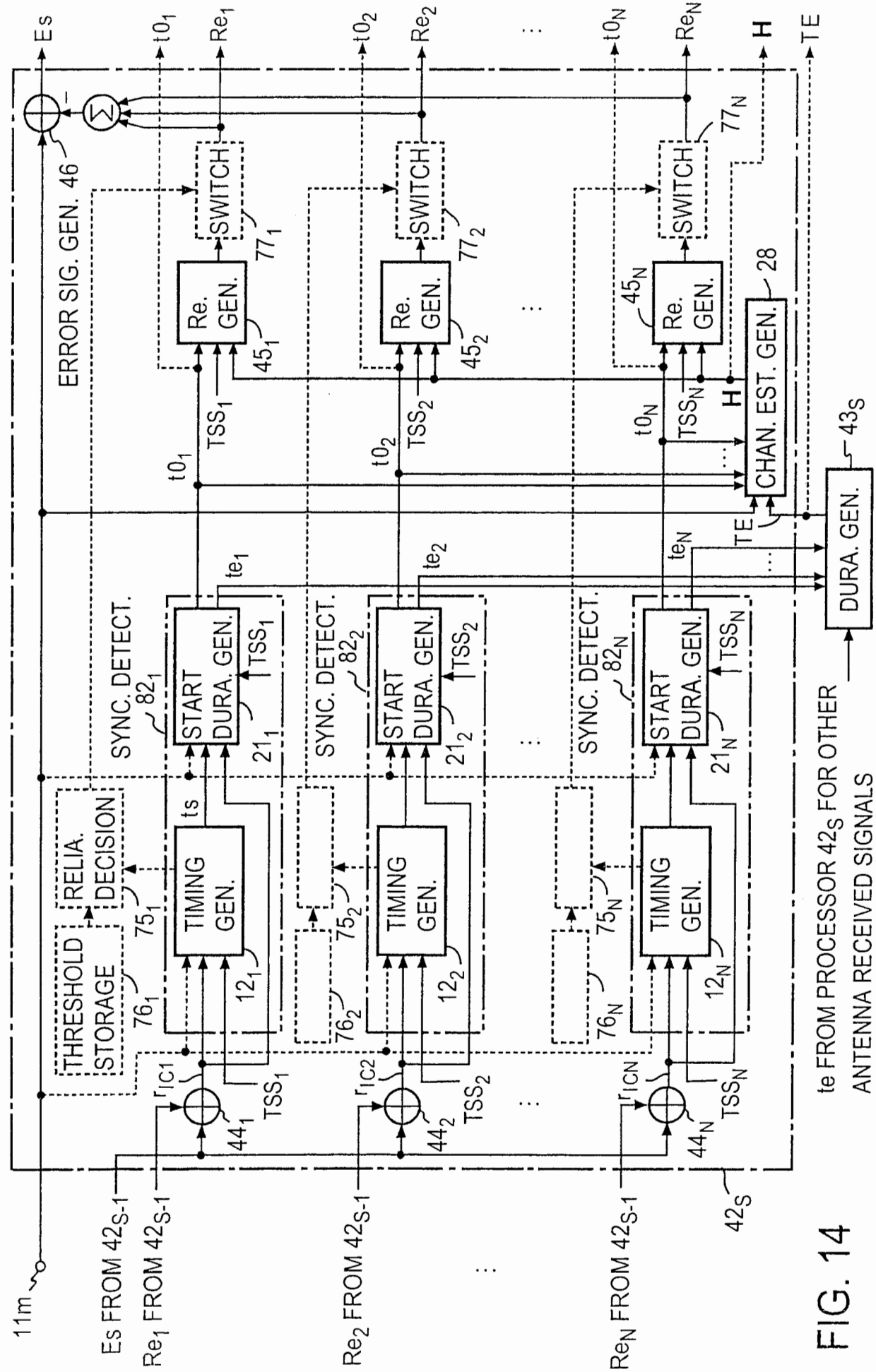

Es
$t0_1$
Re_1
$t0_2$
Re_2
$t0_N$
Re_N
H
TE
ERROR SIG. GEN. 46
SWITCH 77_1
SWITCH 77_2
SWITCH 77_N
Re. GEN. 45_1
Re. GEN. 45_2
Re. GEN. 45_N
CHAN. EST. GEN. 28
DURA. GEN. 43_S
SYNC. DETECT. 82_1
SYNC. DETECT. 82_2
SYNC. DETECT. 82_N
START DURA. GEN. 21_1
START DURA. GEN. 21_2
START DURA. GEN. 21_N
TIMING GEN. 12_1
TIMING GEN. 12_2
TIMING GEN. 12_N
THRESHOLD STORAGE 76_1
RELIA. DECISION 75_1
76_2
75_2
76_N
75_N
ts
te_1
te_2
te_N
TSS_1
TSS_2
TSS_N
r_{IC1}
r_{IC2}
r_{ICN}
44_1
44_2
44_N
11m
Es FROM 42_{S-1}
Re_1 FROM 42_{S-1}
Re_2 FROM 42_{S-1}
Re_N FROM 42_{S-1}
42_S
te FROM PROCESSOR 42_S FOR OTHER ANTENNA RECEIVED SIGNALS

FIG. 14

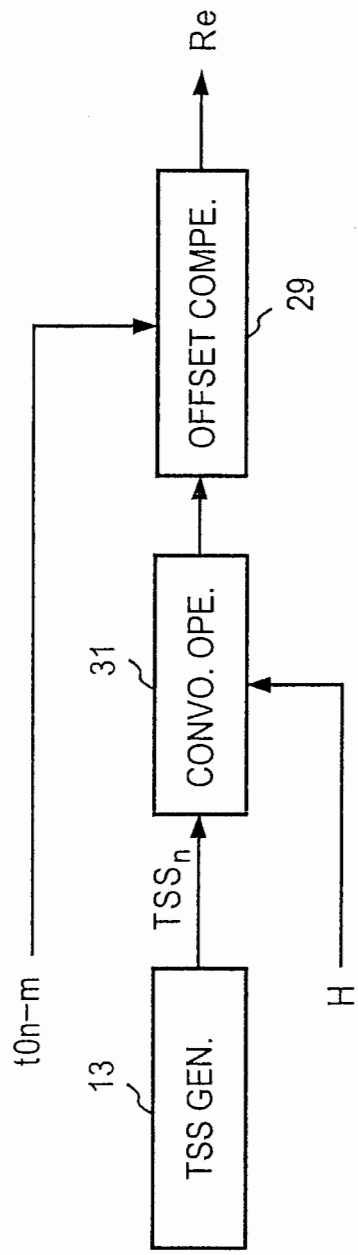


FIG. 15

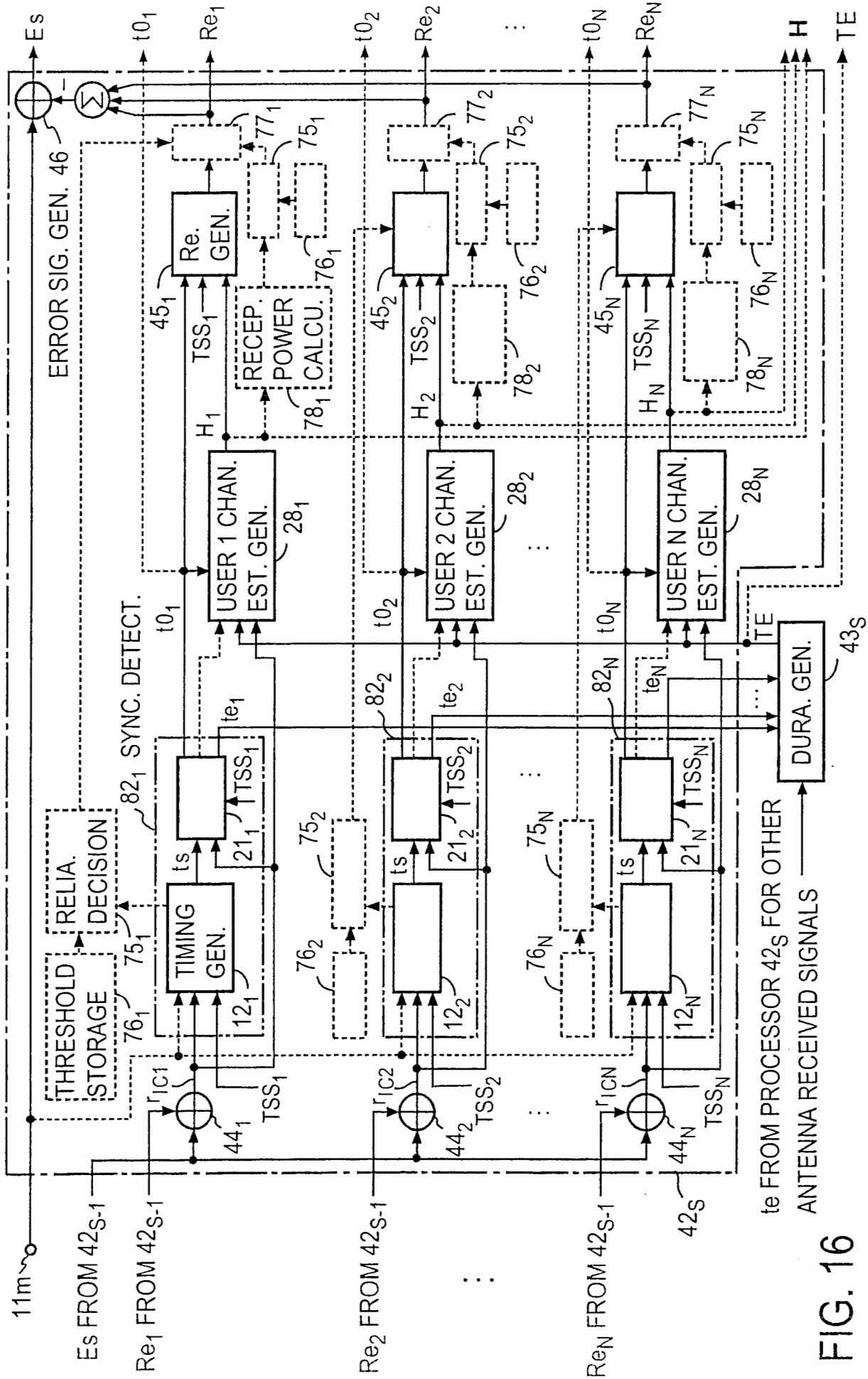

Es
t0$_1$
Re$_1$
t0$_2$
Re$_2$
t0$_N$
Re$_N$
H
TE
ERROR SIG. GEN. 46
Re. GEN.
RECEP. POWER CALCU.
USER 1 CHAN. EST. GEN.
USER 2 CHAN. EST. GEN.
USER N CHAN. EST. GEN.
SYNC. DETECT.
THRESHOLD STORAGE
RELIA. DECISION
TIMING GEN.
DURA. GEN.
11m
Es FROM 42$_{S-1}$
Re$_1$ FROM 42$_{S-1}$
Re$_2$ FROM 42$_{S-1}$
Re$_N$ FROM 42$_{S-1}$
42$_S$
te FROM PROCESSOR 42$_S$ FOR OTHER ANTENNA RECEIVED SIGNALS

FIG. 16

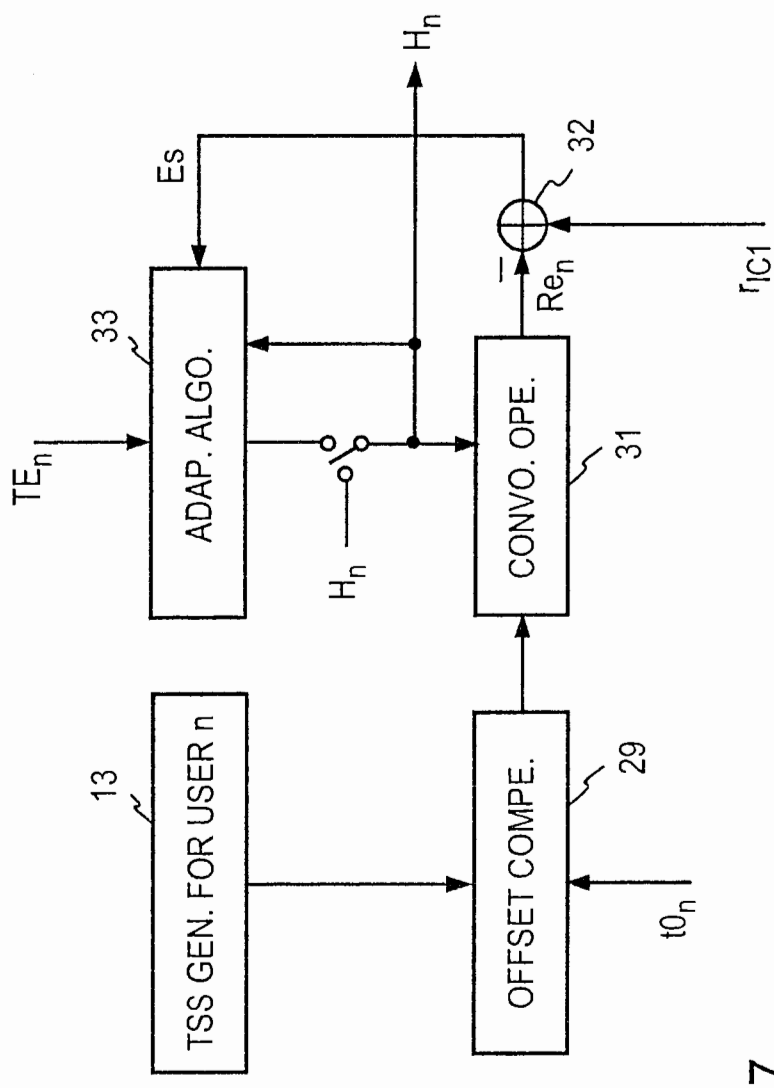

H_n
Es
32
Re_n
r_{IC1}
33
ADAP. ALGO.
TE_n
H_n
CONVO. OPE.
31
13
TSS GEN. FOR USER n
OFFSET COMPE.
29
$t0_n$

FIG. 17

FIG. 18

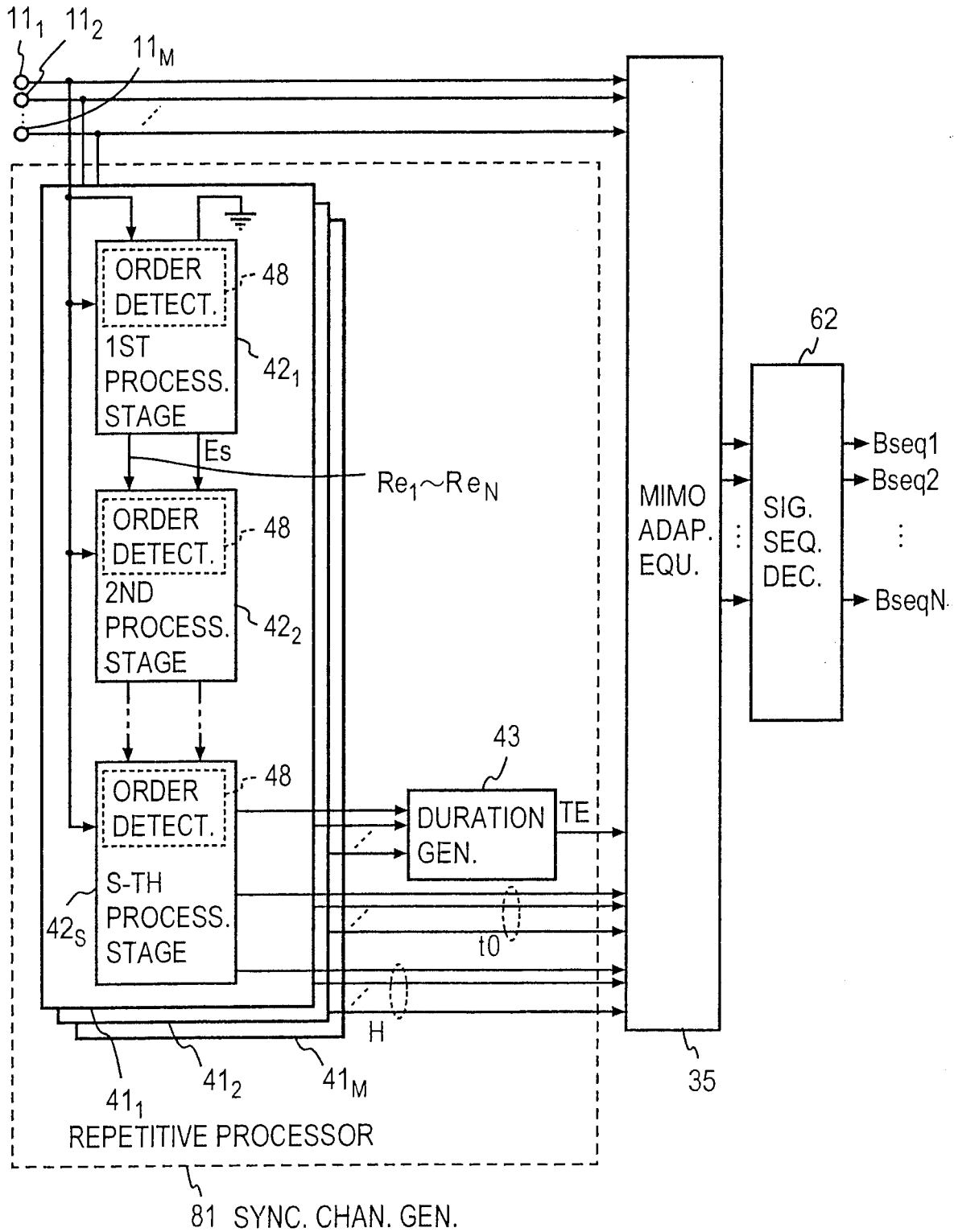
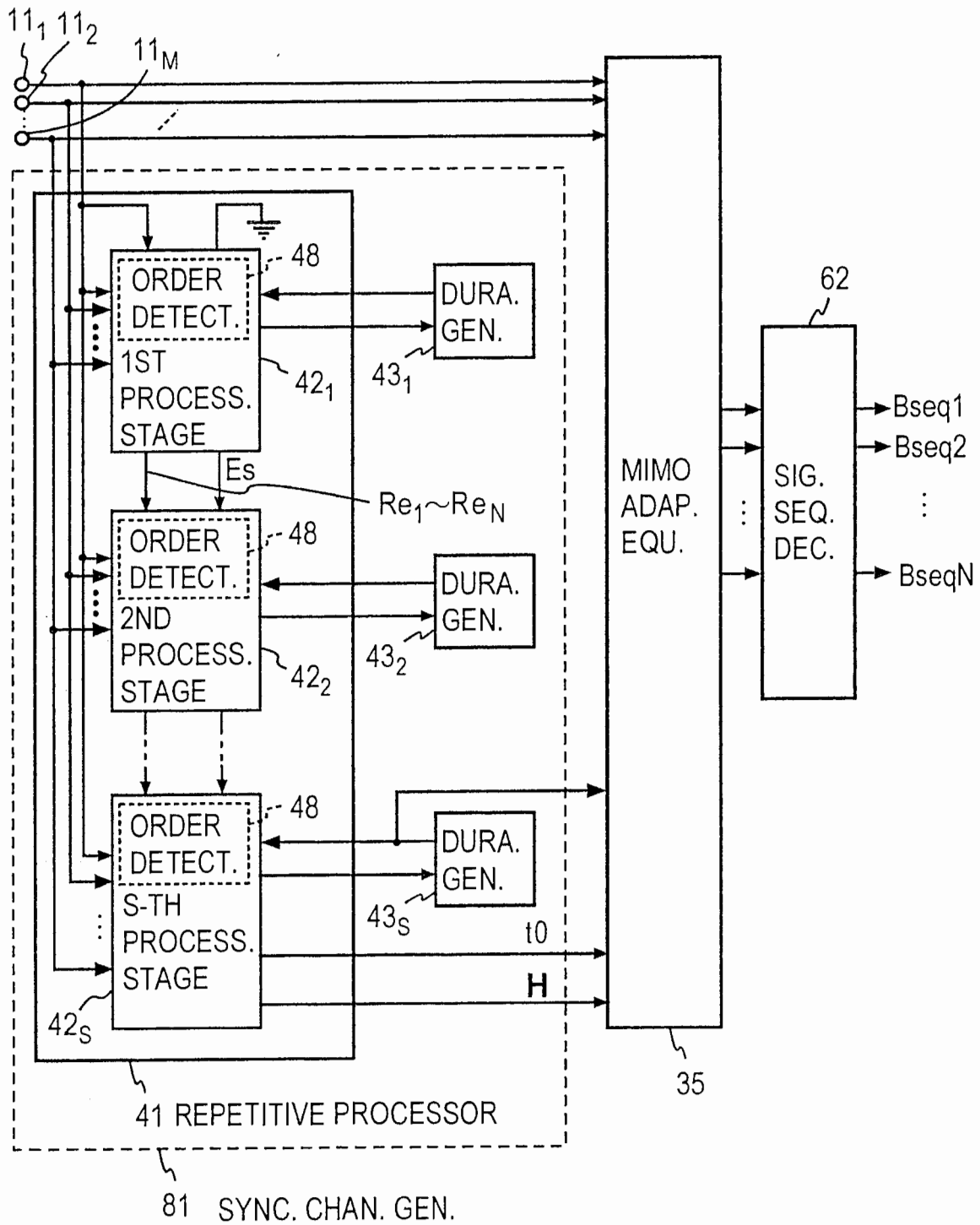

11_1 11_2 11_M
ORDER DETECT.
48
1ST PROCESS. STAGE
42_1
Es
$Re_1 \sim Re_N$
ORDER DETECT.
48
2ND PROCESS. STAGE
42_2
ORDER DETECT.
48
S-TH PROCESS. STAGE
42_S
43
DURATION GEN.
TE
t0
H
41_1
41_2
41_M
REPETITIVE PROCESSOR
81 SYNC. CHAN. GEN.
MIMO ADAP. EQU.
35
62
SIG. SEQ. DEC.
Bseq1
Bseq2
BseqN

FIG. 19


11_1 11_2
11_M
ORDER DETECT.
1ST PROCESS. STAGE
48
42_1
DURA. GEN.
43_1
Es
$Re_1 \sim Re_N$
ORDER DETECT.
2ND PROCESS. STAGE
48
42_2
DURA. GEN.
43_2
ORDER DETECT.
S-TH PROCESS. STAGE
48
42_S
DURA. GEN.
43_S
t0
H
41 REPETITIVE PROCESSOR
81 SYNC. CHAN. GEN.
MIMO ADAP. EQU.
35
62
SIG. SEQ. DEC.
Bseq1
Bseq2
BseqN

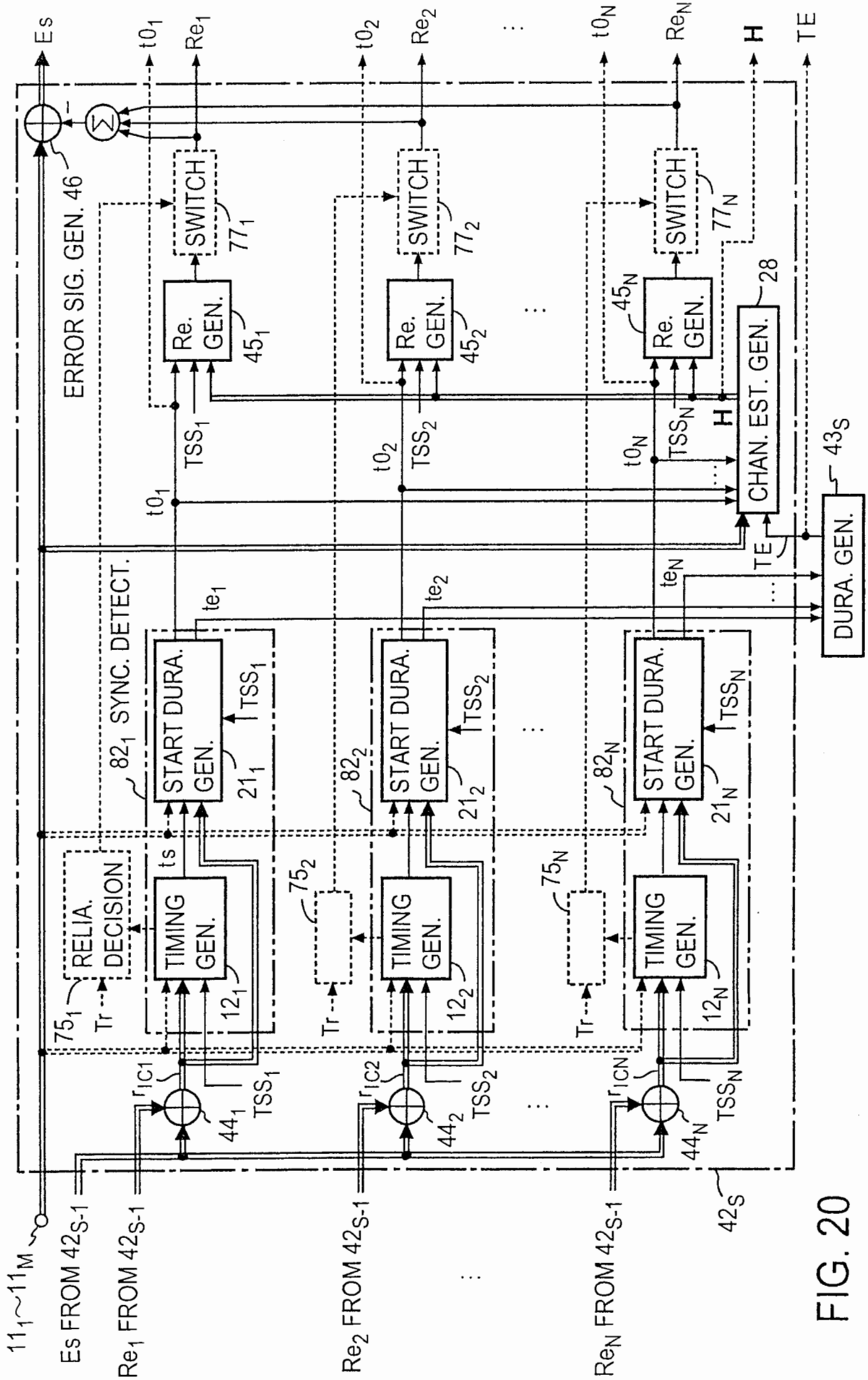

Es
$t0_1$
Re_1
$t0_2$
Re_2
$t0_N$
Re_N
H
TE
ERROR SIG. GEN. 46
SWITCH 77_1
SWITCH 77_2
SWITCH 77_N
Re. GEN. 45_1
Re. GEN. 45_2
Re. GEN. 45_N
CHAN. EST. GEN. 28
DURA. GEN. 43_S
TSS_1
TSS_2
TSS_N
te_1
te_2
te_N
82_1 SYNC. DETECT.
START DURA. GEN. 21_1
START DURA. GEN. 21_2
START DURA. GEN. 21_N
ts
RELIA. DECISION 75_1
75_2
75_N
Tr
TIMING GEN. 12_1
TIMING GEN. 12_2
TIMING GEN. 12_N
r_{IC1}
r_{IC2}
r_{ICN}
44_1
44_2
44_N
42_S
$11_1 \sim 11_M$
Es FROM 42_{S-1}
Re_1 FROM 42_{S-1}
Re_2 FROM 42_{S-1}
Re_N FROM 42_{S-1}

FIG. 20

FIG. 21A

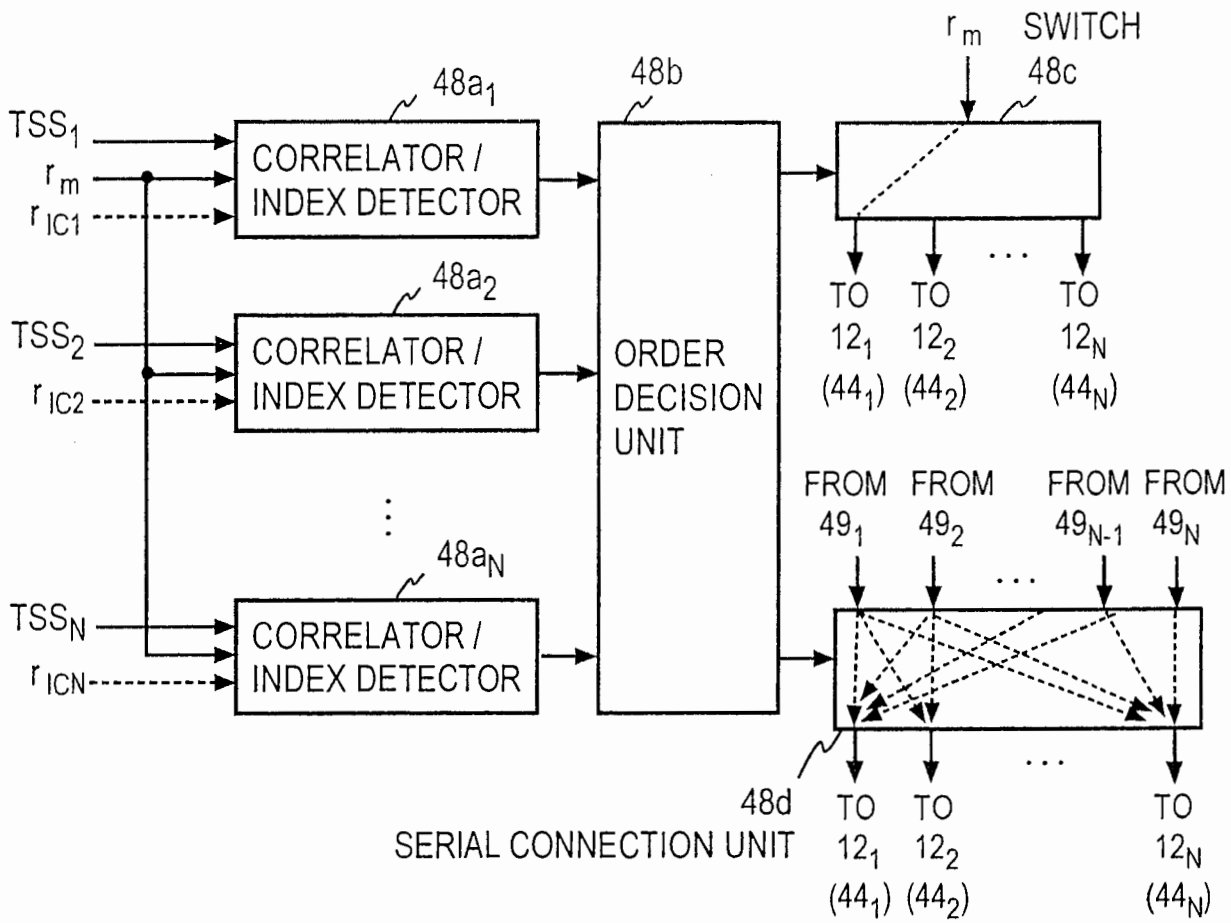
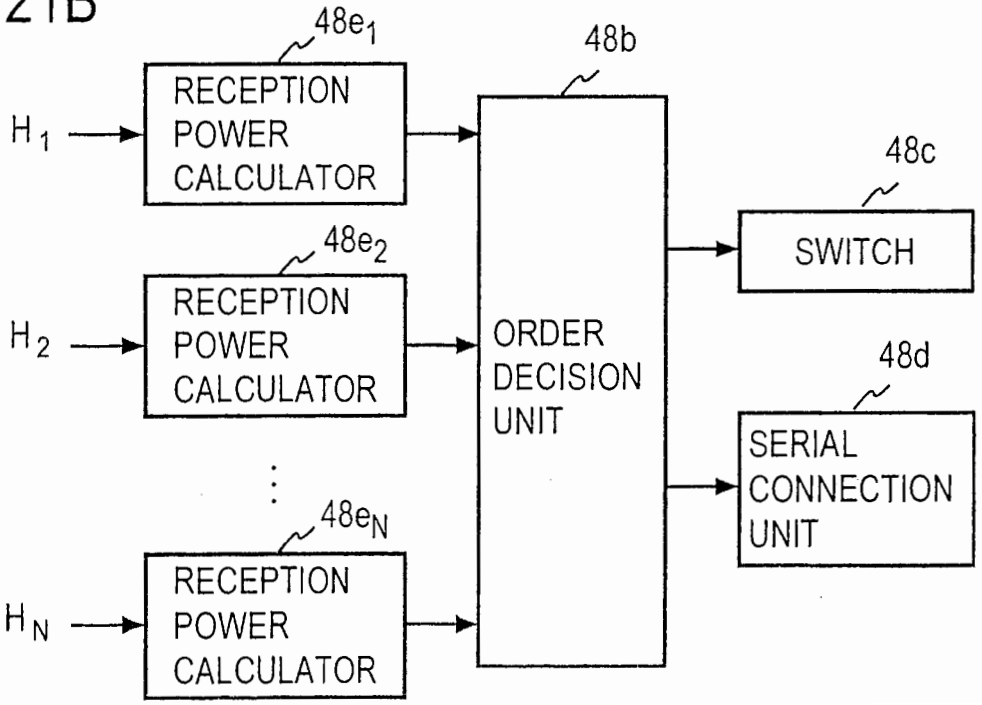


FIG. 21B



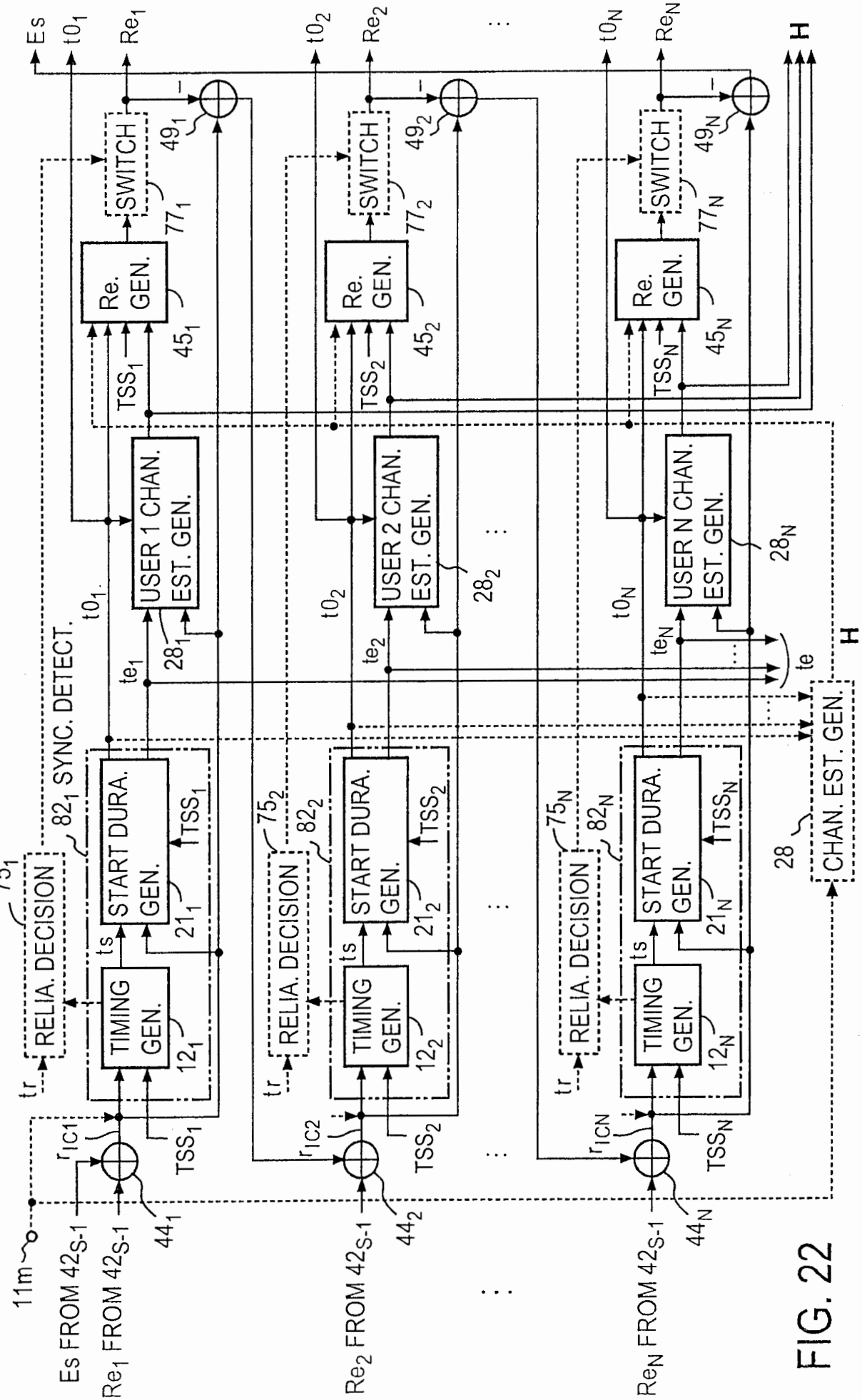
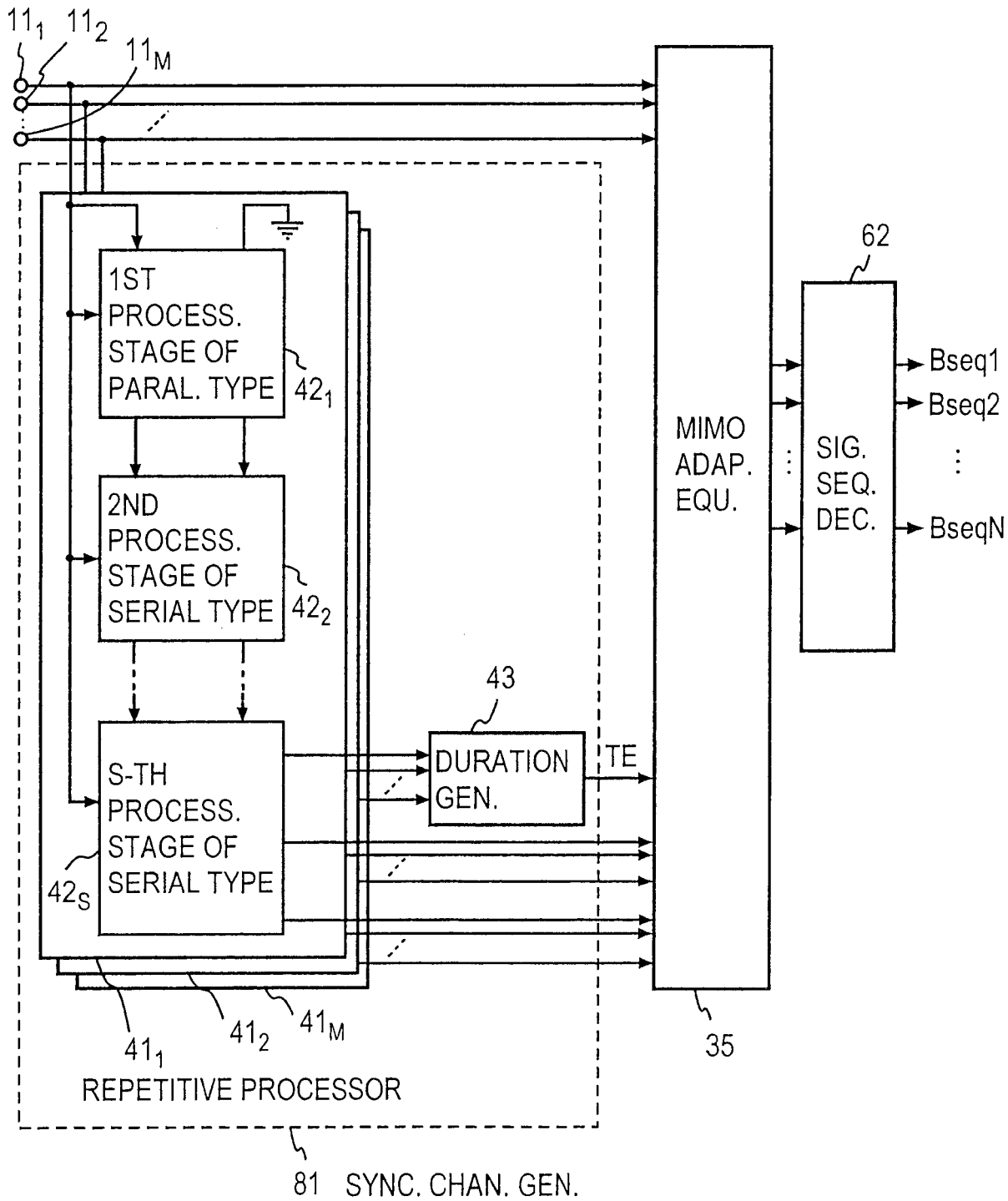

Es
$t0_1$
Re_1
$t0_2$
Re_2
$t0_N$
Re_N
H
SWITCH
77_1
77_2
77_N
49_1
49_2
49_N
Re. GEN.
45_1
45_2
45_N
TSS_1
TSS_2
TSS_N
USER 1 CHAN. EST. GEN.
USER 2 CHAN. EST. GEN.
USER N CHAN. EST. GEN.
28_1
28_2
28_N
te_1
te_2
te_N
te
28
CHAN. EST. GEN.
75_1
75_2
75_N
RELIA. DECISION
82_1
82_2
82_N
SYNC. DETECT.
tr
ts
START DURA. GEN.
21_1
21_2
21_N
TIMING GEN.
12_1
12_2
12_N
r_{IC1}
r_{IC2}
r_{ICN}
44_1
44_2
44_N
11m
Es FROM 42_{S-1}
Re_1 FROM 42_{S-1}
Re_2 FROM 42_{S-1}
Re_N FROM 42_{S-1}

FIG. 22

FIG. 23


11_1
11_2
11_M
1ST PROCESS. STAGE OF PARAL. TYPE
42_1
2ND PROCESS. STAGE OF SERIAL TYPE
42_2
S-TH PROCESS. STAGE OF SERIAL TYPE
42_S
43
DURATION GEN.
TE
MIMO ADAP. EQU.
35
62
SIG. SEQ. DEC.
Bseq1
Bseq2
BseqN
41_1
41_2
41_M
REPETITIVE PROCESSOR
81 SYNC. CHAN. GEN.

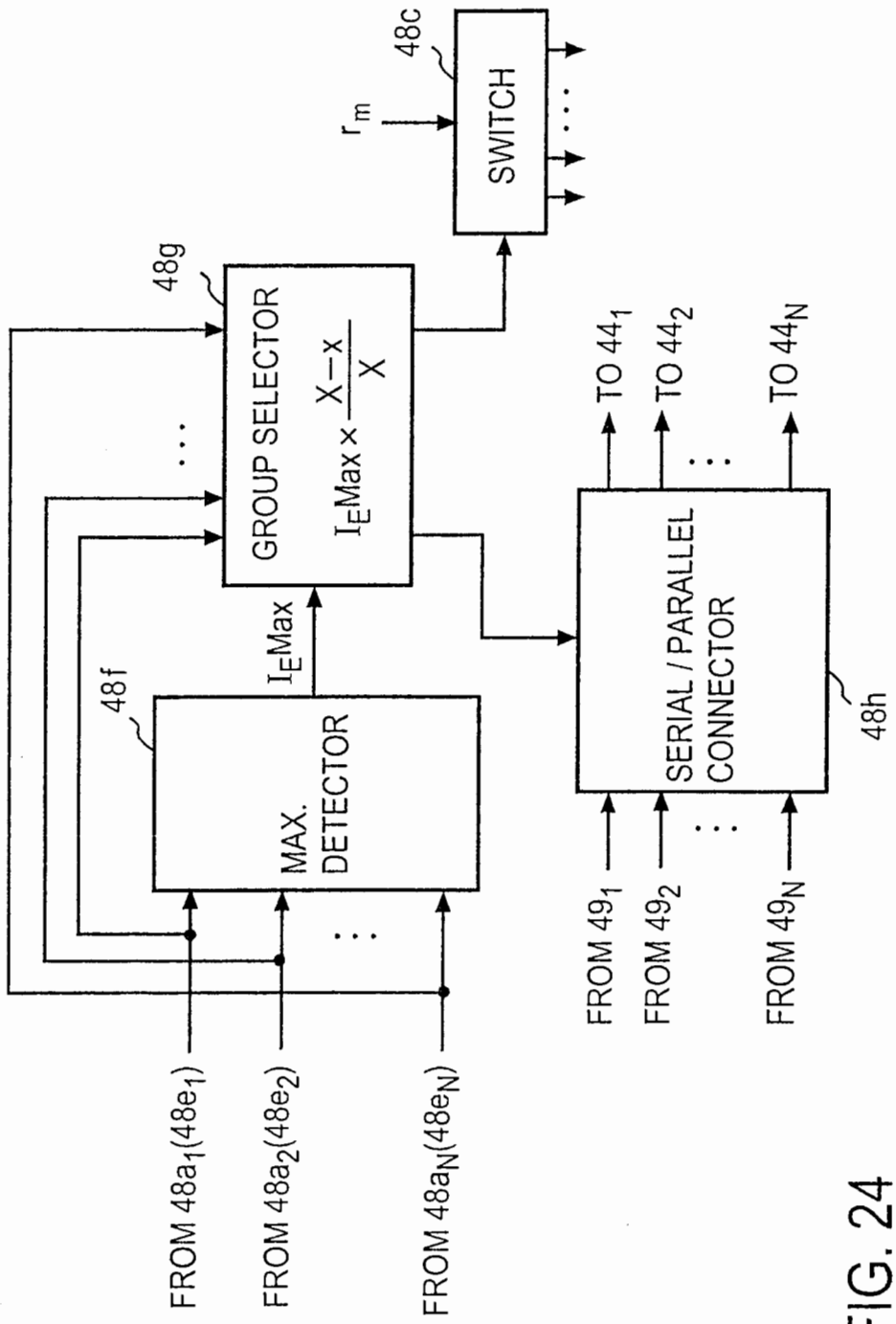

48c
SWITCH
r_m
48g
GROUP SELECTOR
$I_E Max \times \frac{X-x}{X}$
$I_E Max$
48f
MAX. DETECTOR
SERIAL / PARALLEL CONNECTOR
48h
TO 44_1
TO 44_2
TO 44_N
FROM 49_1
FROM 49_2
FROM 49_N
FROM $48a_1(48e_1)$
FROM $48a_2(48e_2)$
FROM $48a_N(48e_N)$

FIG. 24

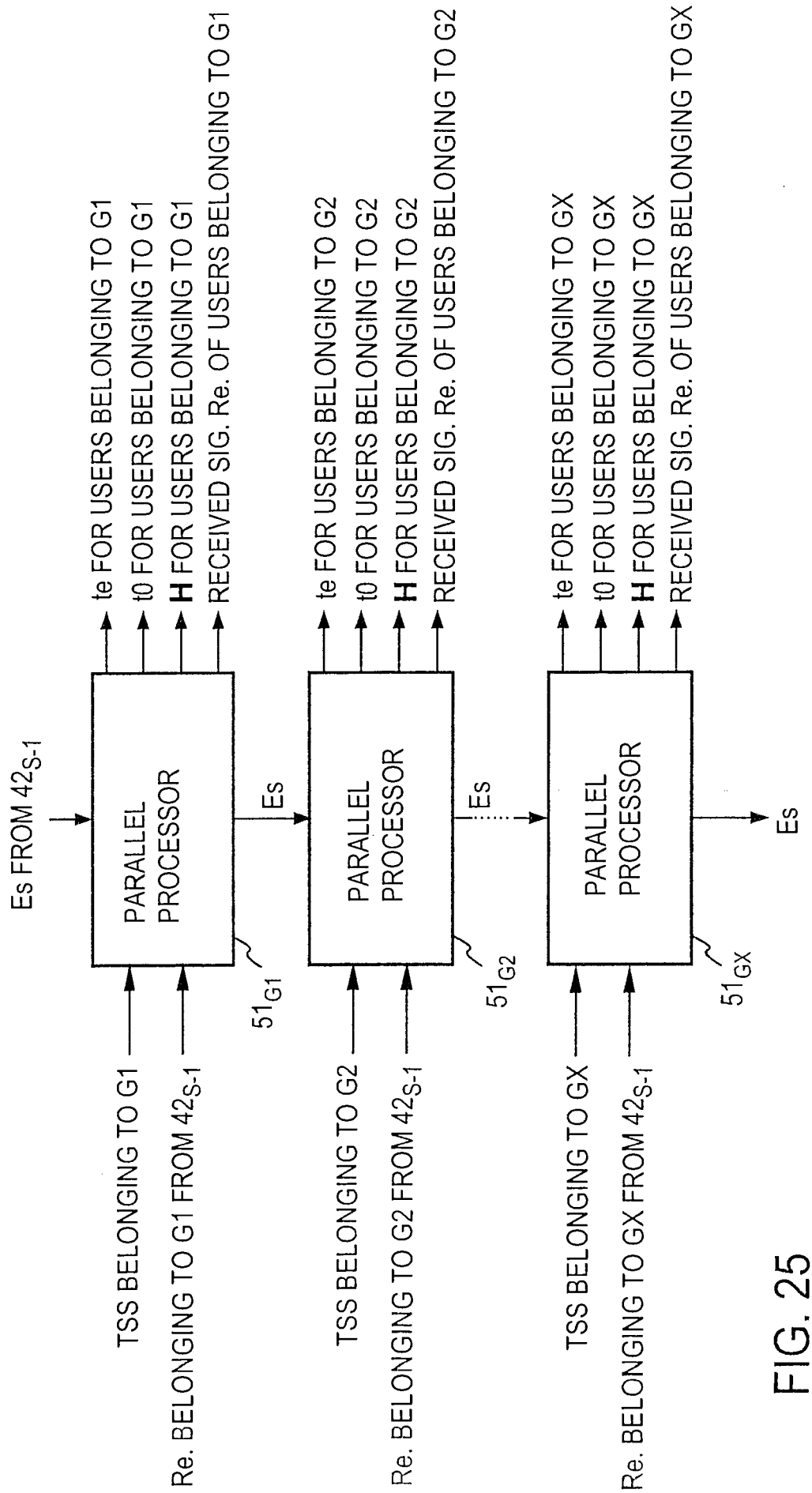
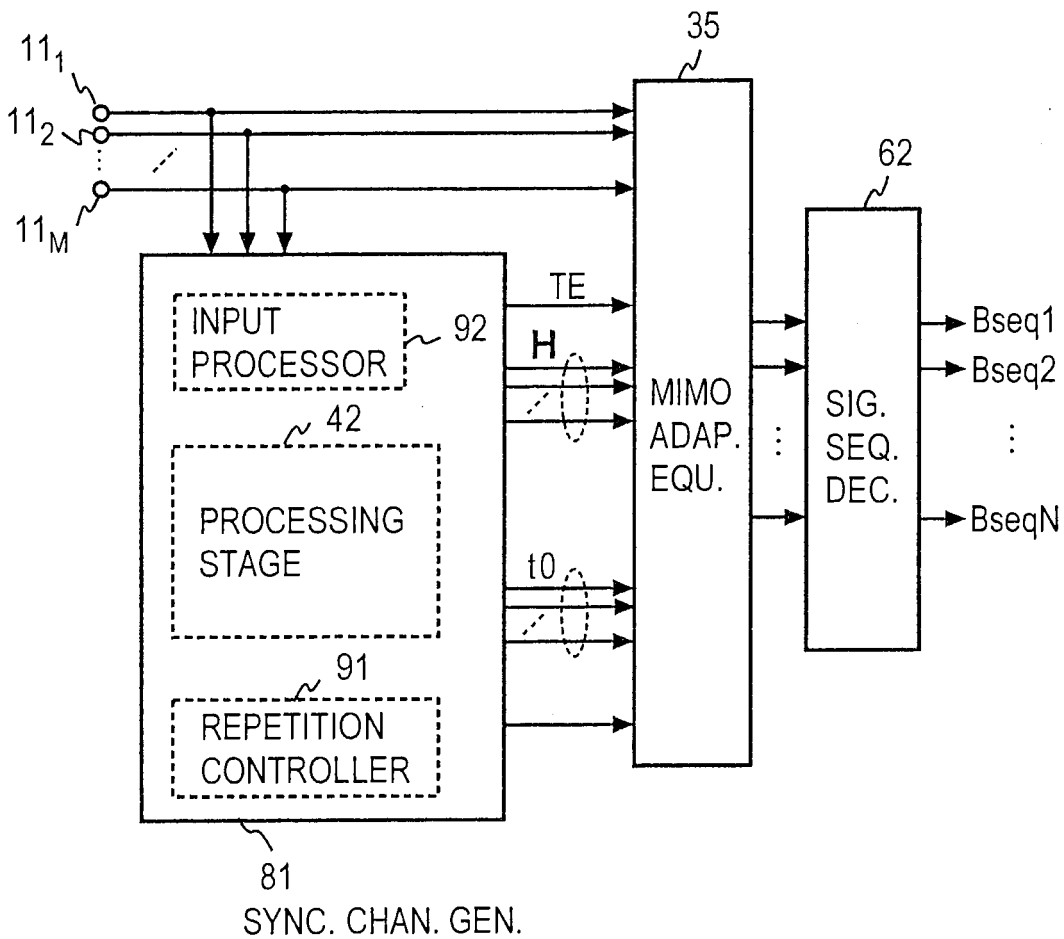

Es FROM 42S-1
PARALLEL PROCESSOR
te FOR USERS BELONGING TO G1
t0 FOR USERS BELONGING TO G1
H FOR USERS BELONGING TO G1
RECEIVED SIG. Re. OF USERS BELONGING TO G1
TSS BELONGING TO G1
Re. BELONGING TO G1 FROM 42S-1
51G1
Es
PARALLEL PROCESSOR
te FOR USERS BELONGING TO G2
t0 FOR USERS BELONGING TO G2
H FOR USERS BELONGING TO G2
RECEIVED SIG. Re. OF USERS BELONGING TO G2
TSS BELONGING TO G2
Re. BELONGING TO G2 FROM 42S-1
51G2
Es
PARALLEL PROCESSOR
te FOR USERS BELONGING TO GX
t0 FOR USERS BELONGING TO GX
H FOR USERS BELONGING TO GX
RECEIVED SIG. Re. OF USERS BELONGING TO GX
TSS BELONGING TO GX
Re. BELONGING TO GX FROM 42S-1
51GX
Es

FIG. 25

FIG. 26


11_1
11_2
11_M
35
62
INPUT PROCESSOR
92
42
PROCESSING STAGE
91
REPETITION CONTROLLER
81
SYNC. CHAN. GEN.
TE
H
t0
MIMO ADAP. EQU.
SIG. SEQ. DEC.
Bseq1
Bseq2
BseqN

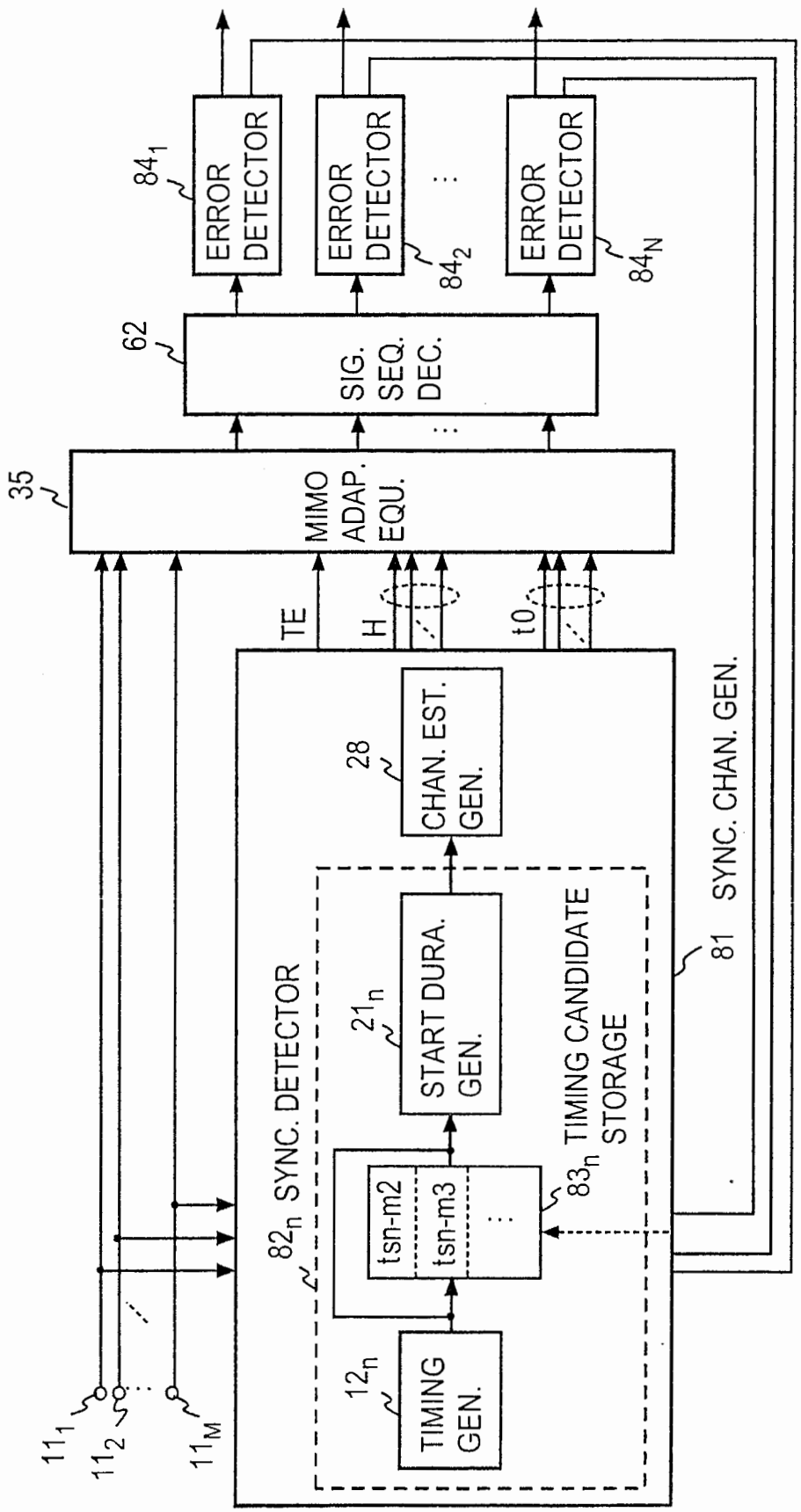

ERROR DETECTOR
84_1
ERROR DETECTOR
84_2
ERROR DETECTOR
84_N
62
SIG. SEQ. DEC.
35
MIMO ADAP. EQU.
TE
H
t0
28
CHAN. EST. GEN.
21_n
START DURA. GEN.
82_n SYNC. DETECTOR
83_n TIMING CANDIDATE STORAGE
tsn-m2
tsn-m3
12_n
TIMING GEN.
81 SYNC. CHAN. GEN.
11_1
11_2
11_M

FIG. 27

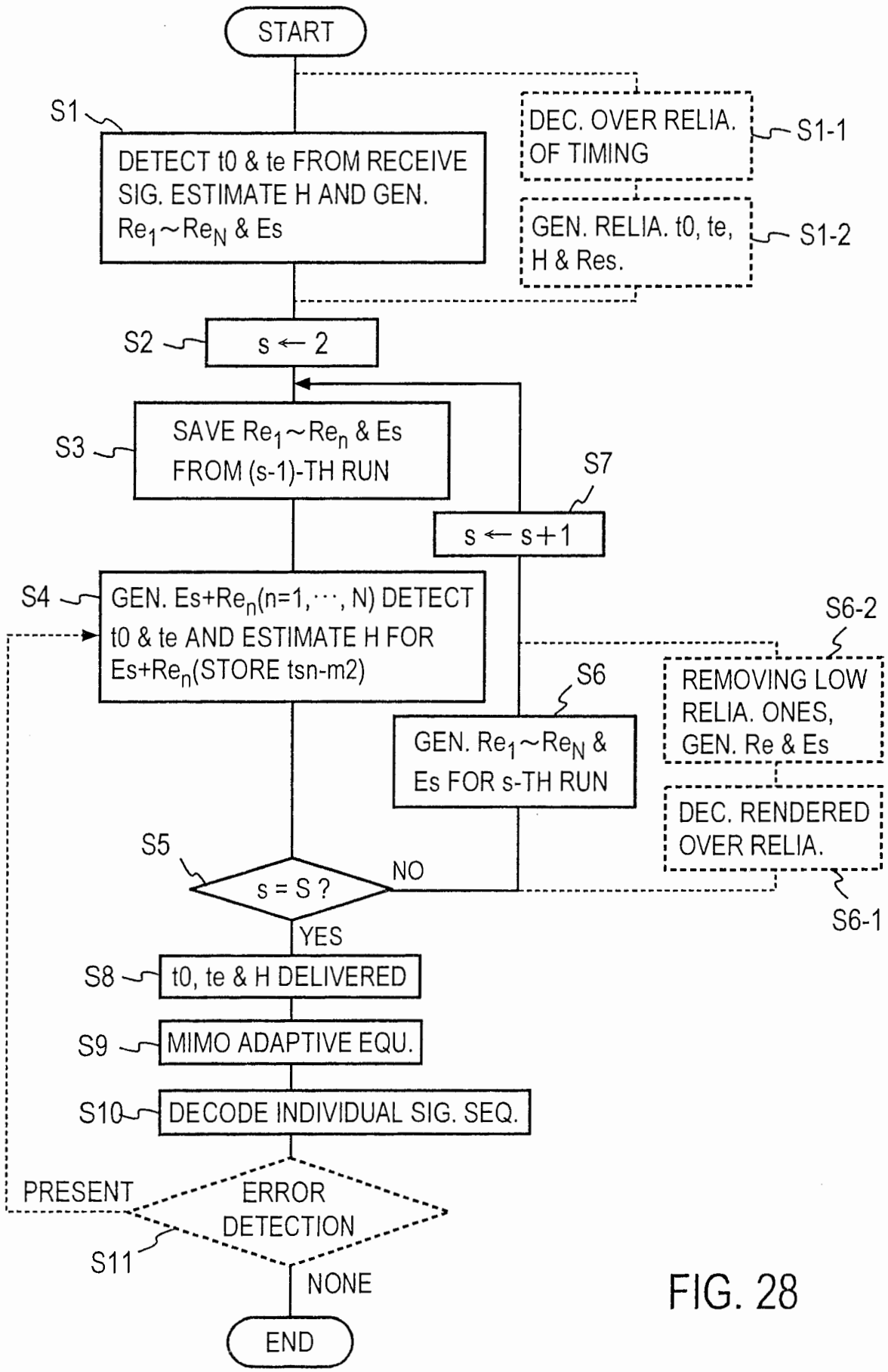

START
S1
DETECT t0 & te FROM RECEIVE SIG. ESTIMATE H AND GEN. Re1~ReN & Es
DEC. OVER RELIA. OF TIMING
S1-1
GEN. RELIA. t0, te, H & Res.
S1-2
S2
s ← 2
S3
SAVE Re1~Ren & Es FROM (s-1)-TH RUN
S7
s ← s+1
S4
GEN. Es+Ren(n=1,···, N) DETECT t0 & te AND ESTIMATE H FOR Es+Ren(STORE tsn-m2)
S6-2
REMOVING LOW RELIA. ONES, GEN. Re & Es
S6
GEN. Re1~ReN & Es FOR s-TH RUN
DEC. RENDERED OVER RELIA.
S6-1
S5
s = S ?
NO
YES
S8
t0, te & H DELIVERED
S9
MIMO ADAPTIVE EQU.
S10
DECODE INDIVIDUAL SIG. SEQ.
PRESENT
ERROR DETECTION
S11
NONE
END

FIG. 28

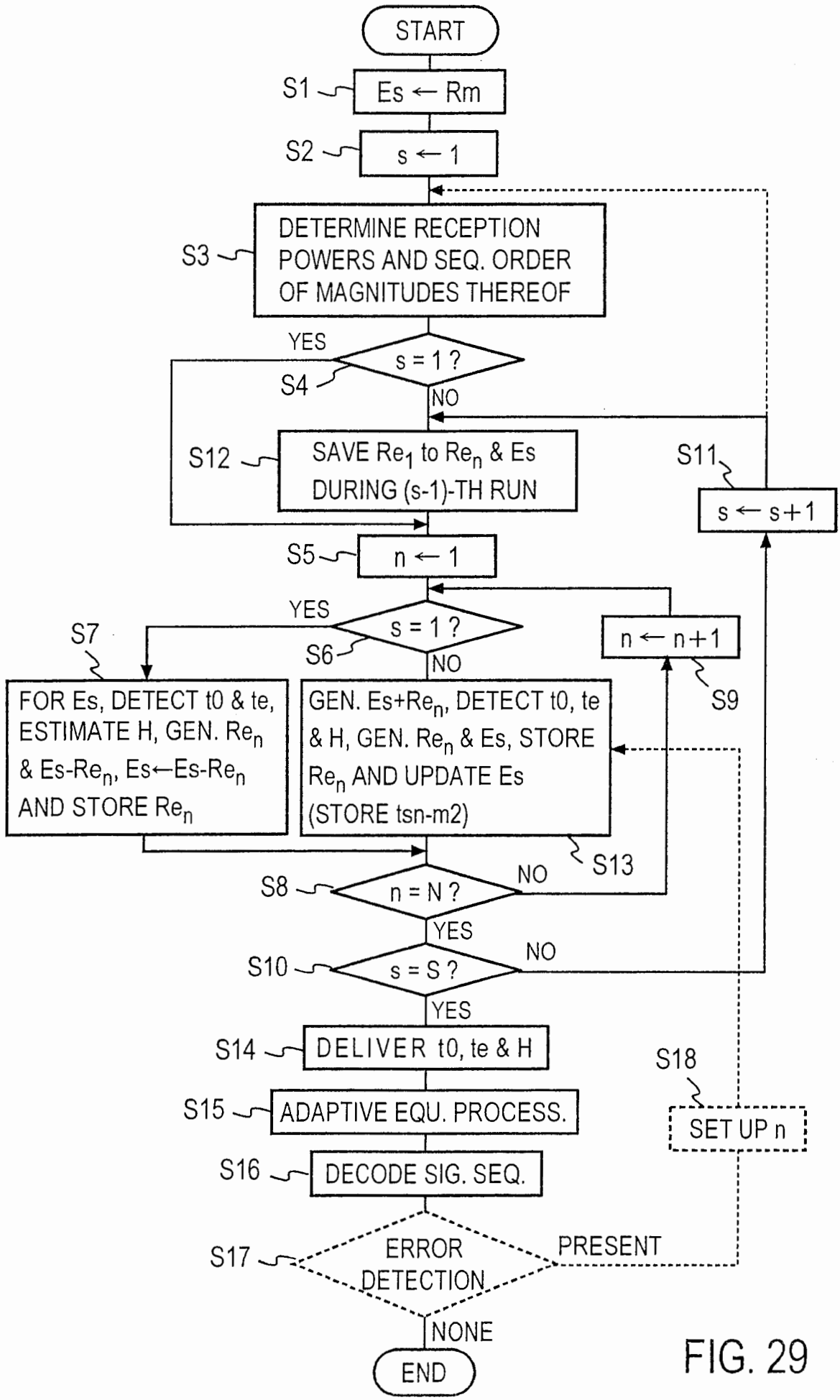

START
S1
Es ← Rm
S2
s ← 1
S3
DETERMINE RECEPTION POWERS AND SEQ. ORDER OF MAGNITUDES THEREOF
YES
S4
s = 1 ?
NO
S12
SAVE Re1 to Ren & Es DURING (s-1)-TH RUN
S11
s ← s+1
S5
n ← 1
YES
S7
S6
s = 1 ?
NO
n ← n+1
S9
FOR Es, DETECT t0 & te, ESTIMATE H, GEN. Ren & Es-Ren, Es←Es-Ren AND STORE Ren
GEN. Es+Ren, DETECT t0, te & H, GEN. Ren & Es, STORE Ren AND UPDATE Es (STORE tsn-m2)
S13
S8
n = N ?
NO
YES
S10
s = S ?
NO
YES
S14
DELIVER t0, te & H
S18
S15
ADAPTIVE EQU. PROCESS.
SET UP n
S16
DECODE SIG. SEQ.
S17
ERROR DETECTION
PRESENT
NONE
END

FIG. 29

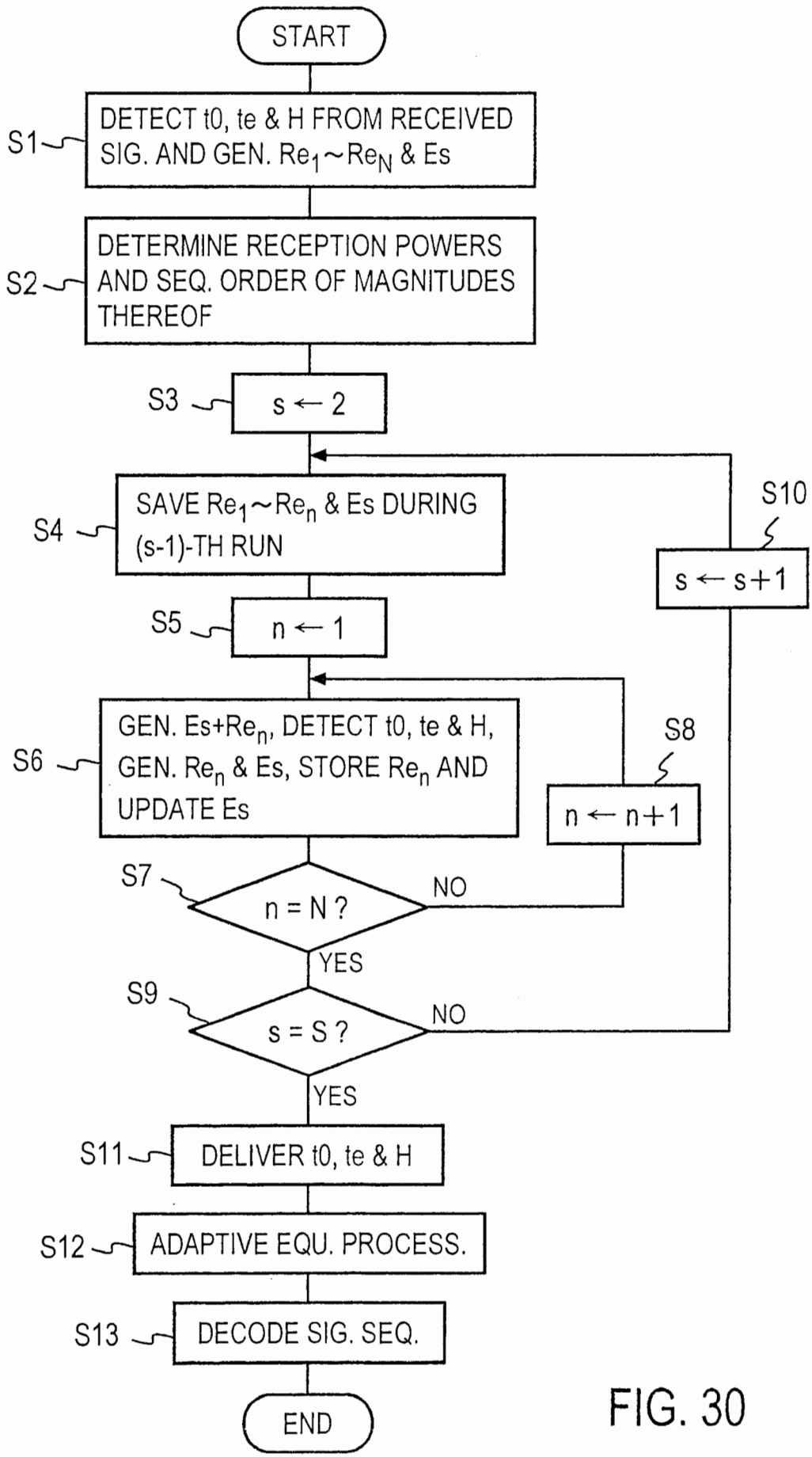

START
S1
DETECT t0, te & H FROM RECEIVED SIG. AND GEN. Re_1~Re_N & Es
S2
DETERMINE RECEPTION POWERS AND SEQ. ORDER OF MAGNITUDES THEREOF
S3
s ← 2
S4
SAVE Re_1~Re_n & Es DURING (s-1)-TH RUN
S5
n ← 1
S6
GEN. Es+Re_n, DETECT t0, te & H, GEN. Re_n & Es, STORE Re_n AND UPDATE Es
S7
n = N ?
NO
YES
S8
n ← n+1
S9
s = S ?
NO
YES
S10
s ← s+1
S11
DELIVER t0, te & H
S12
ADAPTIVE EQU. PROCESS.
S13
DECODE SIG. SEQ.
END

FIG. 30

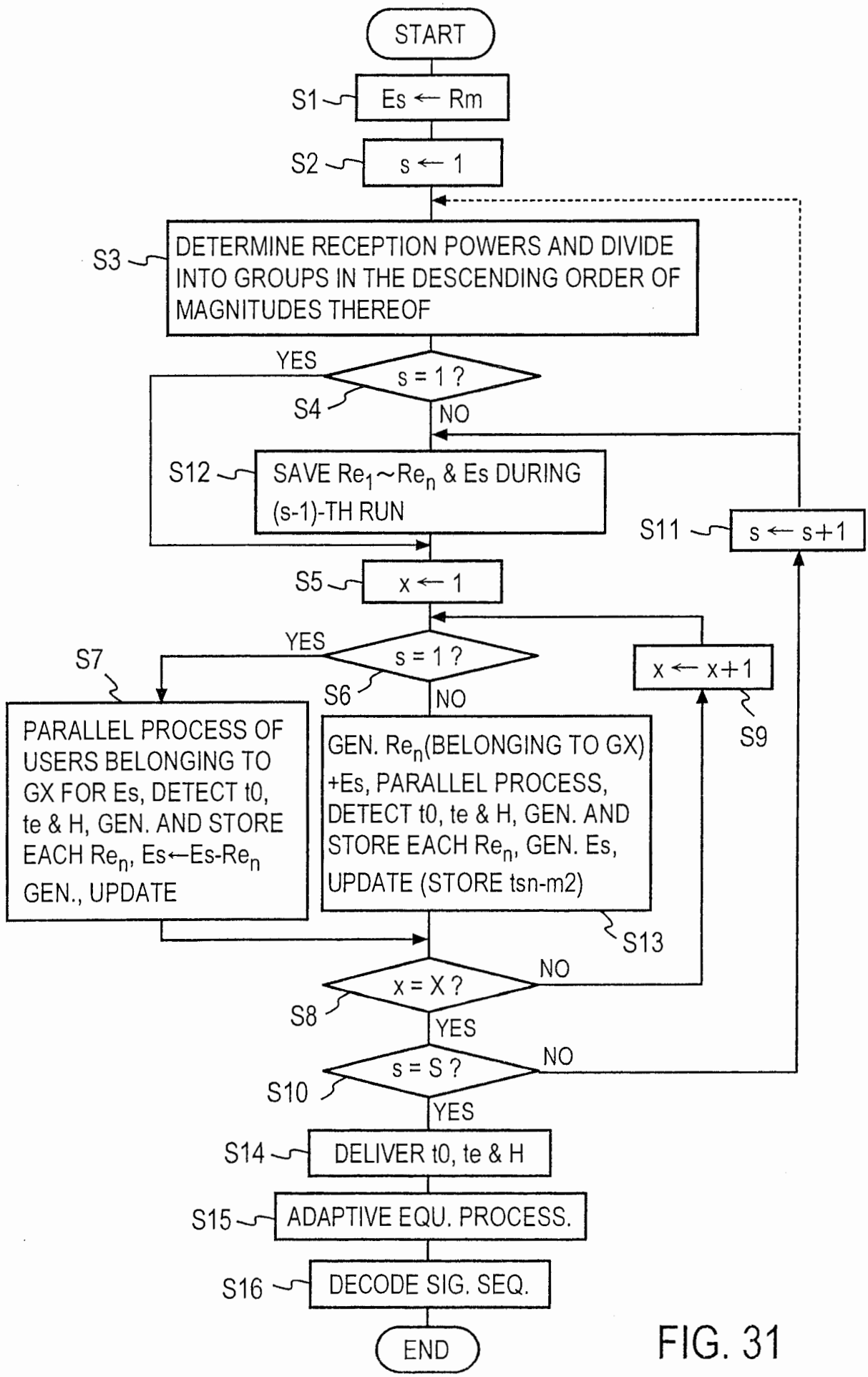

START
S1
Es ← Rm
S2
s ← 1
S3
DETERMINE RECEPTION POWERS AND DIVIDE INTO GROUPS IN THE DESCENDING ORDER OF MAGNITUDES THEREOF
YES
s = 1 ?
S4
NO
S12
SAVE Re1~Ren & Es DURING (s-1)-TH RUN
S11
s ← s+1
S5
x ← 1
YES
s = 1 ?
S7
S6
NO
x ← x+1
S9
PARALLEL PROCESS OF USERS BELONGING TO GX FOR Es, DETECT t0, te & H, GEN. AND STORE EACH Ren, Es←Es-Ren GEN., UPDATE
GEN. Ren(BELONGING TO GX) +Es, PARALLEL PROCESS, DETECT t0, te & H, GEN. AND STORE EACH Ren, GEN. Es, UPDATE (STORE tsn-m2)
S13
NO
x = X ?
S8
YES
NO
s = S ?
S10
YES
S14
DELIVER t0, te & H
S15
ADAPTIVE EQU. PROCESS.
S16
DECODE SIG. SEQ.
END

FIG. 31