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(54) IMPROVEMENTS IN OR RELATING TO PHOTOVOLTAIC DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 222 (formerly of 195) Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to photovoltaic detectors and solar cells. Twenty years after the invention of the silicon solar cell, the photovoltaic solar power plant is still an elusive goal. About two orders of magnitude more capital is required for silicon power station than for one burning fossil fuel (\$0.40 per average watt). At fault are the processing costs resulting from the requirement for high quality bulk material and for shallow p-n homojunctions. Bulk silicon is needed because of the large absorption length ($\sim 100\mu\text{m}$) in this indirect band gap material. In particular, p-n junctions must be shallow (a few tenths of a micrometer) for a trade-off between high efficiency and low surface recombination.

Alternatives to silicon involve direct-gap materials with large absorption coefficients. With these, processing and materials costs can be reduced because thin films and even polycrystalline films may be used. Nevertheless, large absorption coefficients impose even more stringent processing requirements for shallow p-n homojunctions. Thus, the next logical step in cost reduction is to produce the p-n junction

successfully in such materials by depositing, on top of the absorbing semiconductor film, a relatively thick film of an essentially transparent semiconductor of opposite conductivity type, to produce a heterojunction.

The principle of the heterodiode has been known for over twenty years and, consequently, any two semiconductors can be joined together so as to form a heterojunction. Indeed—as was noted by J. J. Loferski in an article entitled "Principles of Photovoltaic Solar Energy Conversion," published in the 25th Annual Proceedings of the Power Sources Conference, May 1972, "The number of possible heterojunction type cells is limited only by the imagination."

Out of this unlimited choice, however, the materials for a workable heterojunction photovoltaic solar cell must satisfy at least five important criteria. These criteria include:

- (1) the electron affinities are such that there exists no barrier impeding current flow;
- (2) there is a large difference in band gap between the two materials in order to collect a large fraction of the solar spectrum;
- (3) the bandgap of the smaller bandgap material should lie in the range between 1.0 to 1.5 eV for high efficiency;
- (4) there should be a small lattice mismatch between the materials; and
- (5) there should be a small difference in the thermal coefficients of expansion of the two materials.

Thus, while A. K. Sreedhar, B. L. Sharma and R. K. Purohit, in their article entitled "Efficiency Calculations for some p-n and

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n-p Heterojunctions", published in *Physica Status Solidi* (a), Volume 3, page K217 (1970), list p-InP/n-CdS as heterojunction-forming materials, it is significant to note that in a subsequently published book ("Semiconductor Heterojunctions", Pergamon Press) written by two of the three coauthors, B. L. Sharma and R. K. Purhoit, the p-InP/n-CdS combination is omitted. In particular, they note at page 133, that "It can be seen from earlier chapters that the diversity of electrical and optical properties together with inadequate understanding of interface states of heterojunctions make it difficult to predict their precise characteristics. At present it is primarily this difficulty which prevents heterojunctions from competing with some of the conventional homojunction devices".

According to the present invention there is provided a light-responsive device comprising a p-type indium phosphide layer, a heterojunction-forming and light-transmissive window of n-type cadmium sulphide formed on the p-type layer, a light-transmissive electrode deposited on the cadmium sulphide window, and means for establishing conductive contact to a surface of the indium phosphide layer remote from the window.

The invention also provides a solar cell device comprising a supporting electrode comprising a zinc-containing conducting metal, a solar-energy absorbing body of p-type indium phosphide disposed on the supporting electrode, a heterojunction-forming and solar-energy transmissive window of n-type cadmium sulphide deposited on the indium phosphide p-type body, a solar-energy transmissive electrode deposited on the cadmium sulphide and a protective solar-energy transmissive body over the cadmium sulphide and the transmissive electrode.

The invention further provides a method of making a light-responsive device comprising forming a layer of n-type cadmium sulphide on a p-type layer of indium phosphide, the cadmium sulphide layer being light-transmissive, thus forming a heterojunction between the layers, depositing a light-transmissive electrode on the cadmium sulphide layer, establishing a conductive contact to a surface of the indium phosphide layer and annealing the device at a temperature of from 400°C to 625°C.

A p-InP/n-CdS photovoltaic cell may be formed wherein the junction is formed between (111) InP and (0001) CdS. This can be achieved by either growing cadmium sulphide on the (111) surface of indium phosphide, or, alternatively, indium phosphide can be grown on a surface in the (0001) crystalline plane of a cadmium sulphide crystal. In either case, the desired (111) InP—(0001) CdS interface is formed.

Photovoltaic cells constructed in this manner

have been measured to have solar efficiencies of up to 12.5 percent. It has been discovered, however, that the solar efficiency can be further improved to 14 percent by a brief annealing step. More specifically, the heterojunction is annealed in a slightly reducing atmosphere for a time period in a range encompassing the time period of 15 minutes and at a temperature in the range of from about 400 degrees centigrade to about 625 degrees centigrade. The slightly reducing atmosphere appears to prevent undue increase in the resistivity of the CdS. The physical cause of the efficiency improvement is as yet not established, but is reliably reproducible.

The preferred annealing temperature is in the range from about 550 degrees centigrade to about 600 degrees centigrade. For temperatures below these limits, but within the broader range specified above, the annealing time is desirably adjusted in inverse dependence on the temperature change.

It has also been discovered that the slightly reducing atmosphere is preferably a mixture including mainly a substantially inert component and a minor portion of hydrogen. A still more specifically preferred mixture is a mixture of H₂ and N₂, such as forming gas (15% H₂+85% N₂).

It is surprising that even heterojunctions of InP and CdS which appear to be inferior, based on measurements taken across the junction via a temporary contact to the CdS, can be improved to 14 percent overall solar efficiency in the finished cell by employing the foregoing annealing procedure.

It is also surprising that such a short annealing time can have a beneficial effect on such a semiconductive heterojunction.

Embodiments of the invention will now be described by way of example with reference to the accompanying drawings, in which:—

FIG. 1 is a partially pictorial and partially schematic illustration of a photovoltaic cell being used as a detector;

FIG. 2 shows a potential energy diagram with respect to distance through the photovoltaic device of FIG. 1;

FIG. 3 shows curves illustrating the solar conversion efficiency of a device according to FIG. 1 as compared to other competitive devices;

FIG. 4 shows curves illustrating photocurrent versus photovoltage characteristics;

FIG. 5 shows a typical cross-section of a solar cell in the form of a large-area panel according to the invention;

FIG. 6 shows a partially pictorial and partially diagrammatic illustration of a typical mode of manufacturing solar panel sheet of the type illustrated in FIG. 5;

FIG. 7 is a partially pictorial and partially diagrammatic illustration of a solar cell undergoing annealing; and

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FIGS. 8 and 9 show various curves helpful in understanding the operation of the invention.

Referring to the drawings, FIG. 1 shows one embodiment of a photovoltaic cell in accordance with the present invention. The cell includes a crystalline body 11 of p-type indium phosphide in contact with a crystalline body 13 of n-type cadmium sulphide to form a heterojunction therebetween. More specifically, the contacting surfaces of said respective bodies 11 and 13 lie in the (111) crystalline plane of the indium phosphide crystal 11 and in the (0001) crystalline plane of the cadmium sulphide crystal 13. Electrical contact is made to the back, or far side of the CdS body by means of a transmissive indium electrode structure in the form of a grid 16. Electrical contact is made to the back side of the InP body by means of an Au/Zn/Au contact 12 to which a copper block 15 is connected by means of a layer of silver paste 14.

An external load resistor 17 is also shown connected between contact 16 and block 15.

Crystals of InP are grown by a liquid encapsulant technique and Cd or Zn is added as an acceptor impurity to achieve controlled p-type conductivity. The single crystalline ingot is oriented for cutting (111) wafers, which are then polished with a final Syton polish on one face. The p-type InP portion 11 of the heterodiodes had $\sim 2^{\text{nd}}$ -cm resistivity. The "back" contact 12 to the InP side of the final diode can be applied before or after growing the n-type CdS layer 13. When contact 12 is applied before, the Syton polished face is embedded in wax, and three films, i.e., Au, Zn and Au are successively electro-deposited on the InP. After removal of the wax, and boiling first in acetone, then in methanol, the metallic contact 12 is annealed for ~ 5 min at 475°C in forming gas.

When no contact 12 is applied to the InP wafer 11 before the CdS layer 13 growth, the wafer 11 is cleaned after the Syton polishing by boiling in acetone and then in methanol. The InP wafers 11, with or without contact, are now ready for CdS growth. They are immediately mounted, in a laminar flow hood (not shown), on a substrate holder which is then transferred to the CdS growth station. Also used are "Syton" polished InP wafers 11 which have been slightly etched in cold HCl before a final methanol rinse.

The apparatus for n-CdS growth is a modification of earlier apparatus developed by D. Beecham *Rev. Sci. Instrum.* 41, 1654, (1970) and S. Wagner *Applied Physics Letters*, 22 351 (1973); *Jo. Applied Physics*, 45, 246 (1974). Following mounting the InP substrate holder therein, the vacuum station used for the growth of CdS films 13 is closed and evacuated with oil-free pumps to a pressure $< 1 \times 10^{-5}$ Torr. The coaxial isothermal CdS source (not shown), which con-

tains elemental cadmium and elemental sulphur, is then heated to 350°C . Simultaneously the InP substrate holder is heated to 200 — 250°C . During the heat-up, a shutter separates the source compartment from the substrate.

When source and substrate have reached the set temperature the shutter is opened and a 5 to $10\mu\text{m}$ thick crystalline n-CdS film 13 is grown on the p-InP wafer 11. The rate of film growth is monitored with a quartz crystal oscillator. It is about $0.15\mu\text{m}/\text{min}$. When the desired film thickness has been reached the shutter is closed and both the source and the substrate heaters are turned off. The substrate holder is cooled to room temperature, the vacuum station is filled with nitrogen, opened, and the samples are removed. When the Au/Zn/Au contact 12 to the InP has been made prior to CdS growth, this contact 12 is now slightly buffed, and attached with silvered paste 14 to a copper block 15. Samples 11, 13 without Au/Zn/Au contact 12 are waxed with the CdS layer 13 down. Then the contact 12 is made by electroplating, and is sintered as described earlier. The InP wafer 11 is mounted on a copper block 15 by means of silver paste 14. On the CdS surface, a contact grid 16 of indium metal is applied although where annealing is to occur, no contact is deposited until the annealing step is complete.

The photovoltaic conversion efficiency, i.e., the ratio of the current in the external circuit to the photon flux incident upon the CdS surface, is displayed in FIG. 3 by curve 21, as a function of wavelength. The efficiency is uniformly 70% between 550 and 910 nm wavelength. The efficiency of p-n Si detectors, of p-CuInSi₂/n-CdS detectors, and the solar intensity spectrum at air mass 2 are shown for comparison by curves 22, 23 and 24 respectively. In the InP/CdS diodes, the cut-off, at ~ 550 nm results from absorption by CdS, that at ~ 910 nm from transmission through the InP.

Diodes like that in FIG. 1 which have been cleaved on all sides to reduce surface leakage currents have up to $10\text{ M}\Omega/\text{cm}^2$ (for 1 cm^2 diode area) resistance at 0 to IV reverse-bias. Forward series resistances of $\sim 10^{\text{th}}$ (for 1 cm^2 diode area) have been reached.

FIG. 4 shows the photocurrent/photovoltage characteristic of a InP/CdS solar cell 41 in comparison to that of a 9.5% efficient silicon solar cell 42. The light source is a solar simulator made up of a W-Halogen lamp at 3200K and a KG-2 filter resulting in an incident power density of $83\text{ mW}/\text{cm}^2$. The active area of the InP/CdS cell is 0.70 cm^2 , that of the Si cell is 0.90 cm^2 (however all data and the graph are converted to unit area). The power output under operating conditions is equal to the area of the $I_{\text{sc}} \times V_{\text{oc}}$ rectangles inscribed to the I-V curves. It is

6.28 mW/cm² for InP/CdS and 7.87 mW/cm² for the 9.5% efficient Si cell. Thus the InP/CdS cell is ~7.6% efficient. More recent InP/CdS cells (not shown) have efficiency of 12.5% under these same conditions. The efficiency of this prototype device is presently surpassed only by silicon and by gallium arsenide cells.

When forward biased, infrared light emission is observed from an InP/CdS cell, but no detailed measurements have yet been carried out.

It will be appreciated that there are a number of variations within the scope of the embodiments of the invention. These include: (1) increasing the open circuit voltage and reducing the forward resistance by varying the doping level of the InP, and by varying the growth conditions for the CdS, (2) achieving a higher short circuit current by experimenting with the InP doping level, (3) increasing the short circuit current by the application of an antireflection coating, (4) making InP/CdS diodes from thin films of InP and thin films of CdS as a first step towards an inexpensive solar cell, (5) reversing the procedure by growing the p-type indium phosphide on the (0001) surface of the n-type cadmium sulphide and (6) the lattice mismatch between InP and CdS can be reduced by the addition of about 10 more percent of CdSe to CdS. The tetrahedral interatomic distances are virtually identical, In-P=2.533 Å and Cd-S=2.532 Å. These interatomic distances are calculated from the tetrahedral radii listed in *Bonds and Bands in Semiconductors* by J. C. Phillips, Academic Press, New York (1973) p. 22. Thus, a good lattice match between InP and CdS can be expected regardless of the crystallographic orientation of the interface. This makes InP/CdS a promising candidate for an efficient thin film on thin film solar cell, as described hereinafter with reference to FIG. 5.

The absence of interfacial spikes is a fortunate and advantageous result of the heterojunction because of the potential energy and energy gap relationships through the heterojunction. Curves 31 through 36 in FIG. 2 represent these potential energy relationships as a function of distance through the diode in a direction normal to the heterojunction plane. The separation of curves 31 and 32 at the left-hand side of the diagram represent the energy gap for the p-type InP 11 and the separation of curves 34 and 36 at the right-hand side of the diagram represent the energy gap of the n-type CdS layer 13. The band edges bend toward each other in the junction region as shown by the curved portions of curves 31, 32, 34 and 36 where they join the potential barriers represented by curves 33 and 35.

In FIG. 5, typical proposed substrates (sheet 65 in FIG. 6) for structural support

and electrical contact in large-area solar panels are copper or stainless steel sheet. These are coated with a thin metal film (not shown) for improved contact to the semiconductor. Galvanized steel sheet may be an efficient and very inexpensive substrate for p-type indium phosphide layer 51. The zinc of the galvanic coating is the best acceptor element for making ohmic contact to the indium phosphide. Iron contamination of the InP may not be harmful because iron is a likely acceptor in InP. Properly galvanized steel sheet has a lifetime of over 30 years.

A clean Zn surface on galvanized steel may be obtained by chemically etching, as shown diagrammatically in apparatus 71 in FIG. 6, for instance with dilute hydrochloric acid. Subsequently, the sheet is rinsed with distilled water, and finally is dried in a stream of hot inert gas. This is the second state of apparatus 71.

A 1 to 10 μm thick film 51 with a net acceptor density of $\sim 1 \times 10^{15}$ to $\sim 1 \times 10^{16}$ cm⁻³ will be required. Evaporation of the compound, possibly with addition of excess phosphorus, or a p-type dopant, may be the most simple and inexpensive method. Phosphorus or a p-type dopant may have to be added to ensure a p-type film. Flash evaporation, where small quantities of the compound are successively evaporated, may be the method of choice to avoid preferential volatilization of phosphorus from the source container. Some research has been done on chemical vapour deposition (CVD) of InP, using indium and phosphorus trichloride, or triethyl indium and phosphine, as the source compounds. CVD may be another way to deposit InP films. Also, InP films can be produced by evaporation of In and of P from separate source containers.

While CdS films 53 can also be grown by CVD, virtually all work on CdS films for CdS/Cu₂S solar cells has involved evaporation of the compound. Useful net donor concentrations have been achieved in the range from $\sim 1 \times 10^{15}$ to $\sim 1 \times 10^{18}$ cm⁻³. Required film thickness is about 10 μm. This procedure occurs in the fourth stage of process apparatus 71.

Contacts 56 to the CdS are best applied by evaporation of metallic, e.g., chromium, films through shadow masks. This stage is the last in the vacuum or protective gas portion, in apparatus 71, in FIG. 7.

An adhesive 57 for the cell cover 58 may be a synthetic resin with a 30-year lifetime. It must be transparent to light between 500 and 1000 nm wavelength. It may be applied by roller 72.

The cell cover will probably be made of a thin glass cover sheet 58, sheet 68 in FIG. 6 (e.g., ~ 5 μm thick and of material commercially available under the Trade Mark Pyrex 7740) which is transparent between 500 and 1000 μm and impermeable to corroding agents.

This cover may be coated with an antireflection film 59, by any conventional technique, which is not shown in FIG. 6, but could be applied at or near roller 73.

Except for indium, all materials in the solar cell are readily available. Because of its limited use (low melting solders, low friction bearings, semiconductors), the production capacity for indium is only ~ 100 tons/year. However, indium is more abundant than silver whose annual production is $\sim 10,000$ tons. Most of the indium is obtained as a by-product of zinc from ore mines in the United States, Canada and Peru. The principal impurity in In is Zn. It may not be necessary to refine In to semiconductor purity because Zn is desirable acceptor impurity in InP. The price of indium is given as \$0.05 to \$0.15 per gram. With a $2.5\mu\text{m}$ thick InP film in a 5% efficient solar cell the investment in In is 5 cents per average watt, assuming 5¢/g of In. One ton of In is required for a power output of one average megawatt.

Photovoltaic cells have been made to show efficiencies of up to 14 percent for overall solar power conversion, or nearly 70 percent quantum efficiency over the band of wavelengths between 550 nm and 910 nm. This high efficiency is due in part to the empirical discovery that there are no undesirable interface states between the (111) InP and the (0001) CdS layers.

It will be appreciated that the p-InP/n-CdS cell described herein can be used generally as a radiant energy conversion cell, it is a particularly promising candidate for use in a low cost solar panel for the following reasons:

InP has a room temperature direct band gap of 1.34 eV. This is in the regime for optimum solar power conversion.

CdS transmits most of the solar radiation because of its 2.42 eV gap (at 300K).

A small gap p-type and a large gap n-type semiconductor form the best *a priori* combination for avoiding an interfacial "spike" in the conduction band. This spike would drastically reduce the short circuit photocurrent and thus the solar efficiency.

A further feature of the invention is that the lattice match between InP and CdS is excellent and guarantees lattice continuity across the junction plane. The lattice parameter of zinc blende InP is $a_0 = 5.869 \text{ \AA}$, the corresponding parameter of wurtzite CdS, $a_w/\sqrt{2} = 5.85 \text{ \AA}$, i.e., the lattice mismatch is 0.32%. The interatomic distances calculated from Phillip's tetrahedral radii are, In-P = $2.533 \text{ \AA}$, Cd-S = $2.532 \text{ \AA}$ (0.04%).

While single-crystal diodes have been made so far, the device shows considerable long-term promise for continuous-process polycrystalline thin-film fabrication employing zincated copper or steel sheet under the InP and a simple contact structure and protective

covers, such as glass, over the heterojunction. It should be cost-reducible in mass production.

In addition, p-InP/n-CdS heterodiode solar cells and photovoltaic detectors have been made with uniform quantum (conversion) efficiency of $\sim 70\%$ between $\sim 550 \text{ nm}$ and $\sim 910 \text{ nm}$. The diodes have $\sim 8.5\%$ solar energy conversion efficiency with considerable potential for improvement. Forward biased diodes luminesce in the infrared.

A process will now be described for increasing the efficiency of our heterojunction InP/CdS solar cells to 14 percent. This process also increased the efficiency of inadvertently inferior cells also to 14 percent. This latter unexpected advantage obviously increases the yield in the production of solar cells and thereby reduces costs. The effectiveness of this process may be of greatest value in future production of thin-film InP/CdS solar cells by increasing the efficiency of continuous sections of solar panel sheet to a uniformly high value.

Briefly, in one successful experiment, the process involves annealing an InP/CdS solar cell in "forming gas" ($15\% \text{ H}_2 + 85\% \text{ N}_2$) for 15 minutes at 600 degrees centigrade. This temperature is near optimum since lower temperatures are somewhat less effective, and temperatures of 650 degrees centigrade or more catastrophically destroy the cells. Forming gas ($\text{H}_2 + \text{N}_2$) or a variant thereof, is preferred since annealing in air at these temperatures severely degrades the cell's performance. Some slightly lower temperatures and correspondingly longer annealing times should be as effective to increasing the efficiency, although less convenient. Nevertheless, for temperatures from 550 degrees centigrade to 600 degrees centigrade, a 15 minute anneal is approximately sufficient to gain most of the improvement obtainable.

The efficiency of a given InP/CdS cell is directly related to its particular current-voltage characteristic as measured in the dark. Departures of the current density versus voltage curves from an ideal shape can be attributed to impurities and defects at the interface between the CdS and the InP. Such defects and associated excess current in the heterojunction region could probably be eliminated by more sophisticated growth procedures in which either the InP substrate was vapour etched or an InP layer (n-type) was deposited, *in situ* just prior to the CdS growth; but such procedures may be disadvantageous for large scale commercial use. Clearly, these is a variability to the previously measured departures from the ideal; but it has been found that all such departures can be greatly reduced by the following processing.

The annealing step is performed as follows.

Referring to FIG. 7 of the drawings, the heterojunction device 11-13 is placed in an annealing oven 74, which includes the air-

(13) (12)

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tight chamber 75, heating coil 76, power supply 77, temperature sensor 78, temperature scheduler 79, and comparator and negative feedback controller 80, acting on power supply 77, all of conventional type. To an input port of oven 74, is connected the source 81, which supplies a controlled stream of slightly reducing and mainly inert gas, such as forming gas, which flows over and around the heterojunction device and out through the output port, which is connected to the atmosphere exhaust 82.

There is evidence that a slightly reducing atmosphere is desirable to the annealing process, because preliminary tests of annealing in air (an oxidizing atmosphere) showed marked increases in CdS resistivity. Such CdS resistivities would lead to excessive internal power dissipation in the solar cells.

Fortunately such an effect is not observed when the cell is annealed in forming gas as shown in the curves of FIG. 8.

Various runs involved different annealing temperatures, shown in degrees C along the abscissa. Individual ordinates are shown for each curve, 83, 84 and 85 with appropriate units for open-circuit voltage V_{oc} , acceptor concentration N_a in the InP, and CdS resistivity, ρ respectively. Although the shape of the curve 85 depicting CdS resistivity ρ is quite complicated, for all annealing temperatures $\leq 600^\circ\text{C}$, the resistivity lies in the interval $0.02 < \rho < 0.10$ ohm-cm and thus lies in the range required for high performance. It can also be seen in FIG. 8, in curve 83, that V_{oc} increases to 0.72 eV subsequent to the 600°C anneal. This open circuit voltage is considerably larger than the best value obtained previously and leads to a calculated solar efficiency of 14 percent for a SiO_2 coated cell. A subsequent anneal at 650°C catastrophically destroyed this cell.

Although a 600°C anneal leads to the maximum solar efficiency, slightly lower temperatures might ultimately prove wiser since at 600°C the metallurgical junction is modified. As is shown by the capacitance-voltage characteristic curve 92 as compared to curve 92, in FIG. 9, the metallurgical junction is essentially unchanged by 15 minute anneals at temperatures $\leq 550^\circ\text{C}$. The 600°C anneal causes a noticeable change in the junction capacitance, as shown by curve 93, and indicates the formation of a thin resistive layer at the interface.

It is also apparent from this work that InP/CdS solar cells will have quite long useful lifetimes. Although such lifetimes have yet to be measured, it is clear from the 15 minute anneals in an air ambient (not shown) that temperatures above 450°C are needed to deteriorate a cell's performance. Therefore, the lifetime will be quite long under operating conditions ($T \sim 50^\circ\text{C}$). Furthermore, should this oxidation of the CdS be the factor ultimately

limiting the useful lifetime, an oxygen-impervious encapsulation will lead to much longer lifetimes.

For temperatures below 550°C , it may be desirable to increase the annealing time beyond 15 minutes up to several hours. For temperatures from 600°C to 625°C , times as short as 10 minutes may be desirable. It should also be clear that the amount of hydrogen in the annealing atmosphere may not need to exceed the amount necessary to counteract any traces of oxygen in the nitrogen, in the walls of oven 51 and in the surface or near-surface regions of the heterojunction device. Other substantially inert or noble gases may be substituted for the nitrogen. Examples are helium, neon, argon, krypton and xenon.

If an improved ohmic contact for CdS layer 13 is substituted for the indium grid contact 16, annealing after otherwise-complete fabrication of the solar cell may become more desirable. One such alternative contact is a layer of chromium.

WHAT WE CLAIM IS:—

1. A light-responsive device comprising a p-type indium phosphide layer, a heterojunction-forming and light-transmissive window of n-type cadmium sulphide formed on the p-type layer, a light-transmissive electrode deposited on the cadmium sulphide window, and means for establishing conductive contact to a surface of the indium phosphide layer remote from the window.

2. A device as claimed in claim 1, wherein the means for establishing conductive contacts to the indium phosphide surface comprises a metallic alloy contact disposed on the indium phosphide layer, a silver paste contacting the metallic alloy and a conductive heat sink contacting the silver paste wherein the silver paste is intermediate the alloy and the heat-sink.

3. A solar cell device comprising a supporting electrode comprising a zinc-containing conducting metal, a solar-energy absorbing body of p-type indium phosphide disposed on the supporting electrode, a heterojunction-forming and solar-energy transmissive window of n-type cadmium sulphide deposited on the indium phosphide p-type body, a solar-energy-transmissive electrode deposited on the cadmium sulphide and a protective solar-energy-transmissive body over the cadmium sulphide and the transmissive electrode.

4. A device as claimed in any one of the preceding claims, wherein the cadmium sulphide layer is a polycrystalline layer forming a heterojunction with the p-type indium phosphide layer, the indium/phosphide layer being polycrystalline.

5. A device as claimed in claim 3, wherein the transmissive electrode is a contact grid disposed upon and making ohmic contact to the cadmium sulphide layer.

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tight chamber 75, heating coil 76, power supply 77, temperature sensor 78, temperature scheduler 79, and comparator and negative feedback controller 80, acting on power supply 77, all of conventional type. To an input port of oven 74, is connected the source 81, which supplies a controlled stream of slightly reducing and mainly inert gas, such as forming gas, which flows over and around the heterojunction device and out through the output port, which is connected to the atmosphere exhaust 82.

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It is also apparent from this work that InP/CdS solar cells will have quite long useful lifetimes. Although such lifetimes have yet to be measured, it is clear from the 15 minute anneals in an air ambient (not shown) that temperatures above 450°C are needed to deteriorate a cell's performance. Therefore, the lifetime will be quite long under operating conditions ($T \sim 50^\circ\text{C}$). Furthermore, should this oxidation of the CdS be the factor ultimately

limiting the useful lifetime, an oxygen-impermeable encapsulation will lead to much longer lifetimes.

For temperatures below 550°C , it may be desirable to increase the annealing time beyond 15 minutes up to several hours. For temperatures from 600°C to 625°C , times as short as 10 minutes may be desirable. It should also be clear that the amount of hydrogen in the annealing atmosphere may not need to exceed the amount necessary to counteract any traces of oxygen in the nitrogen, in the walls of oven 51 and in the surface or near-surface regions of the heterojunction device. Other substantially inert or noble gases may be substituted for the nitrogen. Examples are helium, neon, argon, krypton and xenon.

If an improved ohmic contact for CdS layer 13 is substituted for the indium grid contact 16, annealing after otherwise-complete fabrication of the solar cell may become more desirable. One such alternative contact is a layer of chromium.

WHAT WE CLAIM IS:—

1. A light-responsive device comprising a p-type indium phosphide layer, a heterojunction-forming and light-transmissive window of n-type cadmium sulphide formed on the p-type layer, a light-transmissive electrode deposited on the cadmium sulphide window, and means for establishing conductive contact to a surface of the indium phosphide layer remote from the window.

2. A device as claimed in claim 1, wherein the means for establishing conductive contacts to the indium phosphide surface comprises a metallic alloy contact disposed on the indium phosphide layer, a silver paste contacting the metallic alloy and a conductive heat sink contacting the silver paste wherein the silver paste is intermediate the alloy and the heat-sink.

3. A solar cell device comprising a supporting electrode comprising a zinc-containing conducting metal, a solar-energy absorbing body of p-type indium phosphide disposed on the supporting electrode, a heterojunction-forming and solar-energy transmissive window of n-type cadmium sulphide deposited on the indium phosphide p-type body, a solar-energy-transmissive electrode deposited on the cadmium sulphide and a protective solar-energy-transmissive body over the cadmium sulphide and the transmissive electrode.

4. A device as claimed in any one of the preceding claims, wherein the cadmium sulphide layer is a polycrystalline layer forming a heterojunction with the p-type indium phosphide layer, the indium/phosphide layer being polycrystalline.

5. A device as claimed in claim 3, wherein the transmissive electrode is a contact grid disposed upon and making ohmic contact to the cadmium sulphide layer.

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6. A device as claimed in claim 3, wherein the protective transmissive body comprises a film of an adhesive, a transparent glass cover sheet and an antireflection coating.

7. A device as claimed in claim 3, wherein the supporting electrode is a galvanized sheet of steel.

10 8. A method of making a light-responsive device comprising forming a layer of n-type cadmium sulphide on a p-type layer of indium phosphide, the cadmium sulphide layer being light transmissive, thus forming a hetero-junction between the layers, depositing a light-transmissive electrode on the cadmium sulphide layer, establishing a conductive contact to a surface of the indium phosphide layer and annealing the device at a temperature of from 400°C to 625°C.

20 9. A method as claimed in claim 8, wherein the temperature is from 550°C to 600°C.

10. A method as claimed in claim 9, wherein the device is annealed for 15 minutes.

11. A method as claimed in claim 8, 9 or

10, wherein the device is annealed in an atmosphere consisting essentially of substantially inert gas and hydrogen. 25

12. A method as claimed in claim 11, wherein the substantially inert gas is nitrogen.

13. A method as claimed in claim 12, wherein the composition of the atmosphere is 15% hydrogen and 85% nitrogen. 30

14. A method of making a light-responsive device substantially as hereinbefore described with reference to and illustrated in FIGS. 7—9 of the accompanying drawings. 35

15. A light-responsive device substantially as hereinbefore described with reference to and illustrated in FIGS. 1—6 and 7—9 of the accompanying drawings.

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