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METHOD FOR FABRICATING A SMALL DIMENSIONAL GATE WITH ELEVATED SOURCE/DRAIN STRUCTURES

Abstract

A method of manufacturing a transistor with a small self aligned gate and self aligned elevated source/drain regions. A first insulating layer is formed over a substrate. A first opening is formed in the first insulating layer to expose the substrate. We form a gate dielectric layer over the substrate in the first opening. Next, first spacers are formed on the sidewalls of the first insulating layer. A gate layer is formed over the first insulating layer, the first spacers, and the gate dielectric layer. We planarize the gate layer to form a gate electrode. The first spacers are removed to form LDD openings. Next, we form lightly doped source/drain regions in the substrate in the LDD openings. Subsequently, second spacers are formed on the sidewalls of the first insulating layer and on the sidewalls of the gate electrode to form S/D openings. Source/drain regions are formed in the substrate in the S/D openings. Next, we form a conductive layer over the substrate at least partially filling the S/D openings. The conductive layer is planarized to form elevated source/drain structures.

FIGURE 3

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