ABSTRACT

BONDED SOI WAFER WITH <100> DEVICE LAYER AND <110) SUBSTRATE FOR PERFORMANCE IMPROVEMENT

A new silicon structure is provided. Under a first embodiment of the invention, a first silicon substrate having a ‹100› crystallographic orientation is bonded to the surface of a second silicon substrate having a ‹110› crystallographic orientation, the wafer alignment notch of the first and the second silicon substrates are aligned with each other. Under a first embodiment of the invention, a first silicon substrate having a ‹100› crystallographic orientation is bonded to the surface of a second silicon substrate having a ‹110› crystallographic orientation, the wafer alignment notch of the first and the second silicon substrates are not aligned with each other.

Figure 2

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