HYDROFLUOROCARBON COMPOUNDS AND THEIR USE IN INTEGRATED CIRCUIT MANUFACTURING PROCESSES

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Application No. 63/568,638, filed March 22, 2024, which is hereby incorporated in its entirety.

TECHNICAL FIELD

[0002] This disclosure generally describes 1,2,2-trifluoro-2-(trifluoromethoxy)ethene and its use in integrated circuit manufacturing processes, as well as analogs of 1,2,2-trifluoro-2-(trifluoromethoxy)ethene, and the use of these analogs in integrated circuit manufacturing processes too.

BACKGROUND

[0003] Lateral, two-dimensional, geometries of integrated circuit devices continue to decrease in size, and as such, the surface density of these devices continues to increase. With this increased density, the chance of electrical interference, including cross-talk and parasitic capacitance, between adjacent devices increases, thereby leading to decreased overall integrated circuit performance. To reduce the likelihood of this electrical interference, films of low dielectric constant ("low-k") insulating materials are often placed in the gaps, trenches, vias, and other surface features, between adjacent devices.

[0004] Nevertheless, the placement of low-k insulating materials in the gaps, trenches, and vias, of laterally laid out integrated circuit devices has its limitations too. More specifically, the ability of such low-k insulating materials to eliminate, or reduce, the electrical interference described above may decrease as the distance between adjacent devices is lessened and thus the thickness of the low-k insulating material film between adjacent devices decreases too. Accordingly, manufacturers

have begun looking at forming integrated circuit devices not only laterally in two-dimensions, but "vertically" in the third dimension simultaneously too.

[0005] As circuitry is laid out in an increasingly vertical orientation, the number of layers of alternating thin films of integrated circuit materials has increased. For example, three-dimensional NOT AND ("3D NAND") flash memory devices have gone from 24-layer "stacks" of alternating thin films of integrated circuit materials, to 32-layer stacks, and even to 48-layer stacks of such alternating thin films. More recently, work has begun directed to forming 3D NAND flash memory devices incorporating 96-layer, and 128-layer, stacks of these alternating thin film integrated circuit materials.

[0006] To retain the advantage of moving to three-dimensional vertically laid out circuits, integrated circuit manufacturers require new processes and corresponding materials. One such process, and corresponding set of materials, under review by integrated circuit manufacturers includes the formation of "channels" in 3D NAND flash memory devices. Per the art, a channel is a more or less cylindrical conduit that extends between the bottommost surface of the bottom-layer of alternating thin films of integrated circuit materials in the 3D NAND stack described above, and the opposing outermost surface of the topmost layer of the top-layer of the same stack of alternating thin films integrated circuit materials. Being more or less cylindrical, the channel also has a diameter.

[0007] As the number of layers in the 3D NAND flash memory devices increases, so too does the aspect ratio of the channel. As this aspect ratio increases manufacturers often experience more defects during channel formation including "incomplete etch," "bowing," and "twisting." Incomplete etch occurs when such conduit fails to fully extend between the bottommost surface of the bottom-layer of alternating thin films of integrated circuit materials, and the opposing outermost surface of the topmost layer of the top-layer of the same stack alternating thin films integrated circuit materials. Bowing occurs when the diameter of the conduit is greater than the preferred diameter at some point along the channel, as etching occurs more laterally than vertically at such point. A twisting defect occurs when the channel retains the preferred diameter but extends more laterally than vertically along its preferred,

predetermined, path. These defects are to be avoided when etching channels in 3D flash memory devices.

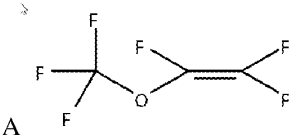
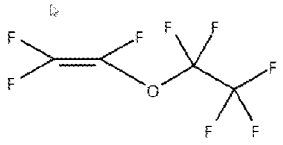
[0008] Besides these issues, 3D NAND flash memory device manufacturers are also focusing on utilizing etching compounds having lower global warming potential than more highly fluorinated compounds. Octafluorocyclobutane, for example, is a perfluorocarbon compound that is a greenhouse gas, and has a global warming potential approximately 3200 times greater than carbon dioxide. Octafluorocyclobutane is also a hydrofluorocarbon that may be used to etch the above-described channels. As such, integrated circuit manufacturers are looking for alternative hydrofluorocarbon compounds and mixtures having lower global warming potential than perfluorocarbon compounds, and that also help minimize above-described incomplete etch, bowing, and twisting defects during the etching of channels in 3D NAND flash memory devices.

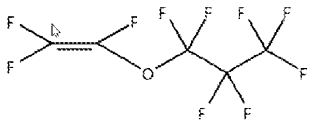
[0009] The present disclosure is directed to overcoming on or more problems set forth above, and/or other problems associated with the prior art.

SUMMARY OF THE INVENTION

[0010] In accordance with a first aspect of the present application, a mixture configured to etch a thin film of an integrated circuit material is disclosed. The mixture may comprise:

a first compound comprising one or more of:

A , B , and

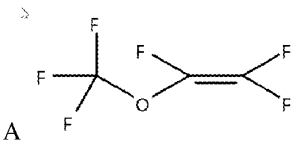
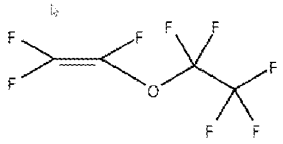


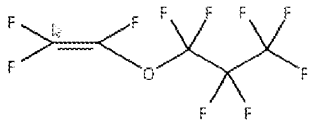
C ; and

a second compound comprising one or more of: oxygen, argon, helium, nitrogen, octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF4), methyl fluoride (CH_3F), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), 2,3,3,3-tetrafluoropro-1-ene (C3H2F4, 1234ze), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), or 1,1,3,3,3-pentafluoropropene (C_3HF_5).

[0011] In accordance with a second aspect of the present disclosure, a method of etching a thin film of an integrated circuit material is disclosed. The method may include the step of contacting a surface of the thin film of the integrated circuit material with a plasma comprising reactive ions generated by subjecting a mixture configured to etch the thin film of the integrated circuit material to a plasma generating device, thereby removing a portion of the thin film of the integrated circuit material. The mixture may comprise:

a first compound comprising one or more of:

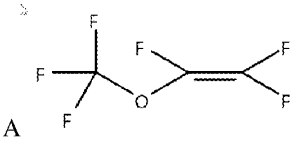
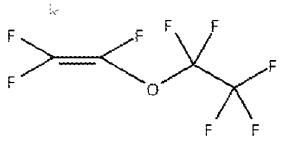
A  , B  , and

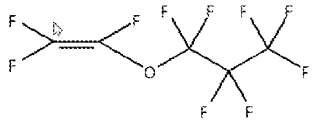


C ; and

a second compound comprising one or more of: oxygen, argon, helium, nitrogen, octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF4), methyl fluoride (CH_3F), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), or 1,1,3,3,3-pentafluoropropene (C_3HF_5).

[0012] Lastly, in accordance with a third aspect of the present disclosure, a method of patterning a thin film of an integrated circuit material is disclosed. The method may include the step of contacting a surface of the thin film with a plasma comprising reactive ions generated by subjecting a mixture configured to etch the thin film of the integrated circuit material to a plasma generating device, thereby removing a portion of the thin film and generating a pattern in the thin film of the integrated circuit material. In this method, at least a portion of the thin film is disposed between confronting surfaces of a substrate and a masking material layer, wherein the masking material layer comprises an aperture defined therein exposing a portion of the surface of the thin film. In this method, the mixture may comprise a first compound comprising one or more of:

A , B , and



C ; and

a second compound comprising one or more of: oxygen, argon, helium, nitrogen, octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF_4), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), or 1,1,3,3,3-pentafluoropropene (C_3HF_5), nitrogen trifluoride (NF_3), and sulfur hexafluoride (SF_6).

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is a side elevation view of a multi-layer stack of alternating thin films of integrated circuit materials in a 3D NAND flash memory device depicting: (1) defect free channels etched through the stack; (2) examples of bowing and twisting in channels extending through the stack; and (3) an example of an incomplete etch that fails to extend through the stack.

[0014] FIG. 2 is a flowchart depicting a method configured to etch a thin film of an integrated circuit material with the compounds and mixtures disclosed herein.

[0015] FIG. 3 is a cross-sectional diagram of a wafer that may be utilized in the method configured to etch a thin film of an integrated circuit material depicted in FIG. 2.

[0016] FIG. 4 is a flowchart depicting a method configured to pattern a thin film of an integrated circuit material with the compounds and mixtures disclosed herein.

[0017] FIG. 5A is cross-sectional diagram of a wafer that may be utilized in the method configured to etch a thin film of an integrated circuit material depicted in FIG. 4 before patterning occurs.

[0018] FIG. 5B is a cross-sectional diagram of a wafer that may be utilized in the method configured to etch a thin film of an integrated circuit material depicted in FIG. 4 during the patterning process.

[0019] FIG. 5C is a cross-sectional diagram of a wafer that may be utilized in the method configured to etch a thin film of an integrated circuit material depicted in FIG. 4 depicting a pattern generated in the thin film of integrated circuit material.

[0020] FIGS. 6A-D are cross-sectional SEM images of trenches etched by using an octafluorocyclobutane (C_4F_8) mixture in comparison to trenches etched utilizing a mixture comprising compound A disclosed herein under three different process conditions.

[0021] FIGS. 7A-D are cross-sectional SEM images of trenches etched by using an octafluorocyclobutane (C_4F_8) mixture in comparison to trenches etched utilizing a mixture using compound B disclosed herein under three different process conditions.

[0022] FIGS. 8A-D are cross-sectional SEM images of trenches etched by using an octafluorocyclobutane (C_4F_8) mixture in comparison to trenches etched utilizing a mixture using compound C disclosed herein under three different process conditions.

DETAILED DESCRIPTION

[0023] Example embodiments will be described more fully with reference to the accompanying drawings. Example embodiments are provided so that this disclosure will be thorough, and will fully convey the scope to those who are skilled in the art. Numerous specific details are set forth such as examples of specific compositions, components, devices, and methods, to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to those skilled in the art that specific details need not be employed, that example embodiments may be embodied in many different forms and that neither should be construed to limit the scope of the disclosure. In some example embodiments, well-known processes, well-known device structures, and well-known technologies are not described in detail.

[0024] The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting. As used herein, the singular forms "a," "an," and "the" may be intended to include the plural forms as well, unless the context clearly indicates otherwise. The terms "comprises," "comprising," "including," and "having," are inclusive and therefore specify the presence of stated features, elements, compositions, steps, integers, operations, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. Although the open-ended term "comprising," is to be understood as a non-restrictive term used to describe and claim various embodiments set forth herein, in certain aspects, the term may alternatively be understood to instead be a more limiting and restrictive term, such as "consisting of" or "consisting essentially of." Thus, for any given embodiment reciting compositions, materials, components, elements, features, integers, operations, and/or process steps, the present disclosure also specifically includes embodiments consisting of, or consisting essentially of, such recited compositions, materials, components, elements, features, integers, operations, and/or

process steps. In the case of "consisting of," the alternative embodiment excludes any additional compositions, materials, components, elements, features, integers, operations, and/or process steps, while in the case of "consisting essentially of," any additional compositions, materials, components, elements, features, integers, operations, and/or process steps that materially affect the basic and novel characteristics are excluded from such an embodiment, but any compositions, materials, components, elements, features, integers, operations, and/or process steps that do not materially affect the basic and novel characteristics can be included in the embodiment.

[0025] Any method steps, processes, and operations described herein are not to be construed as necessarily requiring their performance in the particular order discussed or illustrated, unless specifically identified as an order of performance. It is also to be understood that additional or alternative steps may be employed, unless otherwise indicated.

[0026] When a component, element, or layer is referred to as being "on," "engaged to," "connected to," or "coupled to" another element or layer, it may be directly on, engaged, connected, or coupled to the other component, element, or layer, or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly engaged to," "directly connected to," or "directly coupled to" another element or layer, there may be no intervening elements or layers present. Other words used to describe the relationship between elements should be interpreted in a like fashion (*e.g.,* "between" versus "directly between," "adjacent" versus "directly adjacent," etc.). As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0027] Although the terms first, second, third, etc. may be used herein to describe various steps, elements, components, regions, layers and/or sections, these steps, elements, components, regions, layers and/or sections should not be limited by these terms, unless otherwise indicated. These terms may be only used to distinguish one step, element, component, region, layer or section from another step, element, component, region, layer, or section. Terms such as "first," "second," and other numerical terms when used herein do not imply a sequence or order unless clearly indicated by the context. Thus, a first step, element, component, region, layer, or

section discussed below could be termed a second step, element, component, region, layer, or section without departing from the teachings of the example embodiments.

[0028] Spatially or temporally relative terms, such as "before," "after," "inner," "outer," "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. Spatially or temporally relative terms may be intended to encompass different orientations of the device or system in use or operation in addition to the orientation depicted in the figures.

[0029] Throughout this disclosure, the numerical values represent approximate measures or limits to ranges to encompass minor deviations from the given values and embodiments having about the value mentioned as well as those having exactly the value mentioned. Other than in the working examples provided at the end of the detailed description, all numerical values of parameters (*e.g.,* of quantities or conditions) in this specification, including the appended claims, are to be understood as being modified in all instances by the term "about" whether or not "about" actually appears before the numerical value. "About" indicates that the stated numerical value allows some slight imprecision (with some approach to exactness in the value; approximately or reasonably close to the value; nearly). If the imprecision provided by "about" is not otherwise understood in the art with this ordinary meaning, then "about" as used herein indicates at least variations that may arise from ordinary methods of measuring and using such parameters. For example, "about" may comprise a variation of less than or equal to 5%, optionally less than or equal to 4%, optionally less than or equal to 3%, optionally less than or equal to 2%, optionally less than or equal to 1%, optionally less than or equal to 0.5%, and in certain aspects, optionally less than or equal to 0.1%.

[0030] In addition, disclosure of ranges includes disclosure of all values and further divided ranges within the entire range, including endpoints and sub-ranges given for the ranges. Thus, ranges are, unless specified otherwise, inclusive of endpoints and include disclosure of all distinct values and further divided ranges within the entire range. Disclosure of values and ranges of values for specific parameters (such as temperatures, molecular weights, weight percentages, etc.) are not exclusive of other values and ranges of values useful herein. It is envisioned that two or more specific exemplified values for a given parameter may define endpoints for a range of values

that may be claimed for the parameter. For example, if Parameter X is exemplified herein to have value A and also exemplified to have value Z, it is envisioned that Parameter X may have a range of values from about A to about Z. Similarly, it is envisioned that disclosure of two or more ranges of values for a parameter (whether such ranges are nested, overlapping, or distinct) subsume all possible combination of ranges for the value that might be claimed using endpoints of the disclosed ranges. For example, if Parameter X is exemplified herein to have values in the range of 1–10, or 2–9, or 3–8, it is also envisioned that Parameter X may have other ranges of values including 1–9, 1–8, 1–3, 1–2, 2–10, 2–8, 2–3, 3–10, and 3–9.

[0031] As used herein, the terms "composition" and "material" are used interchangeably to refer broadly to a substance containing at least the preferred chemical constituents, elements, or compounds, but which may also comprise additional elements, compounds, or substances, including trace amounts of impurities, unless otherwise indicated.

[0032] Various aspects of the disclosure will now be described with reference to the drawings and tables disclosed herein, if applicable, with like reference numbers referring to like elements, unless specified otherwise. As described above, to retain the advantage of moving to three-dimensional vertically laid out circuitry, integrated circuit manufacturers require new processes and corresponding materials. One such process under review is the formation of channels during the creation of 3D flash memory devices having minimal formation of defects such as incomplete etch, bowing, and twisting. Turning now to FIG. 1, a side elevation view of a multi-layer stack **10** of alternating thin films of integrated circuit materials **12** utilized in a 3D flash memory device is depicted. As represented there, a channel **14** can extend between the bottommost surface **16** of the bottom-layer **18** of the alternating thin films of integrated circuit materials **12** in the multi-layer stack **10**, and the opposing outermost surface **20** of the top-layer **22** of the alternating thin films of integrated circuit materials **12** in the multi-layer stack **10**. Without intending to be limiting, the alternating thin films of integrated circuit materials **12** in such stack **10** are often comprised of a layer of silicon nitride (i.e., Si_3N_4) followed by a layer of silicon dioxide (i.e., SiO_2).

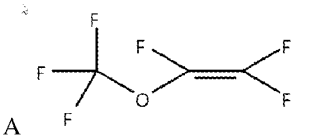
[0033] As is additionally shown in FIG.1, defects may occur during the creation of the channel **14** in 3D flash memory devices. One such defect is an incomplete etch

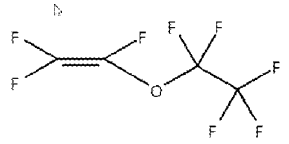
defect **24**. More specifically, and as is described above, the incomplete etch defect **24** occurs when the channel **14** fails to fully extend between the bottommost surface **16** of the bottom-layer **18** of the alternating thin films of integrated circuit materials **12** in the multi-layer stack **10**, and the opposing topmost surface **20** of the top-layer **22** of the alternating thin films of integrated circuit materials **12** in the multi-layer stack **10**. Another defect integrated circuit manufacturers may experience during the creation of the channel **14** in 3D flash memory devices includes a bowing defect **26**.

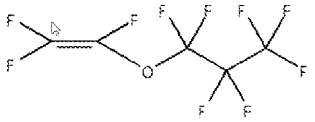
[0034] As represented in FIG. 1, the bowing defect **26** occurs when the diameter of the channel **14** is greater than the preferred, predetermined, diameter of the channel **14** at some point along the channel **14** extending between the bottommost surface **16** of the bottom-layer **18** of the alternating thin films of integrated circuit materials **12** in the multi-layer stack **10**, and the opposing outermost surface **20** of the top-layer **22** of the alternating thin films of integrated circuit materials **12** in the multi-layer stack **10**. The thickness of the of each layer of the alternating thin films of integrated circuit materials **12** in the multi-layer stack **10** may be as little as a single nanometer, and possibly may be two, three, four, five, or more, microns in thickness.

[0035] Finally, another defect that may occur in the formation of the channel **14** in 3D flash memory devices is a twisting defect **28**. As seen in FIG. 1, the twisting defect **28** occurs when the channel **14** retains the preferred diameter, but at least some portion of the channel **14** extends more laterally, than vertically, relative to its preferred path **30**. As was also described above, manufacturers are simultaneously looking to utilize hydrofluorocarbon compounds having lower global warming potential than more traditionally utilized perfluorocarbon compounds, such as octafluorocyclobutane, during the etching of such channels **14**.

[0036] In a first aspect of the invention disclosed herein, novel and non-obvious mixtures configured to have lower global warming potential, which may be used for etching thin films, such as thin films of integrated circuit materials **12** in the multi-layer stack **10**, are provided herein. More specifically, such mixtures may comprise at least one first compound comprising a compound corresponding in structure to:

A  ;

B  ; and

C  .

[0037] Such mixture configured to etch a thin film of an integrated circuit material additionally include at least one second compound besides compounds A, B and C, listed above. More clearly, such mixture includes at least one second compound comprising oxygen (O_2), argon (Ar), octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF_4), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), 1,1,3,3,3-pentafluoropropene (C_3HF_5), sulfur hexafluoride (SF_6), and nitrogen trifluoride (NF_3). These second compounds, like the first compounds described above may also function as materials that contribute to etching thin films as described herein.

[0038] Besides the first and second compounds described above, such mixtures often include at least one third compound comprising oxygen, argon, helium, xenon, krypton, and nitrogen. Oxygen is customarily used as a material that limits the creation of fluoropolymers generated when reactive ions of the first and second compounds described and depicted above recombine a polymer at some point along the channel **14** of the alternating thin films of integrated circuit materials **12** in the multi-layer stack **10**. Such buildup of fluoropolymer at the bottom of the channel **14** may help lead to the incomplete etch defect **24** described above. Alternatively, such

buildup of fluoropolymer at differing points along the channel **14** may also help lead to the formation of the bowing defect **26** as well as the twisting defect **28**.

[0039] As described before, the at least one third compound may also be selected from argon, helium, xenon, krypton, and nitrogen. Such compounds often act as carrier gases for the etching process, and more importantly act to help transfer energy to, and ionize, the first compounds and second compounds described before.

[0040] In a preferred embodiment of this aspect of the disclosure, the at least one first compound comprises greater than, or equal to, about 1% by volume of this mixture, and less than or equal to about 99% by volume of the mixture. In a more preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 90% by volume of the mixture. In a further preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 80% by volume of the mixture. In a further preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 70% by volume of the mixture. In another preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 60% by volume of the mixture. In an additional preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 50% by volume of the mixture.

[0041] The at least one second compound, and the at least one third compound, make up the balance of the % volumes described just above. More specifically, when the at least one first compound ranges between 1% and 99% of the volume of the mixture, then the at least one second compound alone, or together with the at least one third compound, ranges between 99% and 1% by volume of the mixture. In the instance that the least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 80% by volume of the mixture, then the at least one second compound alone, or together with the at least one third compound, ranges between 90% and 20% by volume of the mixture. Additionally, in another example, in the instance that the least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about

50% by volume of the mixture, then the at least one second compound alone, or together with the at least one third compound, ranges between 90% and 50% by volume of the mixture. Generally, the ratio of the first compound to the second compound between 5:1 and 1:5 in this mixture.

[0042] As described before, the mixtures described in this first aspect of the present disclosure are configured to etch thin films of integrated circuit materials. In many instances, this thin film of integrated circuit material includes silicon, silicon oxide, silicon dioxide, silicon carbide, silicon nitride, silicon carbonitride, silicon oxycarbonitride, silicon oxycarbide, silicon oxycarbonitride, or where appropriate, combinations thereof. However, the mixtures described in this first aspect of the present disclosure may also find usefulness in etching other thin film materials including, but not necessarily limited to, gallium nitride, aluminum gallium nitride, gallium arsenide, aluminum gallium arsenide, indium phosphide, indium aluminum arsenide, indium gallium arsenide, silicon germanium, silicon hydrogen bromide, zinc selenide, indium tin oxide, lead zirconium titanate, molybdenum, poly-silicon, photoresist, carbon hard mask, and combinations thereof, too.

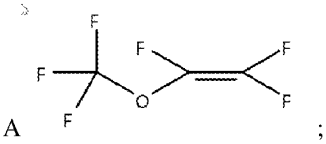
[0043] In operation, the compounds and mixtures depicted and described above find usefulness in many integrated circuit manufacturing processes including, but not limited to, etching a thin film, for example, a thin film of an integrated circuit material circuit material **12** in the multi-layer stack **10** depicted in FIG. 1,in a plasma-enhanced etching process. Accordingly in a second aspect of the present disclosure, and as represented in FIG. 2, a flowchart depicting a method configured to etch a thin film of an integrated circuit material with the compounds and mixtures disclosed herein is disclosed. As seen in a step **110**, a wafer comprising a thin film of an integrated circuit material disposed thereon may be positioned inside a plasma-enhanced etching tool reaction chamber.

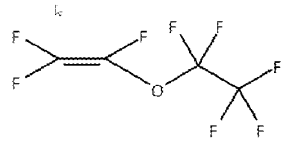
[0044] Turning now to FIG. 3, a cross-sectional diagram of an exemplary wafer **210** that may be utilized in step **110**, as well as any remaining steps of the process depicted in FIG. 2, is disclosed. As seen therein, the wafer may be comprised of a substrate **212** having a thin film of an integrated circuit material **214** disposed thereon. The substrate **212** comprises one of either silicon (e.g.., monocrystalline silicon) or poly-silicon. In many instances the thin film of integrated circuit material **214**

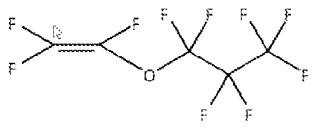
comprises silicon oxide, silicon dioxide, silicon carbide, silicon nitride, silicon carbonitride, silicon oxycarbonitride, silicon oxycarbide, silicon oxycarbonitride, and where appropriate, combinations thereof. In most instances the thin film of integrated circuit material **214** will either be one of silicon dioxide or silicon nitride.

[0045] Additionally, or alternatively, the thin film of integrated circuit material **214** disposed on the wafer **210** may also include gallium nitride, aluminum gallium nitride, gallium arsenide, aluminum gallium arsenide, indium phosphide, indium aluminum arsenide, indium gallium arsenide, silicon germanium, silicon hydrogen bromide, zinc selenide, indium tin oxide, lead zirconium titanate, molybdenum, poly-silicon, photoresist, carbon hard mask, and combinations thereof, too. Additionally, the thin film of integrated circuit material **214** comprises a surface **216** that may be contacted with a plasma comprising reactive ions of the mixture that is configured to etch the thin film of integrated circuit material **214**. Although not shown in FIG. 3, it is contemplated herein that the wafer may include more than one thin film of integrated circuit material, for example, alternating thin films of the same and/or different material as described herein, disposed on a substate.

[0046] Now turning back to FIG. 2, and while still reviewing FIG. 3, in step **112** a mixture configured to etch the thin film of integrated circuit material **214** may be flowed into the plasma-enhanced etching tool chamber. Such mixtures may comprise at least one first compound comprising a compound corresponding in structure to:

A  ;

B  ; and

C  .

[0047] Such mixture configured to etch a thin film of an integrated circuit material additionally include at least one second compound besides compounds A, B and C, listed above. More clearly, such mixture includes at least one second compound comprising oxygen (O_2), argon (Ar), octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF_4), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), 1,1,3,3,3-pentafluoropropene (C_3HF_5), sulfur hexafluoride (SF_6), and nitrogen trifluoride (NF_3). These second compounds, like the first compounds described above may also function as materials that contribute to etching thin films as described herein.

[0048] Besides the first and second compounds described above, such mixtures often include at least one third compound comprising oxygen, argon, helium, xenon, krypton, and nitrogen. Oxygen is customarily used as a material that limits the creation of fluoropolymers generated when reactive ions of the first and second compounds described and depicted above recombine a polymer at some point along the channel **14** of the alternating thin films of integrated circuit materials **12** in the multi-layer stack **10**. Such buildup of fluoropolymer at the bottom of the channel **14** may help lead to the incomplete etch defect **24** described above. Alternatively, such buildup of fluoropolymer at differing points along the channel **14** may also help lead to the formation of the bowing defect **26** as well as the twisting defect **28**.

[0049] As described before, the at least one third compound may also be selected from argon, helium, xenon, krypton, and nitrogen. Such compounds often act as carrier gases for the etching process, and more importantly act to help transfer energy to, and ionize, the first compounds and second compounds described before.

[0050] In a preferred embodiment of this aspect of the disclosure, the at least one first compound comprises greater than, or equal to, about 1% by volume of this mixture, and less than or equal to about 99% by volume of the mixture. In a more preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 90% by volume of the mixture. In a further preferred embodiment, the at least one first compound

comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 80% by volume of the mixture. In a further preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 70% by volume of the mixture. In another preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 60% by volume of the mixture. In an additional preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 50% by volume of the mixture.

[0051] The at least one second compound, and the at least one third compound, make up the balance of the % volumes described just above. More specifically, when the at least one first compound ranges between 1% and 99% of the volume of the mixture, then the at least one second compound alone, or together with the at least one third compound, ranges between 99% and 1% by volume of the mixture. In the instance that the least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 80% by volume of the mixture, then the at least one second compound alone, or together with the at least one third compound, ranges between 90% and 20% by volume of the mixture. Additionally, in another example, in the instance that the least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 50% by volume of the mixture, then the at least one second compound alone, or together with the at least one third compound, ranges between 90% and 50% by volume of the mixture. Generally, the ratio of the first compound to the second compound between 5:1 and 1:5 in this mixture.

[0052] As described before, the mixtures described in this first aspect of the present disclosure are configured to etch thin films of integrated circuit materials. In many instances, this thin film of integrated circuit material includes silicon, silicon oxide, silicon dioxide, silicon carbide, silicon nitride, silicon carbonitride, silicon oxycarbonitride, silicon oxycarbide, silicon oxycarbonitride, or where appropriate, combinations thereof. However, the mixtures described in this first aspect of the present disclosure may also find usefulness in etching other thin film materials including, but not necessarily limited to, gallium nitride, aluminum gallium nitride,

gallium arsenide, aluminum gallium arsenide, indium phosphide, indium aluminum arsenide, indium gallium arsenide, silicon germanium, silicon hydrogen bromide, zinc selenide, indium tin oxide, lead zirconium titanate, molybdenum, poly-silicon, photoresist, carbon hard mask, and combinations thereof, too.

[0053] While still reviewing FIG. 2, in view of FIG. 3, in step **114** a plasma generating device electronically coupled with the plasma-enhanced etching tool reaction chamber may be turned on, and thereby generate a plasma comprising reactive ions of the mixture configured to etch the thin film of integrated circuit material **214** inside the plasma-enhanced etching tool's reaction chamber. In step **116** depicted in FIG. 2, the surface **216** of FIG. 3 may be contacted with the plasma comprising reactive ions of the mixture configured to etch the thin film of integrated circuit material **214**, thereby removing a portion of that thin film **214** disposed on the wafer **210**.

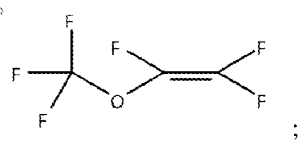
[0054] In accordance with a third aspect of the invention disclosed herein, a method of pattering a thin film of an integrated circuit material is disclosed. Turing now to FIG. 4, while also reviewing FIGS. 5A-5C, at step **310** a wafer **410** may be positioned inside a plasma-enhanced etching tool reaction chamber. As represented in each of FIGS. 5A-5C, the wafer **410** may be comprised of a substrate **420** having a thin film of an integrated circuit material **430** disposed thereon between opposing surfaces **440** of the substrate **420** and a masking material layer **450**.

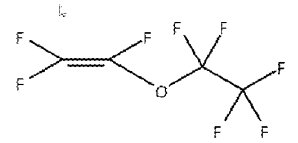
[0055] Substrate **420** comprises one of either silicon (e.g.., monocrystalline silicon) or poly-silicon. In many instances the thin film of integrated circuit material **430** comprises silicon oxide, silicon dioxide, silicon carbide, silicon nitride, silicon carbonitride, silicon oxycarbonitride, silicon oxycarbide, silicon oxycarbonitride, and where appropriate, combinations thereof. In most instances the thin film of integrated circuit material **430** will either be one of silicon dioxide or silicon nitride.

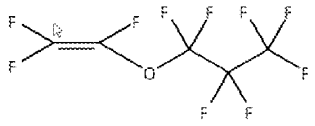
[0056] Additionally, or alternatively, the thin film of integrated circuit material **430** disposed between the opposing surfaces **440** comprises gallium nitride, aluminum gallium nitride, gallium arsenide, aluminum gallium arsenide, indium phosphide, indium aluminum arsenide, indium gallium arsenide, silicon germanium, silicon hydrogen bromide, zinc selenide, indium tin oxide, lead zirconium titanate, molybdenum, poly-silicon, and combinations thereof, too. In addition, the masking

material layer **450** may comprise carbon hard mask, a photoresist, a metal mask, and combinations thereof. Finally, and as is seen in FIG. 5A, the masking material layer **450** comprises one or more apertures **460** at least partially defined therethrough. In another instance, the one or more apertures **460** may be defined fully through the masking material layer **450**. As is understood by a person having ordinary skill in the art, the apertures **460** will define a pattern in the thin film of integrated circuit material **430** after etching.

[0057] Turning back to FIG. 4, and while still reviewing FIGS. 5A and 5B, in step **312** a mixture configured to etch the thin film of integrated circuit material **430** may be flowed into the plasma-enhanced etching tool chamber. Such mixture may comprise at least one first compound comprising a compound corresponding in structure to:

A  ;

B  ; and

C  .

[0058] Such mixture configured to etch a thin film of an integrated circuit material additionally include at least one second compound besides compounds A, B and C, listed above. More clearly, such mixture includes at least one second compound comprising oxygen (O_2), argon (Ar), octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF_4), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), hexafluoropropene (C_3F_6),

hexafluorocyclopropane (C_3F_6), 1,1,3,3,3-pentafluoropropene (C_3HF_5), sulfur hexafluoride (SF_6), and nitrogen trifluoride (NF_3). These second compounds, like the first compounds described above may also function as materials that contribute to etching thin films as described herein.

[0059] Besides the first and second compounds described above, such mixtures often include at least one third compound comprising oxygen, argon, helium, xenon, krypton, and nitrogen. Oxygen is customarily used as a material that limits the creation of fluoropolymers generated when reactive ions of the first and second compounds described and depicted above recombine a polymer at some point along the channel **14** of the alternating thin films of integrated circuit materials **12** in the multi-layer stack **10**. Such buildup of fluoropolymer at the bottom of the channel **14** may help lead to the incomplete etch defect **24** described above. Alternatively, such buildup of fluoropolymer at differing points along the channel **14** may also help lead to the formation of the bowing defect **26** as well as the twisting defect **28**.

[0060] As described before, the at least one third compound may also be selected from argon, helium, xenon, krypton, and nitrogen. Such compounds often act as carrier gases for the etching process, and more importantly act to help transfer energy to, and ionize, the first compounds and second compounds described before.

[0061] In a preferred embodiment of this aspect of the disclosure, the at least one first compound comprises greater than, or equal to, about 1% by volume of this mixture, and less than or equal to about 99% by volume of the mixture. In a more preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 90% by volume of the mixture. In a further preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 80% by volume of the mixture. In a further preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 70% by volume of the mixture. In another preferred embodiment, the at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 60% by volume of the mixture. In an additional preferred embodiment, the

at least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 50% by volume of the mixture.

[0062] The at least one second compound, and the at least one third compound, make up the balance of the % volumes described just above. More specifically, when the at least one first compound ranges between 1% and 99% of the volume of the mixture, then the at least one second compound alone, or together with the at least one third compound, ranges between 99% and 1% by volume of the mixture. In the instance that the least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 80% by volume of the mixture, then the at least one second compound alone, or together with the at least one third compound, ranges between 90% and 20% by volume of the mixture. Additionally, in another example, in the instance that the least one first compound comprises greater than, or equal to, about 10% by volume of this mixture, and less than or equal to about 50% by volume of the mixture, then the at least one second compound alone, or together with the at least one third compound, ranges between 90% and 50% by volume of the mixture. Generally, the ratio of the first compound to the second compound between 5:1 and 1:5 in this mixture.

[0063] As described before, the mixtures described in this first aspect of the present disclosure are configured to etch thin films of integrated circuit materials. In many instances, this thin film of integrated circuit material includes silicon, silicon oxide, silicon dioxide, silicon carbide, silicon nitride, silicon carbonitride, silicon oxycarbonitride, silicon oxycarbide, silicon oxycarbonitride, or where appropriate, combinations thereof. However, the mixtures described in this first aspect of the present disclosure may also find usefulness in etching other thin film materials including, but not necessarily limited to, gallium nitride, aluminum gallium nitride, gallium arsenide, aluminum gallium arsenide, indium phosphide, indium aluminum arsenide, indium gallium arsenide, silicon germanium, silicon hydrogen bromide, zinc selenide, indium tin oxide, lead zirconium titanate, molybdenum, poly-silicon, photoresist, carbon hard mask, and combinations thereof, too.

[0064] Moving on, in step **314** a plasma generating device electronically coupled with the plasma-enhanced etching tool reaction chamber may be turned on, and thereby generate a plasma comprising reactive ions of the mixture configured to etch the thin

film of integrated circuit material **430** inside the plasma-enhanced etching tool's reaction chamber. In step **316** depicted in FIG. 4, the one or more apertures **460** represented in FIGS. 5A and 5B may be contacted with the plasma comprising reactive ions of the mixture configured to etch the thin film of integrated circuit material **430**, thereby removing any remaining masking material layer **440** and thus fully defining the one or more apertures **460** through the entirety of the masking material layer **440** and thereby exposing a surface **470** of the thin film of integrated circuit material **430** consistent in shape and size to the aperture **460** from which it is associated.

[0065] In step **318**, as is represented in FIG. 4, the surface **470** of FIG. 5B may be contacted with the plasma comprising reactive ions of the mixture configured to etch the thin film of integrated circuit material **430**, thereby removing a portion of that thin film **430** disposed on the wafer **410**. As seen in FIG. 5C, the removal of this material **430** in step **318** generated a pattern **480** in the thin film of integrated circuit material **430**. As a person having ordinary skill in the dry etching arts understands, the pattern **480** generated in this process is consistent in shape and size with the aperture **460** from which it is coupled in the masking material layer **440**. Some common patterns **480** etched into the thin film of integrated circuit material **430** include gaps, trenches, vias that may subsequently be backfilled with a low-k material. Alternatively, the pattern **480** may comprise a channel **14** of a 3D flash memory device depicted above in FIG. 1.

[0066] Use of the mixtures described herein advantageously result in thin film etching and patterning with desirable selectivity. For example, where the thin film comprises silicon dioxide or silicon nitride, the mixture can have an etch selectivity for the thin film to the masking material layer (*e.g.*, metal mask, carbon hard mask, photoresist) of greater than or equal to about 1.

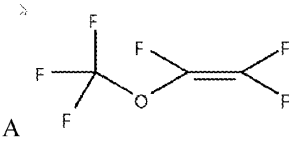
[0067] The foregoing description of the embodiments has been provided for purposes of illustration and description. It is not intended to be exhaustive or to limit the disclosure. Individual elements or features of a particular embodiment are generally not limited to that particular embodiment, but, where applicable, are interchangeable and can be used in a selected embodiment, even if not specifically shown or described. The same may also be varied in many ways. Such variations are not to be

regarded as a departure from the disclosure, and all such modifications are intended to be included within the scope of the disclosure.

Patterning Methods

[0068] All patterning tests were conducted with a PlasmaTherm APEX SLR ICP 200mm reaction chamber. The plasma generating device electronically coupled with the reaction chamber is an inductively coupled plasma generator having a 2 MHz top electrode source and a 13.56 MHz biased bottom electrode/susceptor. The top electrode power may be varied between 0 watts ("W") and about 2000 W, while the bottom electrode/susceptor power can be varied between 0 W and about 600 W. The temperature of the bottom electrode/susceptor may be varied between about -40°C and 250°C to evaluate the effect of reduced temperature on pattern formation. The pressure of the reaction chamber may be varied between about 1 mTorr and 100 mTorr, and the flow rate of the mixture configured to etch the tin films of integrated circuit material may be varied between 1 and 500 standard cubic centimeters per minute ("sccm"). Oxygen, argon or oxygen and argon. are typically flowed into the reaction chamber as part of the mixture configured to etch a thin film of an integrated circuit material, while up to three other gases may be simultaneously flowed into the reaction chamber along with oxygen and/or argon to help generate a pattern in a thin film of an integrated circuit material.

[0069] Working Example 1 – Use of Compound A to Generate a Trench:



A .

Based on a blanket wafer screening DOE several process conditions were selected for a patterned wafer etch and compared to octafluorocyclobutane (C_4F_8) Best Known Method ("BKM") conditions. BKM is a term of art. The below table shows C_4F_8 BKM conditions:

RF [W]	**Bias** [W]	**Press** [mtorr]	**O2** [sccm]	**Ar** [sccm]	**C4F8** [sccm]	**Etch Time** [min]
600	600	5	3	36	21	3

The table below shows three process conditions with Compound A run on patterned wafers:

Wafer	RF [W]	Bias [W]	Press [mtorr]	O2 [sccm]	Ar [sccm]	C3F6O [sccm]	Etch Time [min]
P1	600	600	4	3	20	35	3
P19	600	800	4	3	15	30	3
P20	600	800	4	3	25	40	3

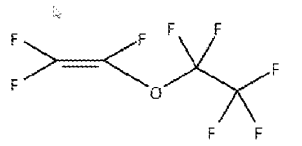
All patterned etches from the table above were carried out at a chamber temperature of 60°C and an electrode temperature of 25°. The table below shows an etch profile comparison of the 3 process conditions of Compound A. CD in the all the tables below is defined as Critical Dimension, a term of art.

	C4F8 BKM	C3F6O P1	C3F6O P19	C3F6O P20
ER [nm/min]	305	352	404	379
Selectivity	1.21	1.0	1.1	1.0
Hole CD [nm]	388	407	456	437
BTM CD [nm]	260	239	278	317
BTM/TOP	0.67	0.59	0.61	0.73

The data shows that Compound A demonstrates higher pattern silicon oxide etch rates than C_4F_8 with slightly reduced selectivity and up to 9% improved bottom/top CD ratio.

Cross-sectional SEM images of trenches generated by the C_4F_8 BKM, P1, P19 and P20 processes with compound A are seen in FIGS. 6A-D. The SEM images demonstrate the deeper trenches with compound A with less remaining photoresist, proving the higher pattern SiO_2 etch rate and slightly reduced selectivity compared to C_4F_8. The etch profiles show straighter sidewalls than with C_4F_8 too.

[0070] Working Example 2 – Use of Compound B to Generate a Trench:



B .

Based on a blanket wafer screening DOE several process conditions were selected for a patterned wafer etch and compared to octafluorocyclobutane (C_4F_8) Best Known Method ("BKM") conditions. BKM is a term of art. The below table shows C_4F_8 BKM conditions:

RF [W]	**Bias** [W]	**Press** [mtorr]	**O2** [sccm]	**Ar** [sccm]	**C4F8** [sccm]	**Etch Time** [min]
600	600	5	3	36	21	3

The table below shows three process conditions with Compound B run on patterned wafers:

Wafer	**RF** [W]	**Bias** [W]	**Press** [mtorr]	**O2** [sccm]	**Ar** [sccm]	**C4F8O** [sccm]	**Etch Time** [min]
P4	600	600	5	5	5	25	3
P8	1200	600	5	5	5	25	3
P9	900	600	10	5	5	17.5	3

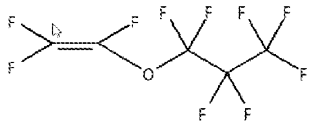
All patterned etches from the table above were carried out at a chamber temperature of 60°C and an electrode temperature of 25°C. The table below shows an etch profile comparison of the 3 process conditions of Compound B. CD in the all the tables below is defined as Critical Dimension, a term of art.

	C4F8 BKM	**C4F8O P4**	**C4F8O P8**	**C4F8O P9**
ER [nm/min]	305	306	290	311
Selectivity	1.21	1.1	1.0	1.0
Hole CD [nm]	388	369	468	361
BTM CD [nm]	260	278	468	210
BTM/TOP	0.67	0.75	1	0.58

The data shows that Compound B demonstrates comparable pattern silicon oxide etch rates to C_4F_8 with slightly lower selectivity and significant improvements to bottom/top CD ratio.

Cross-sectional SEM images of trenches generated by the C_4F_8 BKM, P4, P8 and P9 processes with compound B are seen in FIGS. 7A-D. The SEM images show deep trenches with compound B, now with less remaining photoresist, this proves the comparable pattern etch rate but reduced selectivity to that of C_4F_8. The SEM images also display significant improvements to BTM/TOP compared to C_4F_8.

[0071] Working Example 3 – Use of Compound C to Generate a Trench:



C .

Based on a blanket wafer screening DOE several process conditions were selected for a patterned wafer etch and compared to octafluorocyclobutane (C_4F_8) Best Known Method ("BKM") conditions. BKM is a term of art. The below table shows C_4F_8 BKM conditions:

RF [W]	**Bias** [W]	**Press** [mtorr]	**O2** [sccm]	**Ar** [sccm]	**C4F8** [sccm]	**Etch Time** [min]
600	600	5	3	36	21	3

Based on a blanket wafer screening DOE selected conditions were chosen for patterned wafer etch. The table below shows three process conditions with Compound C run on patterned wafers:

Wafer	**RF** [W]	**Bias** [W]	**Press** [mtorr]	**O2** [sccm]	**Ar** [sccm]	**C5F10O** [sccm]	**Etch Time** [min]
P6	900	600	8	5	5	23	3
P7	900	600	8	5	5	18	3
P8	900	600	13	5	5	18	3

All patterned etches from the table above were carried out at a chamber temperature of 60°C and an electrode temperature of 25°C. The table below shows an etch profile comparison of the 3 process conditions of Compound C. CD in the all the tables below is defined as Critical Dimension, a term of art.

	C4F8 BKM	**C5F10O P6**	**C5F10O P7**	**C5F10O P8**
ER [nm/min]	305	340	319	347
Selectivity	1.21	1.0	1.0	1.1
Hole CD [nm]	388	409	413	389
BTM CD [nm]	260	317	317	202
BTM/TOP	0.67	0.78	0.77	0.52

The data shows that Compound C demonstrates higher pattern silicon oxide etch rates than C_4F_8 with slightly reduced selectivity and improved bottom/top CD ratio.

Cross-sectional SEM images of trenches generated by the C_4F_8 BKM, P6, P7 and P8 processes with compound C are seen in FIGS. 8A-D. The SEM images demonstrate the deeper trenches with compound C with less remaining photoresist, proving the higher pattern SiO_2 etch rate and reduced selectivity than C_4F_8. The etch profiles show straighter sidewalls than with C_4F_8 too.

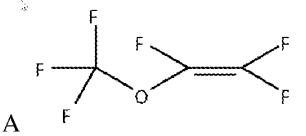
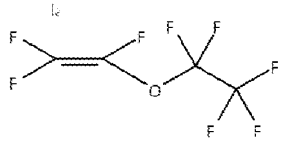
[0072] The above description is meant to be representative only, and thus modifications may be made to the aspects of the invention disclosed herein without departing from the scope of the disclosure. Thus, these modifications fall within the scope of the present disclosure and are intended to fall within the appended claims.

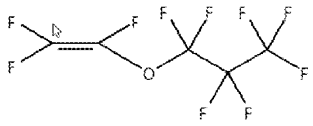
CLAIMS

What is claimed is:

1. A mixture configured to etch a thin film of an integrated circuit material, comprising:

a first compound comprising one or more of:

A , B , and



C ; and

a second compound comprising one or more of: oxygen, argon, helium, nitrogen, octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF4), methyl fluoride (CH_3F), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), or 1,1,3,3,3-pentafluoropropene (C_3HF_5).

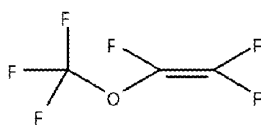
2. The mixture configured to etch a thin film of an integrated circuit material according to claim 1, wherein the thin film comprises silicon, silicon oxide, silicon dioxide, silicon carbide, silicon nitride, silicon carbonitride, silicon oxycarbide, silicon oxynitride, silicon oxycarbonitride, gallium nitride, aluminum gallium nitride, gallium arsenide, aluminum gallium arsenide, indium phosphide, indium aluminum arsenide, indium gallium arsenide, silicon germanium, silicon hydrogen bromide, zinc selenide, indium tin oxide, lead zirconium titanate, molybdenum, polysilicon, a carbon hard mask, or a photoresist material .

3. The mixture configured to etch a thin film of an integrated circuit material according to claim 1, wherein the first compound comprises greater than or equal to about 1% by volume of the mixture, and less than or equal to about 99% by volume of the mixture.

4. The mixture configured to etch a thin film of an integrated circuit material according to claim 3, wherein the second compound comprises greater than or equal to about 1% by volume of the mixture, and less than or equal to about 99% by volume of the mixture, and wherein the first compound and the second compound comprise 100% by volume of the mixture.

5. The mixture configured to etch a thin film of an integrated circuit material according to claim 4, wherein a ratio of the first compound to the second compound is between 5:1 and 1:5.

6. The mixture configured to etch a thin film of an integrated circuit material according to claim 1, wherein one or more of the following are satisfied:

(i) the first compound comprises 

; and

(ii) the second compound comprises octafluorocyclobutane (C_4F_8) or hexafluorobutadiene (C_4F_6).

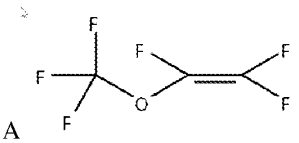
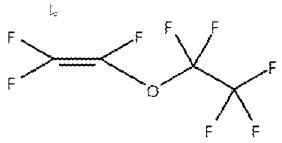
7. The mixture configured to etch a thin film of an integrated circuit material according to claim 1, further comprising a third compound comprising one or more of oxygen, argon, helium, nitrogen, octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), and carbon tetrafluoride (CF_4) octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), or 1,1,3,3,3-pentafluoropropene (C_3HF_5), nitrogen trifluoride (NF_3), and sulfur hexafluoride (SF_6).

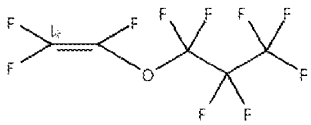
8. The mixture configured to etch a thin film of an integrated circuit material according to claim 7, wherein the third compound comprises greater than or equal to about 1% by volume of the mixture, and less than or equal to about 99% by volume of the mixture, and wherein the first compound, the second compound, and the third compound comprise 100% by volume of the mixture.

9. A method of etching a thin film of an integrated circuit material, comprising:

contacting a surface of the thin film of the integrated circuit material with a plasma comprising reactive ions generated by subjecting a mixture configured to etch the thin film of the integrated circuit material to a plasma generating device, thereby removing a portion of the thin film of the integrated circuit material;

wherein the mixture comprises a first compound comprising one or more of:

A  , B  , and



C ; and

a second compound comprising one or more of: oxygen, argon, helium, nitrogen, octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF4), methyl fluoride (CH_3F), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene

($C_3H_2F_4$), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), or 1,1,3,3,3-pentafluoropropene (C_3HF_5).

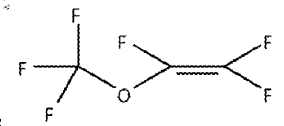
10. The method of etching a thin film of an integrated circuit material according to claim 9, wherein the thin film comprises silicon, silicon oxide, silicon carbide, silicon nitride, silicon carbonitride, silicon oxycarbide, silicon oxynitride, gallium nitride, aluminum gallium nitride, gallium arsenide, aluminum gallium arsenide, indium phosphide, indium aluminum arsenide, indium gallium arsenide, silicon germanium, silicon hydrogen bromide, zinc selenide, indium tin oxide, lead zirconium titanate, molybdenum, polysilicon, a carbon hard mask, or a photoresist material.

11. The method of etching a thin film of an integrated circuit material according to claim 9, wherein the first compound comprises greater than or equal to about 1% by volume of the mixture, and less than or equal to about 99% by volume of the mixture.

12. The method of etching a thin film of an integrated circuit material according to claim 11, wherein the second compound comprises greater than or equal to about 1% by volume of the mixture, and less than or equal to about 99% by volume of the mixture, and wherein the first compound and the second compound comprise 100% by volume of the mixture.

13. The method of etching a thin film of an integrated circuit material according to claim 12, wherein a ratio of the first compound to the second compound is between 5:1 and 1:5.

14. The method of etching a thin film of an integrated circuit material according to claim 9, wherein one or more of the following are satisfied:

(i) the first compound comprises 

; and

(ii) the second compound comprises octafluorocyclobutane (C_4F_8) or hexafluorobutadiene (C_4F_6).

15. The method of etching a thin film of an integrated circuit material according to claim 9, further comprising a third compound comprising one or more of: oxygen, argon, helium, nitrogen, octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF4), methyl fluoride (CH3F), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), 1,1,3,3,3-pentafluoropropene (C_3HF_5), nitrogen trifluoride (NF_3), and sulfur hexafluoride (SF_6).

16. The method of etching a thin film of an integrated circuit material according to claim 15, wherein the third compound comprises greater than or equal to about 1% by volume of the mixture, and less than or equal to about 99% by volume of the mixture, and wherein the first compound, the second compound, and the third compound comprise 100% by volume of the mixture.

17. The method of etching a thin film of an integrated circuit material according to claim 9, wherein the thin film comprises a first film and a second film.

18. The method of etching a thin film of an integrated circuit material according to claim 17, wherein the first film and the second film each independently comprise silicon dioxide, silicon nitride, or a masking material.

19. The method of etching a thin film of an integrated circuit material according to claim 18, wherein the first film comprises silicon dioxide and the second film comprises silicon nitride, and the mixture has an etch selectivity for silicon dioxide compared to silicon nitride of greater than or equal to about 1.

20. The method of etching a thin film of an integrated circuit material according to claim 18, wherein the first film comprises silicon dioxide or silicon nitride and the second film comprises a masking material, and the mixture has an etch selectivity for silicon dioxide compared to the masking material of greater than or equal to about 1

or the mixture has an etch selectivity for silicon nitride compared to the masking material of greater than or equal to about 1.

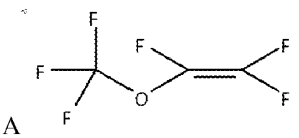
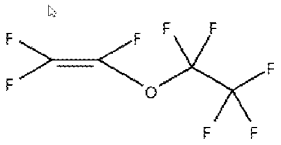
21. The method of etching a thin film of an integrated circuit material according to claim 20, wherein the masking material comprises a carbon hard mask or a photoresist material.

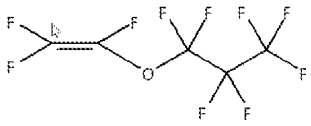
22. A method of patterning a thin film of integrated circuit material, comprising:

contacting a surface of the thin film with a plasma comprising reactive ions generated by subjecting a mixture configured to etch the thin film of the integrated circuit material to a plasma generating device, thereby removing a portion of the thin film and generating a pattern in the thin film of the integrated circuit material;

wherein at least a portion of the thin film is disposed between confronting surfaces of a substrate and a masking material layer, wherein the masking material layer comprises an aperture defined therein exposing a portion of the surface of the thin film; and

wherein the mixture comprises a first compound comprising one or more of:

A , B , and



C ; and

a second compound comprising one or more of: oxygen, argon, helium, nitrogen, octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF_4), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), 1,1,3,3,3-pentafluoropropene (C_3HF_5), nitrogen trifluoride (NF_3), and sulfur hexafluoride (SF_6).

23. The method of patterning a thin film of integrated circuit material according to claim 22, wherein the substrate is selected from the group consisting of silicon, silicon oxide, silicon dioxide, silicon nitride, tantalum, tantalum nitride, titanium nitride, aluminum oxide, copper, tungsten carbonitride, molybdenum, polysilicon, a carbon hard mask, a photoresist material and a combination thereof.

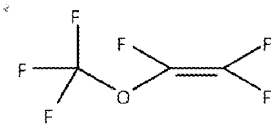
24. The method of patterning a thin film of integrated circuit material according to claim 22, wherein the thin film comprises silicon, silicon oxide, silicon carbide, silicon nitride, silicon carbonitride, silicon oxycarbide, silicon oxynitride, gallium nitride, aluminum gallium nitride, gallium arsenide, aluminum gallium arsenide, indium phosphide, indium aluminum arsenide, indium gallium arsenide, silicon germanium, silicon hydrogen bromide, zinc selenide, indium tin oxide, lead zirconium titanate, molybdenum, polysilicon, a carbon hard mask, or a photoresist material.

25. The method of patterning a thin film of integrated circuit material according to claim 22, wherein the first compound comprises greater than or equal to about 1% by volume of the mixture, and less than or equal to about 99% by volume of the mixture.

26. The method of patterning a thin film of integrated circuit material according to claim 25, wherein the second compound comprises greater than or equal to about 1% by volume of the mixture, and less than or equal to about 99% by volume of the mixture, and wherein the first compound and the second compound comprise 100% by volume of the mixture.

27. The method of patterning a thin film of integrated circuit material according to claim 26, wherein a ratio of the first compound to the second compound is between 5:1 and 1:5.

28. The method of patterning a thin film of integrated circuit material according to claim 22, wherein one or more of the following are satisfied:

(i) the first compound comprises  ; and

(ii) the second compound comprises octafluorocyclobutane (C_4F_8) or hexafluorobutadiene (C_4F_6).

29. The method of patterning a thin film of integrated circuit material according to claim 22, wherein the masking material comprises a carbon hard mask or a photoresist material.

30. The method of patterning a thin film of integrated circuit material according to claim 22, further comprising a third compound comprising one or more of: oxygen, argon, helium, nitrogen, octafluorocyclobutane (C_4F_8), hexafluorobutadiene (C_4F_6), carbonyl fluoride (COF_2), difluoromethane (CH_2F_2), trifluoromethane (CHF_3), carbon tetrafluoride (CF4), methyl fluoride (CH_3F), octafluorocyclopentene (C_5F_8), 2,3,3,3-tetrafluoropro-1-ene ($C_3H_2F_4$), hexafluoropropene (C_3F_6), hexafluorocyclopropane (C_3F_6), or 1,1,3,3,3-pentafluoropropene (C_3HF_5), nitrogen trifluoride (NF_3), and sulfur hexafluoride (SF_6).

31. The method of patterning a thin film of integrated circuit material according to claim 30, wherein the third compound comprises greater than or equal to about 1% by volume of the mixture, and less than or equal to about 99% by volume of the mixture, and wherein the first compound, the second compound, and the third compound comprise 100% by volume of the mixture.

32. The method of patterning a thin film of integrated circuit material according to claim 22, wherein the thin film comprises silicon dioxide or silicon nitride and the mixture has an etch selectivity for the thin film to the masking material of greater than or equal to about 1.

33. The method of patterning a thin film of integrated circuit material according to claim 22, wherein the thin film comprises a first film and a second film.

34. The method of patterning a thin film of integrated circuit material according to claim 33, wherein the first film comprises silicon dioxide and the second film comprises silicon nitride, and the mixture has an etch selectivity for silicon dioxide compared to silicon nitride of greater than or equal to about 1.