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(54) SIGNAL TRANSLATING CIRCUIT WITH DIFFERENTIAL AMPLIFICATION PROPERTIES

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to signal translating circuits with differential amplification properties and, more particularly, to a type of differential amplifier well suited for use in suppressing direct signal components wasteful of dynamic range in integrated circuit amplifier configurations.

"Signal translating circuits" is a term for circuits which amplify signals, change the direct component level of signals, add signals to each other, subtract signals from each other and/or invert signals. "Integrated circuitry" is a term which is used herein to describe a unitary or monolithic semiconductor structure or "chip" incorporating the equivalent of a network of interconnected active and passive electrical circuit elements (e.g. transistors, diodes, resistors, capacitors).

"Differential amplifiers" are used to amplify the differences between two input signals, usually with much higher gain than that for associated amplification of the similarities between the two input signals.

A particular need for providing an output signal which is representative of the difference between two input signal components arises when a plurality of direct coupled amplifier stages are employed and it is desired to remove an undesired, large direct component and leave the desired signal with a smaller direct component. This can be done using the common-mode rejection of a differential amplifier. Specifically, in the design of amplifier circuits employing semiconductor devices, and particularly those constructed as integrated circuits, limited output voltage

variations may be obtained. It is therefore desirable, where an object of an amplifier is to produce a varying signal as its output, to provide an input signal wherein the direct component of signal level is not large compared to the signal variations about that level conserving dynamic range in the amplifier and permitting it to produce a peak to peak output signal variation approximately equal to the available direct operating bias (B+).

In circuits employing discrete components (i.e. non-integrated circuits), capacitors and inductors frequently are used to remove direct components of signal and thereby preserve dynamic range throughout the signal processing stages. However, such elements generally cannot be conveniently fabricated on integrated circuit chips and therefore require the uneconomical and undesirable use of an "outboard" discrete component and one or more connecting terminals of the chip.

One method of constructing in integrated form a signal processing stage to provide level shift or level setting in direct coupled integrated circuits is described in our United States Patent No. 3531730 in the name of Steven Steckler. When the input signal to this signal processing stage includes an undesired direct component which exceeds the desired varying signal component, it cannot provide the desirable result of a peak to peak output voltage variation approximately equal to the available operating direct supply voltage.

In accordance with one aspect of the present invention, a differential amplifier having first and second input terminals and an output terminal comprises a first and a second semiconductor amplifier device each having a first electrode for the application of input signal, a second electrode for the application of reference potential, and a third electrode to provide output signal; a first resistive device with first and second electrodes and a non-linear conductivity therebetween proportional to the transconductance of the first amplifier device; a second resistive device with first

and second electrodes and a non-linear conductivity therebetween proportional to the transconductance of the second amplifier device; a first point of reference potential to which the second electrodes of the first amplifier device and first resistive device are connected; and a second point of reference potential to which the second electrodes of the second amplifier device and the second resistive device are connected. The first electrodes of the first amplifier device and the first resistive device are both direct current coupled to the first input terminal. The first electrodes of the second amplifier device and the second resistive device are both direct current coupled to the second input terminal and to the third electrode of the first amplifier device. The third electrode of the second amplifier device is connected to the output terminal and to means for providing operating current. The first and second resistive devices may be formed from semiconductor devices similar to the first and second semiconductor amplifier devices, which semiconductor devices are each connected in a degenerative feedback configuration.

In accordance with a further aspect of the invention, the described differential amplifier is used for removing undesired components from an input signal. Input signals including desired and undesired components are coupled to the interconnected first electrodes of the second resistive device and second semiconductor amplifier device and to the third electrode of the first semiconductor amplifier device. At least a portion of the input signals including the undesired component are coupled to the interconnected first electrodes of the first resistive device and first semiconductor amplifier device. A source of energizing current or equivalent is connected to the third electrode of the second semiconductor amplifier device, at which point output current signals including the desired component but excluding the undesired component are developed.

In accordance with a further aspect of the invention, the described differential amplifier is used for subtractively combining first and second input signals. First input voltage signals are coupled via a first impedance to the interconnected first electrodes of the second resistive device and the second semiconductor amplifier device and the third electrode of the first semiconductor amplifier device while the second input voltage signals are coupled via a second impedance to the interconnected first electrodes of the first resistive device and the first semiconductor amplifier device. A source of energizing voltage is coupled by means of an output impedance to the third electrode of the second semiconductor amplifier device. Output signals which are a function of the difference between the input signals are developed at the output impedance.

For a better understanding of the present invention and objects and advantages thereof, reference is made to the following description in conjunction with the attached drawing wherein:

FIGURE 1 is a schematic diagram of a signal translating circuit employing the present invention;

FIGURE 2 is a schematic diagram of the circuit of FIGURE 1 employing a modified biasing arrangement;

FIGURE 3 is a schematic diagram of the differential amplifier circuit employing the invention which has balanced push-pull input signals applied thereto and provides an unbalanced output signal; and

FIGURE 4 is a schematic diagram of a portion of an integrated circuit for use in a television receiver for which the present invention is particularly suited, the integrated circuit providing the functions of intermediate frequency amplification, video detection, video amplification, sound amplification and automatic gain control.

Referring to FIGURE 1 of the drawing the illustrated differential amplifier is formed basically from two similar circuits each consisting of a combination of a transistor and a diode, which diode is shown as being formed by shorting the base and collector electrodes of a transistor. The base electrodes of these two transistors in combination are connected together; so are their emitter electrodes. Transistor 10 having emitter, base and collector electrodes 10a, 10b, and 10c respectively is so connected with a diode formed from a second transistor having emitter, base and collector electrodes 12a, 12b, and 12c respectively. A second, similar combination is formed from a third transistor 26 having emitter, base and collector electrodes 26a, 26b, and 26c respectively and a diode 28 formed from a transistor having emitter, base and collector electrodes 28a, 28b, and 28c respectively. The differential amplifier configuration is formed by connecting collector 26c to junction 24, the interconnection of base electrodes 10b and 12b and collector electrode 12c. The interconnection of base electrodes 26b and 28b with collector electrode 28c is the point to which one input current to the basic differential amplifier configuration is applied; junction 24, the other. The collector electrode 10c is the point from which output current is withdrawn by the basic differential amplifier configuration.

The means shown in the drawing for applying direct current bias to collector electrode 10c is the series combination of a resistor 16 and a direct energizing voltage source 14 connected to a point of reference potential (ground). The emitter electrodes 10a and 12a are also directly connected to ground. Input signals from a modulated current source shown as being comprised of the series combination

of a resistor 22, a first, varying signal voltage source 20, and a second relatively non-varying, direct voltage source 18 are applied between the junction 24 and ground. An unmodulated current source shown as being comprised of the series combination of the relatively non-varying direct voltage source and a resistor 30 is connected across diode 28, forward biasing it; this relatively non-varying direct voltage source can coincide with the direct voltage source 18 utilized in the construction of the modulated current source supplying junction 14, as is shown in FIGURE 1.

The characteristics of diodes 12 and 28 are closely matched respectively to the characteristics of the transistors 10 and 26. In an integrated circuit structure, where the four devices are constructed simultaneously and in close proximity to one another on a single chip the conduction characteristics of all four devices will be substantially identical.

That is, for a given base-emitter voltage applied to one pair (diode and transistor) of the devices, equal emitter current densities are produced in each device. It should also be recognized that where the junction areas are unequal, proportional rather than equal emitter currents will be produced in the two devices for a given input. The following explanation will relate to the condition of equal currents in the two devices of a pair for illustrative purposes.

The operation of the circuit of FIGURE 1 will be described by first considering the circuit which would be formed if the connection from collector electrode 26c to junction point 24 as well as the connection from resistor 30 to the junction point between sources 18 and 20 were severed, that is transistor 26 and diode 28 are removed from the circuit. The operation of such a circuit is described in detail in the above-identified U.S. Patent No. 3531730. In such a circuit, where transistor 10 and diode 12 produce equal emitter currents as well as equal emitter current densities for a given input voltage, the voltage gain of the circuit, both for alternating and direct input voltage components, is equal to the ratio of resistance

$$\frac{R_{16}}{R_{22}}$$

Where it is desired to linearly reproduce an input voltage at the output (collector electrode 10c) of the configuration, the ratio

$$\frac{R_{16}}{R_{22}}$$

is selected so that the maximum input voltage

provided by the combined source 18, 20 (direct voltage component plus maximum positive-going varying signal voltage component) multiplied by the selected gain is not greater than the voltage provided by source 14. That is, the gain must be selected to prevent "bottoming" at the output electrode 10c of transistor 10 when maximum input signal is applied. A further constraint on the gain is related to the fact that the minimum input voltage provided by the combined source 18, 20 (direct voltage component minus maximum negative-going varying signal voltage component) must at least equal the forward conduction or offset voltage of diode 12 (V_{be}) to preclude distortion resulting from cutoff of diode 12 and transistor 10. If the direct voltage component of the input signal is greater than the negative-going signal component, the minimum input voltage will exceed this offset voltage. The excess direct voltage will then result in production of a direct current in diode 12 which, in turn, will result in a direct collector current in transistor 10 and a direct voltage drop across resistor 16. In this case, the dynamic range of the output voltage (i.e. the available range of signal variation) is less than the full supply voltage of source 14. The gain must be selected less than that for the case where the minimum input voltage equals the diode offset voltage. The unmodulated direct voltage drop across the resistor 16 causes undesirable power dissipation and a resultant loss in efficiency in the translating stage.

Referring again to the complete circuit diagram of FIGURE 1, the above-described shortcoming is overcome by draining from diode 12 the direct current bias (caused by the excess direct input voltage) that gives rise to the unmodulated direct voltage drop across resistor 16. This current drain is provided by a second pair of semiconductor devices 26 and 28 which have characteristics that are substantially the same as those of devices 10 and 12. The two pairs of devices and associated components form a differentially operating configuration which exhibits rejection of commonly applied voltages such as that provided by source 18.

Specifically, the direct voltage component source 18 provides a voltage of a polarity and of sufficient magnitude to forward bias both diode 28 and the base-emitter junction of transistor 26 (i.e. $V_{18} > V_{be_{26}}$). As is described in the above-mentioned U.S. Patent

No. 3531730, a direct current is produced in diode 28 and a substantially equal direct current is demanded in the collector-emitter circuit of transistor 26 by virtue of the fact that the input junctions of diode 28 and transistor 26 are matched and furthermore, they are coupled directly in parallel.

The direct current component supplied to diode 28 is given by the expression:

$$I_{28} = \frac{(V_{18} - V_{be_{28}})}{R_{30}}$$

where

I_{28} = the direct current component in diode 28

5 V_{18} = the direct voltage component of source 18

$V_{be_{28}}$ = the voltage across diode 28 when it

is conducting in the forward direction

10 R_{30} = the resistance of resistor 30.

The direct emitter current demanded by transistor 26 is substantially identical to the current I_{28} as noted above. For transistors of the type normally fabricated by integrated circuit techniques (e.g. $\beta > 30$), the collector current of transistor 26 will be substantially equal to its emitter current. Therefore, with the resistance value of resistor 22 equal to or less than that of resistor 30, and the collector electrode 26c at the same or a lower voltage as compared with the base electrode 28b, the direct current supplied to resistor 22 by source 18 will be sufficient to supply the collector-emitter direct current demand of transistor 26. Where resistors 22 and 30 are of equal value, the direct collector-emitter current of transistor 26 is equal to the direct current in resistor 22. The collector electrode 26c is maintained substantially at the voltage $V_{be_{28}}$

30 since the base electrode 12b of diode 12 is connected directly to collector electrode 26c, thereby preventing increases in voltage at collector electrode 26c above the forward conduction voltage of diode 12 ($V_{be_{28}} = V_{be_{12}}$).

35 Furthermore, the value of resistors 22 and 30 is selected sufficiently large with respect to all expected voltage variations of the input source 18, 20 that transistor 26 is not driven into saturation for any input signal conditions.

40 Where resistor 22 is of a smaller value than resistor 30, direct current supplied from source 18 to junction point 24 (i.e. current through resistor 22) will exceed the direct collector current demand of transistor 26. The excess of direct current will be supplied to diode 12 and the base-emitter circuit of transistor 10 as bias current. In a particular application, therefore, resistor 22 may differ in value from resistor 30 according to bias requirements of diode 12 and transistor 10.

50 As stated above in connection with diode 28 and transistor 26, the collector-emitter current of transistor 10 will be substantially equal to the base-emitter current in diode 12. The bias current supplied to diode 12 is selected in relation to the nature of the signal

provided by source 20, the relative voltage of supply 14 and the resistances of resistors 22 and 16.

For example, assuming that the source 20 provides a symmetrical alternating voltage waveform (no direct voltage component), it is desirable to bias transistor 10 such that the quiescent voltage at collector electrode 10c is substantially one-half the voltage of source 14. Resistors 22 and 30 are selected unequal to provide a desired bias (excess) current to diode 12, which direct current is also produced in the collector circuit of transistor 10. Resistor 16 is then selected equal to the quotient of one-half the voltage provided by source 14 and the desired quiescent collector current in transistor 10. Furthermore, in order to obtain a maximum signal voltage component at collector electrode 10c, the ratio of resistors 16 and 22 is selected to satisfy the expression:

$$\frac{R_{16}}{R_{22}} = \frac{V_{14}}{V_{p-p_{20}}}$$

where

V_{14} = voltage of source 14

$V_{p-p_{20}}$ = peak to peak voltage of source 20.

For the case where the signal source 20 provides a varying direct voltage signal, the bias current provided for diode 12 is selected only of sufficient magnitude to insure all signal voltages are reproduced at collector electrode 10c. That is, a relatively small bias current is supplied to diode 12 and the quiescent voltage at collector electrode 10c is almost equal to V_{14} . The ratio

$$\frac{R_{16}}{R_{22}}$$

is selected according to the expression specified above. The signal voltage gain of the total configuration is equal to

$$\frac{R_{16}}{R_{22}}$$

It can be seen from the above discussion that the circuit shown in FIGURE 1 has the capability of providing an output signal at collector electrode 10c which is independent of the magnitude of all or any undesired portion of the direct voltage component provided by source 18.

On the other hand, the varying voltage signal component provided by source 20 is amplified at collector electrode 10c. The direct voltage level of the amplified voltage at col-

lector electrode 10c may be selected by appropriate choice of value for resistors 16, 22 and 30 with respect to the operating voltage as set forth above. Preferably the active devices

5 have high transconductance compared with the admittances of resistors 30 and 22.

Referring to FIGURE 2, a modification of the circuit of FIGURE 1 is shown wherein bias currents for diode 12 and transistor 10

10 are derived from the voltage source 14 by means of an additional resistor 32 coupled between source 14 and junction point 24.

In FIGURE 2, as well as subsequent Figures, devices corresponding to the diode-connected transistors 10 and 12 of FIGURE 1 will be shown with the conventional diode symbol. The circuit in FIGURE 2 operates in substantially the same manner as the circuit of FIGURE 1 with the exception that resistor 32 is selected to provide the desired bias current for diode 12 and transistor 10. In this case, resistors 22 and 30 may be of equal resistance value while resistors 16 and 32 are selected to provide a desired quiescent operating point for transistor 10 (e.g. resistors 16 and 32 are equal for a varying direct voltage signal input provided by source 20). The signal voltage gain of the total configuration is again determined substantially by the ratio

$$30 \quad \frac{R_{16}}{R_{32}}$$

Greater independence in selection of circuit values is afforded by this configuration. Furthermore, where there is an uncertainty as to the direct voltage component provided by source 18, the circuit of FIGURE 2 may be arranged with a stabilized voltage source 14 so that bias currents for diode 12 and transistor 10 are stabilized.

Referring to FIGURE 3 of the drawing, a further embodiment of the invention which may be employed where signals from two input sources are to be combined, the combination being referenced to a direct voltage level different from that of the input signals. The specific embodiment relates to the case where oppositely phased (i.e. push-pull) input signals are provided. This configuration may be employed, for example, where it is desired to convert a balanced push-pull input signal to a single-ended output signal with a desired direct voltage level. In FIGURE 3, the varying signal component source 20 is coupled across the primary winding 34a of a transformer 34 provided with a center-tapped secondary winding 34b. Direct voltage component source 18 is connected between a reference voltage (ground) and the center-tap 34c of transformer 34. All remaining components shown in FIGURE 3 are designated by the same reference numerals as are employed in FIGURES 1 and 2.

In the operation of the circuit shown in FIGURE 3, it will be assumed that the resistors 22 and 30 are of equal resistance values while resistor 32 is selected with respect to source 14 to provide sufficient bias current to diode 12 and transistor 10 to insure that both devices are conducting for all expected signal levels in the circuit. Resistor 16 is selected for this case equal to one-half the value of resistor 32 to insure maximum utilization (signal modulation) of the voltage at collector electrode 10c.

As described above in connection with FIGURES 1 and 2, substantially equal direct currents are supplied to diode 28 and to the collector-emitter circuit of transistor 26 where the voltage of source 18 is assumed to be greater than the nominal V_{be} of diode 28. Assuming a sinusoidal input voltage waveform is supplied by source 20, when the signal voltage applied to resistor 30 is positive, signal current in addition to the direct current supplied by source 18 is supplied to diode 28 and the base-emitter junction of transistor 26. The increased current in diode 28 is matched by an increase in collector-emitter current of transistor 26, the latter increased current being supplied by a decrease in the bias current supplied via resistor 32 to diode 12. At the same time, the voltage supplied to resistor 22 decreases sinusoidally, further reducing the current which can be supplied via resistor 22 to collector electrode 26c. The further deficiency in current available for transistor 26 is also supplied via resistor 32 so as to further reduce the current in diode 12. Thus a reduction in current in diode 12 twice the increase in current in diode 28 is produced. A reduction in current in the collector-emitter circuit of transistor 10 equal to that in diode 12 is produced. An amplified voltage change is therefore produced at collector electrode 10c.

For the opposite half-cycle of voltage supplied by source 20, the current in diode 28 decreases, the current in transistor 26 decreases by a like amount and the current in diode 12 increases by twice that amount. The opposite half-cycle of input voltage is therefore similarly amplified.

Various modifications of the circuit shown in FIGURE 3 may be made. For example, a second set of four semiconductor devices and associated components identical to those shown may also be coupled across transformer 34. The input signal connections to the second set of devices would, however, be interchanged with respect to those shown so that the output from the second set of devices would be 180° out of phase with respect to the output from the first set. In this manner, the push-pull input signals could be converted to amplified push-pull output signals referenced to a direct voltage level independent of that of the input signals.

A circuit substantially as shown in FIGURE 3 may also be employed where it is desired to combine (e.g. subtract) signals from two independent signal sources. In that case, for example, separate primary windings may be coupled to separate secondary windings of two input transformers in place of transformer 34. The separate secondary windings (or any other appropriate independent signal sources) then may be coupled respectively to the first and second input terminals of the signal translating stage such that the difference between the applied input signals is produced across the output impedance with a direct voltage reference level substantially independent of that of the input signals. It should also be noted that for this case separate gains may be selected for each of the independent signal sources, the separate gain being determined by the ratio of the output impedance 16 to the respective input impedances 22 and 30.

Referring to FIGURE 4 of the drawing, an integrated circuit arranged for providing the functions of intermediate frequency amplification, video detection, video amplification, intermediate frequency sound amplification and automatic gain control in a television receiver is illustrated partially in block diagram and partially in schematic form. This embodiment is the subject of our Application 9876/70 (Serial No. 1298272) copending herewith.

In FIGURE 4, those circuit elements which are fabricated on the integrated circuit chip are enclosed within a dashed line. Operating voltage (B+) is indicated as being supplied from a source external to the chip. For illustrative purposes connecting conductors between several devices on the chip and the external B+ supply have not been shown but rather the point of application of operating voltage to those devices is indicated by the symbol B+. All points internal to the chip which bear the designation B+ are coupled by conductive paths to the single B+ terminal of the chip. Similarly, ground designations have been shown at numerous locations within the chip. External ground connections are provided to terminals at each end of the chip and all points within the chip designated as connected to ground are connected internally on the chip to one or the other of these terminals. For a more detailed description of the physical arrangement of components on the chip, reference may be made to our United States Patent No. 3564125 in the name of Jack Avins.

In FIGURE 4, the intermediate frequency output signal produced by a television tuner is coupled by means of a first frequency selective filter 40 to a first intermediate frequency amplifier 42. Amplified i-f signals produced by amplifier 42 are coupled by means of a second frequency selective filter 46 to directly

coupled second and third i-f amplifier stages 48 and 50.

A further output of second frequency selective filter 46 is coupled to a sound i-f mixer-amplifier 51, the output of which is a 4.5 MHz carrier wave modulated by the accompanying television sound information.

The output of third i-f amplifier 50 is coupled to a base electrode 52b of video detector transistor 52 arranged in an emitter follower configuration. A load resistor 54 is coupled between an emitter electrode 52a of detector 52 and a point of reference voltage (e.g. ground) by means of a bias modulating transistor 56. A filter capacitor 58 is connected between emitter electrode 52a and ground. The output of video detector 52 is coupled by means of a 45 MHz filter network 60 to the base electrode 62b of an emitter follower stage 62. A peaking capacitor 64 is coupled between emitter electrodes 52a and 62a.

Emitter electrode 62a is connected to a first input terminal 65 of a signal translating stage indicated generally by the reference numeral 66. An impedance network comprising a resistor 67 coupled in parallel with a series video peaking combination of a resistor 68 and a capacitor 70 is coupled between emitter electrode 62a and a first circuit junction 72 within signal translating stage 66. A zener diode 74 is coupled from the junction of capacitor 70 and resistor 68 to ground.

The output of third i-f amplifier 50 is also coupled to a filter network comprising a resistor 76 and a capacitor 78 coupled in series between the output of amplifier 50 and ground. A direct voltage which is developed across capacitor 78 is coupled to a bias reference transistor 80, the emitter electrode 80a of which is coupled to the junction of resistor 54 and bias modulating transistor 56. The output of transistor 80 is coupled by means of a 45 MHz filter network 82 (substantially identical to network 60) to an emitter follower transistor 84. An emitter electrode 84a of transistor 84 is connected to a second input terminal 85 of signal translating stage 66. An impedance comprising a resistor 86 is connected between input terminal 85 and a second circuit junction 88 within signal translating stage 66.

Signal translating stage 66 comprises a first transistor 90 having an emitter electrode 90a connected to ground, a collector electrode 90c coupled by means of an output load resistor 92 to a source of operating voltage (B+) and a base electrode 90b connected to first circuit junction 72. A second semiconductor device illustrated as a diode 94 comprising a base electrode 94b and an emitter electrode 94a is directly connected between base electrode 90b and emitter electrode 90a. Diode 94 preferably is fabricated as a transistor identical to transistor

90 but having its collector electrode (not shown) connected directly to base electrode 94b. Signal translating stage 66 further comprises third and fourth semiconductor devices shown as a transistor 96 and a diode 98 which bear the same structural and operational relationship to each other as do devices 90 and 94. Transistor 96 comprises an emitter electrode 96a directly connected to ground, a collector electrode 96c connected to a first circuit junction 72 (i.e. the junction of resistor 67 and base electrode 90b) and a base electrode connected to second circuit junction 88 (i.e. one end of resistor 86). Diode 98 comprises an emitter electrode 98a connected to emitter electrode 96a and a base electrode 98b connected to base electrode 96b at second circuit junction 88.

The output of signal translating stage 66 which is developed at collector electrode 90c is directly connected to a video amplifier transistor 100. Video amplifier transistor 100 is supplied with bias current by means of a current source 102 coupled to emitter electrode 100a through a resistor 104. Amplified video and synchronizing signal components of the detected composite television signal are produced at emitter electrode 100a and are coupled to further video amplifier stages and a synchronizing signal separator circuit as is customary in television receivers. Video amplifier transistor 100 also supplies video signals to a keyed automatic gain control detector 106 and a noise elimination circuit 108. Keying pulses are coupled to noise circuit 108 and AGC detector 106 from the horizontal deflection circuit of the television receiver. AGC detector 106 provides gain control for the i-f and tuner amplifiers in a manner claimed and described in detail in our co-pending British Patent Application No. 9873/70 (Serial No. 1290091).

In the operation of the circuit illustrated in FIGURE 4, amplified i-f signals are produced at the output of third i-f amplifier 50 and are applied to base electrode 52b of video detector 52. Furthermore, since i-f amplifiers 48 and 50 and detector 52 are directly coupled one to another in the order named and are coupled to a common operating voltage source (B+), a substantial undesired direct voltage component is also produced at the base electrode 52b of detector 52. The undesired direct voltage component is removed by means of signal translating stage 66 as will be explained below.

The i-f signal component of the voltage produced at base electrode 52b is filtered by means of resistor 76 and capacitor 78 so that substantially the entire undesired direct voltage component (e.g. 5.5 volts) appears across capacitor 78. The direct voltage component across capacitor 78 reduced by the base-emitter voltage drop (e.g. 0.6 volts) of transistor 80 appears at the junction of emitter

electrode 80a and resistor 54. Similarly, the undesired direct voltage component at base electrode 52b reduced by the base-emitter voltage drop of detector transistor 52 appears at the junction of emitter electrode 52a and resistor 54. The direct voltage at emitter electrode 80a is slightly less than that at emitter electrode 52a such that a small bias current (of the order of 50 microamperes) is supplied to emitter electrode 52a via resistor 54 (e.g. 4000 ohms). Video detector transistor 52 is thereby arranged for linear response to i-f signals down to very low levels as is explained in detail in our United States Patent No. 3560865, in the name of Jack R. Harford.

The direct voltage component produced at emitter electrode 80a, reduced by an additional base-emitter voltage drop of transistor 84 is produced at second input terminal 85 of signal translating stage 66. Similarly, the undesired direct voltage component reduced by the base-emitter voltage of detector 52 and the detected video signal produced at emitter electrode 52a are coupled to emitter-follower transistor 62. The direct voltage component, further reduced by the base-emitter voltage drop of transistor 62, along with the detected video signals are produced at first input terminal 65. As will be explained below, signal translating stage 66 is arranged to reject or remove those voltage components which are common to input terminals 65 and 85 and to amplify those voltage components which appear at only one input terminal. Specifically, the undesired direct voltage component which corresponds to the direct voltage component at the output of third i-f amplifier 50 is removed while the detected video signal component produced at the output of video detector 52 is amplified and coupled to video amplifier transistor 100 by signal translating stage 66.

Signal translating stage 66 operates in substantially the same manner as the circuit shown in FIGURE 1. The undesired direct voltage component source represented in FIGURE 1 by battery 18 corresponds to the direct voltage produced at the output of third i-f amplifier 50 and coupled via transistors 62 and 84 to input terminals 65 and 85, respectively, in FIGURE 4. The desired varying signal source 20 of FIGURE 1 corresponds to the video detector transistor 52 which provides video signal components via transistor 62 to input terminal 65. In FIGURE 4, the undesired direct voltage component provided at input terminal 85 produces a direct current in resistor 86 and in diode 98. A substantially equal direct collector current is demanded by transistor 96. This latter current is supplied by means of the undesired direct voltage component provided at input terminal 65. Resistor 67 is selected slightly less than resistor 86 (e.g. 1980 ohms as compared to

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2000 ohms) so as to provide a direct bias current to diode 94 and to the base-emitter junction of transistor 90. This bias current insures conduction of diode 94 and transistor 90 in response to low level video signal components.

The video signal components provided at input terminal 65 produce current variations in diode 94 and the input (base-emitter) circuit of transistor 90. A varying voltage corresponding to the video signal component is therefore produced at collector electrode 90c. The video signal voltage at collector electrode 90c is substantially equal to the corresponding voltage at input terminal 65 multiplied by the ratio

$$\frac{R_{92}}{R_{67}}$$

(the signal gain of translating stage 66). Typically, resistor 92 is of the order of 8000 ohms, thereby providing a video signal voltage gain of approximately four in translating stage 66. Since the input bias supplied to transistor 90 is relatively small, the output video signal may vary substantially between B+ and ground with substantially no undesired direct voltage component.

The operation of modulating bias transistor 56 is explained in detail in the above-identified United States Patent No. 3560865. For purposes of the present explanation, it is sufficient to note that transistor 56 responds to video signal representative current supplied via resistor 67 so as to maintain bias reference transistor 80 conductive for all expected video signal levels at video detector 52. The maximum video signal level at the output of video detector 52 is maintained at a desired level by operation of the AGC circuit of the television receiver.

WHAT WE CLAIM IS:—

1. A signal translating circuit with a differential amplification property having first and second input terminals and an output terminal, comprising a first and a second semiconductor amplifier device each having a first electrode for the application of input signal, a second electrode for the application of reference potential, and a third electrode to provide output signal; a first resistive device with first and second electrodes and a non-linear conductivity therebetween proportional to the transconductance of said first amplifier device; a second resistive device with first and second electrodes and a non-linear conductivity therebetween proportional to the transconductance of said second amplifier device; a first point for reference potential to which point the second electrodes of said first amplifier device and first resistive device are connected; a second point for reference poten-

tial to which point the second electrodes of said second amplifier device and said second resistive device are connected; first means for direct current coupling the interconnection of the first electrodes of said first amplifier device and said first resistive device to said first input terminal; second means for direct current coupling said second input terminal to said third electrode of said first amplifier device and to the interconnections of the first electrodes of said second resistive device and said second amplifier device, and means for providing operating current to the third electrode of said second amplifier device, the third electrode of said second amplifier device being direct current coupled to said output terminal.

2. A signal translating circuit with a differential amplification property as claimed in Claim 1, comprising a respective semiconductor amplifier device having a first electrode for the application of input signal, a second electrode for the application of reference potential, and a third electrode to provide output signal, the first electrode being direct coupled to the third electrode, to provide each of said resistive devices, said second and third electrodes of said amplifier device corresponding respectively to said second and first electrodes of said resistive device.

3. A signal translating circuit with a differential amplification property as claimed in Claim 2, in which the direct coupling of the first electrode of each semiconductor device to its third electrode is a direct connection.

4. A signal translating circuit with a differential amplification property as claimed in any of the preceding claims, in which said semiconductor amplifier devices have a high transconductance as compared to the admittance of either of said direct current coupling means.

5. A signal translating circuit with a differential amplification property as claimed in Claim 4, in which said semiconductor amplifier devices are bipolar transistors with said associated first, second, and third terminals corresponding respectively to base, emitter, and collector terminals.

6. A signal translating circuit with a differential amplification property as claimed in any of the preceding claims in which at least one of said direct current coupling means consists of a direct connection.

7. A signal translating circuit with a differential amplification property as claimed in Claim 4 or 5 in which at least one of said direct current coupling means consists of a resistor.

8. A signal translating circuit with a differential amplification property as claimed in Claim 7 in which the input terminal connected to each of said direct current coupling means consisting of a resistor in combination with a source of input voltage signals.



2000 ohms) so as to provide a direct bias current to diode 94 and to the base-emitter junction of transistor 90. This bias current insures conduction of diode 94 and transistor 90 in response to low level video signal components.

The video signal components provided at input terminal 65 produce current variations in diode 94 and the input (base-emitter) circuit of transistor 90. A varying voltage corresponding to the video signal component is therefore produced at collector electrode 90c. The video signal voltage at collector electrode 90c is substantially equal to the corresponding voltage at input terminal 65 multiplied by the ratio

$$\frac{R_{92}}{R_{67}}$$

(the signal gain of translating stage 66). Typically, resistor 92 is of the order of 8000 ohms, thereby providing a video signal voltage gain of approximately four in translating stage 66. Since the input bias supplied to transistor 90 is relatively small, the output video signal may vary substantially between B+ and ground with substantially no undesired direct voltage component.

The operation of modulating bias transistor 56 is explained in detail in the above-identified United States Patent No. 3560865. For purposes of the present explanation, it is sufficient to note that transistor 56 responds to video signal representative current supplied via resistor 67 so as to maintain bias reference transistor 80 conductive for all expected video signal levels at video detector 52. The maximum video signal level at the output of video detector 52 is maintained at a desired level by operation of the AGC circuit of the television receiver.

WHAT WE CLAIM IS:—

1. A signal translating circuit with a differential amplification property having first and second input terminals and an output terminal, comprising a first and a second semiconductor amplifier device each having a first electrode for the application of input signal, a second electrode for the application of reference potential, and a third electrode to provide output signal; a first resistive device with first and second electrodes and a non-linear conductivity therebetween proportional to the transconductance of said first amplifier device; a second resistive device with first and second electrodes and a non-linear conductivity therebetween proportional to the transconductance of said second amplifier device; a first point for reference potential to which point the second electrodes of said first amplifier device and first resistive device are connected; a second point for reference poten-

tial to which point the second electrodes of said second amplifier device and said second resistive device are connected; first means for direct current coupling the interconnection of the first electrodes of said first amplifier device and said first resistive device to said first input terminal; second means for direct current coupling said second input terminal to said third electrode of said first amplifier device and to the interconnections of the first electrodes of said second resistive device and said second amplifier device, and means for providing operating current to the third electrode of said second amplifier device, the third electrode of said second amplifier device being direct current coupled to said output terminal.

2. A signal translating circuit with a differential amplification property as claimed in Claim 1, comprising a respective semiconductor amplifier device having a first electrode for the application of input signal, a second electrode for the application of reference potential, and a third electrode to provide output signal, the first electrode being direct coupled to the third electrode, to provide each of said resistive devices, said second and third electrodes of said amplifier device corresponding respectively to said second and first electrodes of said resistive device.

3. A signal translating circuit with a differential amplification property as claimed in Claim 2, in which the direct coupling of the first electrode of each semiconductor device to its third electrode is a direct connection.

4. A signal translating circuit with a differential amplification property as claimed in any of the preceding claims, in which said semiconductor amplifier devices have a high transconductance as compared to the admittance of either of said direct current coupling means.

5. A signal translating circuit with a differential amplification property as claimed in Claim 4, in which said semiconductor amplifier devices are bipolar transistors with said associated first, second, and third terminals corresponding respectively to base, emitter, and collector terminals.

6. A signal translating circuit with a differential amplification property as claimed in any of the preceding claims in which at least one of said direct current coupling means consists of a direct connection.

7. A signal translating circuit with a differential amplification property as claimed in Claim 4 or 5 in which at least one of said direct current coupling means consists of a resistor.

8. A signal translating circuit with a differential amplification property as claimed in Claim 7 in which the input terminal connected to each of said direct current coupling means consisting of a resistor in combination with a source of input voltage signals.

9. A signal translating circuit with a differential amplification property as claimed in any of the preceding claims, comprising a resistor in series with a source of operating potential comprising said means for providing an operating current to the third electrode of said second amplifier device. 5
10. A signal translating circuit with a differential amplification property as claimed in any of the preceding claims, comprising means to supply one of said input terminals with a signal consisting solely of a direct component. 10
11. A signal translating circuit with a differential amplification property as claimed in any of the preceding claims, in which its said component elements are disposed in a single integrated circuit. 15
12. A signal translating circuit with a differential amplification property substantially as hereinbefore described in conjunction with Figure 1 or Figure 2 or Figure 3 or Figure 4 of the accompanying drawings. 20

T. I. M. SMITH,
Chartered Patent Agent,
50 Curzon Street,
London W1Y 8EU.
Agent for the Applicant.

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