ABSTRACT

Semiconductor Devices Having pFET with SiGe Gate Electrode and Embedded SiGe Source/Drain Regions and Methods of Making the Same

In a method of making a semiconductor device, a first gate stack including a first gate electrode material is formed on a substrate at a pFET region. The PFET source/drain regions of the substrate and the first gate electrode material of the first gate stack at the pFET region are etched. The etching being at least partially selective so that the nFET region is shielded by a stress inducing mask layer formed thereon and so that a spacer structure of the pFET region at least partially retained. The etching forms PFET source/drain recesses and also removes at least part of the first gate electrode material at the pFET region providing a gate electrode recess. A SiGe material is epitaxially grown in the source/drain recesses and in the gate electrode recess at the pFET region. The SMT effect is also achieved at the NFET from the stress inducing mask layer.

Fig. 15