

Organic Memory Device and Method of Its Manufacture

Reference to Related Application

Reference is made to our earlier United States provisional patent application number
5 60/802,167 filed May 22, 2006 for an invention titled "Synthesis, Design and Method of
Forming Nanoparticles based on organic Floating State Memory Devices" the priority
of which is hereby claimed, and the contents of which are hereby incorporated by
reference as if disclosed herein in their entirety.

10 Technical Field

This invention relates to an organic memory device and a method of its manufacture and
refers particularly, though not exclusively, to a nanostructure-based organic floating
gate memory and method of its manufacture employing chemical self-assembly and
using nanostructures and/or nano-particles as charge storage components.

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Background

Research in organic electronics has been gaining increasing interest in recent years due
to its potential in providing low-cost fabrication, compatibility with flexible substrates,
amenable to small specialized production runs, suitability for large-area deposition and
20 suitability for mass production. Organic memory offers very attractive alternative
solutions in a number of niche applications of electronics where low cost and inclusion
of different functionalities are desirable. Organic memories have a simple device
design, offering the potential of uncomplicated integration and simple cell concepts with
very small cell sizes. They are of low-cost since they are much simpler to manufacture

than silicon chips and are easy to stack, packing bits at high density. Organic memories also have the extendibility to sensing, radio frequency identification (RFID) and passive or active matrix backplanes.

- 5 Under the three main streams of semiconductor memory technologies – Static Random Access Memory (SRAM), Dynamic Random Access Memory (DRAM) and Flash Memory, only the Flash memory shows non-volatile characteristics. But DRAM shows high density capabilities while SRAM has fast read/write performance. It would be advantageous to be able to combine the benefits of these three types of inorganic
- 10 memories – non-volatility, high performance and high density. Organic memories offer the potential to exhibit such desired characteristics.

Although switching and memory phenomena in organic materials and devices have been reported for more than 30 years, high performance organic memory is still lacking.

- 15 Three-terminal transistors, using ferroelectric polymers, and two-terminal bistable devices, which exploit charge transfer between metal atoms and organic compounds, exhibit interesting performance but are far from practical applications in memory.

- A new electronic bi-stable device with a triple-layer structure consisting of two organic
- 20 layers and a middle discontinuous metal layer, sandwiched between two metal electrodes, has been proposed. It exhibits promising performance and can be used as non-volatile memory. However, its fabrication is by thermal evaporation in a high vacuum, and stringent conditions are required to control the morphology of the middle, discontinuous metal layer. Additional addressing of the sandwich-type memory device

and integration with other transistors is still needed. This will further increase the cost, making organic memories not cost-effective.

5 Floating-gate type transistor-based memory devices that utilize discrete traps as charge storage elements may be integrated as non-volatile memory in logic systems by leveraging on materials used in other silicon transistors and upon conventional silicon microelectronics know-how. The discrete charge storage elements utilized in such devices are usually isolated Si, Ge or metal nanocrystals.

10 Much research has been conducted on nanostructure or nano-particle formation using high temperature CMOS compatible processes. Organic memory devices which use organically passivated nanoparticles as charge storage elements can be deposited at room temperature using simple chemical self-assembly, Langmuir-Blodgett or spin-coating methods. Room temperature formation of nanostructures may find application
15 in future 3-D organic memory architectures, compatible with the low temperature processable materials such as, for example, polymers.

Known organic memory devices involve the use of a multi-step approach of pre-synthesizing nano-particles that have a repulsive interaction so that agglomeration will
20 not occur prior to embedding the particles in an organic layer. This is then followed by the various layers deposition process. This process is overly complex.

Summary

According to a first exemplary embodiment there is provided an organic memory device comprising: an active layer; at least one charge storage layer comprising a film of an organic dielectric material, and nanostructures and/or nano-particles of a charge-storing material on or in the film of dielectric material, each of the nanostructures and/or nano-particles being separated from the others of the nanostructures and/or nano-particles by the organic dielectric material of the organic dielectric film.

The organic memory device may further comprise a tunnelling layer on a first side of the at least one charge storage layer, and a control layer on a second side of the charge storage layer, the first side being opposite the second side. The control layer may be integral with the at least one charge storage layer. Additionally or alternatively, the tunnelling layer may be integral with the at least one charge storage layer.

The film of organic dielectric material may comprise a self-assembled copolymer selected from the group consisting of: diblock, triblock, and multiblock. The film of organic dielectric material may comprise a self-assembled monolayer that may consist of silane derivatives. The nanostructures and/or nano-particles may have an affinity with the self-assembled copolymer or self-assembled monolayer.

According to another exemplary aspect there is provided a method for the fabrication of an organic memory device, the method comprising forming a control layer on a gate electrode, forming a charge storage layer including nanostructures and/or nano-particles on the control layer, forming a tunnelling layer on the charge storage layer, and forming an active layer on the tunnelling layer.

The control layer may be formed integrally with the charge storage layer. Additionally or alternatively, the tunnelling layer may be formed integrally with the charge storage layer. The charge storage layer may comprise a self-assembled copolymer film and the nanostructures and/or nano-particles. The nanostructures and/or nano-particles may be
5 formed on the film by at least one of: spin-coating, screen-printing, and inkjet-printing.

The charge storage layer may include nanostructures and/or nano-particles prepared in a single solution for a self-assembled copolymer film and a precursor for the nanostructures and/or nano-particles. The method may further comprise performing a
10 reduction in the single solution; and adjusting a viscosity of the solution for different deposition processes. The single solution may be cast on a thin oxide layer to form the charge storage layer.

The control layer and the tunnelling layer may both comprise a self-assembled
15 monolayer. The nanostructures and/or nano-particles may be formed between the two layers of self-assembled monolayer. The nanostructures and/or nano-particles may have an affinity to the self-assembled monolayers. The affinity may be physical and/or chemical. The nanostructures and/or nano-particles may be deposited on a first of the two layers of self-assembled monolayer and the other of the two layers of self-
20 assembled monolayer may then be deposited on the nanostructures and/or nano-particles. The self-assembled copolymer may be: diblock, triblock, or multiblock.

For both exemplary aspects, each of the nanostructures and/or nano-particles may be electrically isolated. The charge storage layer may comprise a single layer. The

nanostructures and/or nano-particles may be within the single layer. Alternatively, the charge storage layer may comprise two layers. The nanostructures and/or nano-particles may be formed between the two layers.

- 5 The self-assembled copolymer may be of a material consisting of: vinylene-based, methacrylate-based, and polyethylene oxide-based monomers.

The nanostructures and/or nano-particles may have an affinity with the self-assembled copolymer. The affinity may be at least one of: physical, and chemical. The
10 nanostructures and/or nano-particles may be at least one of: metal, oxide of a metal, semiconductor, ceramic, semiconducting nano-particles, nanoclusters, nanorods, nanofibers, quantum dots, fullerene, and derivatives of fullerene. The quantum dots may be of: gold, silver, copper, titanium dioxide, zinc dioxide, cadmium selenides, and/or cadmium sulphides.

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A charge storage capability may be able to be adjusted by adjusting a concentration of the nanostructures and/or nano-particles in the single solution.

The organic memory device may comprise a thin film transistor. The thin film transistor
20 may further comprise a source electrode, a drain electrode, and a gate electrode. The active layer may comprise a semiconductor. The thin film transistor may further comprise a supporting substrate selected from: glass, plastic, quartz, metal foil, undoped silicon and heavily doped silicon.

The tunnelling layer and control layer may comprise a floating gate dielectric. The floating gate dielectric may comprise: dielectrics, and/or a copolymer-based dielectric. The semiconductor may be at least one of: organic, inorganic, hybrids, and mixtures thereof. The floating gate dielectric may be a self-assembled monolayer. The self-

5 assembled monolayer may comprise at least one silane derivative.

The film of organic dielectric material may comprise a self-assembled copolymer. The block copolymer film may be first processed using a simple solvent extraction method to remove any ionic impurities before the synthesis of the nanostructures is carried out

10 in the film.

Brief Description of the Drawings

In order that the invention may be fully understood and readily put into practical effect there shall now be described by way of non-limitative example only exemplary

15 embodiments of the present invention, the description being with reference to the accompanying illustrative drawings.

In the drawings:

Figure 1 is an illustration of a conventional ONO design;

20 Figure 2 is an image of a thin film of gold nano-particles embedded in polystyrene-poly(4-vinyl pyridine) ("PS-P4VP");

Figure 3 is an illustration of an exemplary organic memory device with the self-assembled charge storage layer between organic control and tunnelling layers;

Figure 4 is an illustration of an exemplary organic memory device with the self-

25 assembled layer acting as both the charge storage layer and the control layer, the tunnelling layer being of a different polymeric material;

Figure 5 is an illustration of an exemplary organic memory device with the self-assembled layer acting as the charge storage, the tunnelling layer and the control layer.

Figure 6 is an illustration of an exemplary self-assembled monolayer design;

Figure 7 is an illustration of an exemplary reaction scheme for reduction of gold in PS-

5 P4VP;

Figure 8 is a graph of absorbance of the $\text{PyH}^+\text{AuCl}_4^-$ ions;

Figure 9 is an illustration of capacitance vs voltage of Metal/PS-P4VP /1.4nm SiO_2 /Si substrate before and after annealing at 150°C for 30mins, the gate voltage being swept from -5V to +5V;

10 Figure 10 is an illustration of capacitance vs voltage of Metal/PS-P4VP-Au /1.4nm SiO_2 /Si substrate before and after annealing at 150°C for 30mins, the gate voltage being sweep from -5V to +5V;

Figure 11 is two illustrations of capacitance vs voltage for: (a) Metal/PS-P4VP/4.5nm SiO_2 /Si substrate, and Metal/PS-P4VP-Au/4.5nm SiO_2 /Si substrate; (b) C-
15 V curves of MIS structure with Au nanoparticles at 100 kHz for different gate bias sweeps. The start/stop gate voltage is (A) -2V/+3V, (B) -3V/+4V and (C) -4V/+5V. The hysteresis window for (A) is 1.66V, (B) is 2.75V and (C) is 3.45V;

Figure 12 is an illustration of absorbance vs wavelength of Au nano-particles;

Figure 13: a TEM image of 3-5nm synthesized Au nano-particles;

20 Figure 14 is an AFM image of Au nano-particles deposited on an APTES-modified substrate;

Figure 15 is an illustration of an exemplary MPIS structure;

Figure 16 is a graph of capacitance and conductance vs voltage of a metal/pentacene/Au nano-particles/APTES-modified substrate obtained by sweeping the gate voltage between +5V and -5V;

Figure 17 is a graph of capacitance and conductance vs voltage of a

5 metal/Pentacene/APTES modified substrate obtained by sweeping the gate voltage between +5V and -5V;

Figure 18 is a graph of capacitance and conductance vs voltage of metal/pentacene/Au nano-particles/APTES-modified at 100 KHz for different gate bias sweep ranges; and

Figure 19 is a graph of current vs voltage of a control sample of a
10 metal/pentacene/APTES-modified substrate and with gold nano-particles.

Detailed Description of the Exemplary Embodiments

As shown in Figure 1, present memory devices are based on silicon oxide-silicon nitride-silicon oxide (ONO) where the nitride layer is the charge storage layer. One of
15 the oxide layers acts as the tunneling oxide and the other acts as the control oxide. The nitride layer can be replaced by a nano-structured film. The charge build up occurs in the nanostructures.

As shown in Figures 2 and 3, and according to an exemplary embodiment, there is
20 provided a charge storage film 12 for use in an organic memory device 10 and which has therein nanostructures and/or nano-particles 26. The charge storage film 12 may be, for example, a self-assembled block of a copolymer film such as, for example, PS-P4VP which has therein the nanostructures and/or nano-particles. The self-assembled block copolymers may be linear macromolecules that consist of different blocks (often

incompatible) of different types of monomers. These self-assembled block copolymers can be diblock, triblock or multiblock and may be vinylene-based, methacrylate-based, and/or polyethylene oxide-based monomers.

- 5 As shown in Figure 6, the self-assembled organic film 24 may be self-assembled monolayers. Self-assembled monolayers are the spontaneous organization of molecules, molecular clusters, and aggregate structures into two-dimensional arrays and three-dimensional networks by attractive forces or chemical bond formation. Self-assembled monolayers may be silane derivative molecules.

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The nanostructures and/or nano-particles 30 may have a physical and/or chemical affinity to the self-assembled monolayers 32.

- 15 The nanostructures and/or nano-particles 26 may be embedded in any vinylene-based, methacrylate-based, or polyethylene oxide-based block copolymers that are capable of self-assembly and provide a phase for the reduction of the precursor to nanostructures and/or nano-particles 26.

- 20 The self-assembled organic films 24 may include nanostructures and/or nano-particles 26/30 of metal, ceramic, semiconducting nano-particles, nanoclusters, nanorods, nanofibers, quantum dots such as, but not limited to, gold, silver, copper, titanium dioxide, zinc dioxide, cadmium selenides, cadmium sulphides, fullerene, and fullerene derivatives. The nanostructures and/or nano-particles 26/30 should not be in contact with each other. This means that there can be many charge storage centres and these

centres will not short. The nanostructures and/or nano-particles 26/30 used in block copolymers or self-assembled monolayers may be of any metal, oxide, or semiconductor that has potential to store charges. The charge storage capability can be adjusted by the concentration of the nanostructures in block copolymer film 12 or on the self-assembled monolayers 32.

The device 10 may be a thin film transistor and may have a supporting substrate of glass, plastic, quartz, metal foil, undoped silicon or heavily doped silicon. The device may also include a semiconductor layer that is organic, inorganic, hybrids, or mixtures thereof.

The device 10 is shown in Figure 3 and has a source 14, drain 16 and gate 18. The tunnelling layer 20 and the control layer 22 are both dielectrics and may be formed of an inorganic, organic or plastics dielectric material such as, for example, a polymeric dielectric material such as polyvinyl alcohol ("PVA") or any other polymeric material with a reasonable dielectric constant. The charge storage layer 24 consists of the charge storage film 12 that has electrically isolated nanostructures and/or nano-particles 26. This means that there can be many charge storage centers and these centers will not short due to them being separated by the copolymer film 12. An active layer 28 is used and to which the source 14 and drain 16 electrodes are connected. The active layer 28 is preferably of an organic semiconductor such as, for example, pentacene or polythiophene. The active layer 28 may also act as a supporting substrate.

As shown in Figure 4, the device 10 may have the self-assembled charge storage film 12 with nanostructures and/or nano-particles 26 acting as both the charge storage layer 24 as well as the control layer 22. Alternatively, the self-assembled charge storage film 12 with nanostructures and/or nano-particles 26 can act as both the charge storage layer 24
5 as well as the tunnelling layer 22.

In Figure 5 the self-assembled charge storage film 12 is acting as the charge storage, the control layer 22 as well as the tunnelling layer 20.

10 The charge storage film 24 may be made using one of two different self-assembly methods each of which are able to be used with plastic substrates at temperatures below 100 °C.

In the first method the charge storage film 24 is a self-assembled copolymer film with
15 in-situ synthesized nanostructures and/or nano-particles that may be, for example, spin-coated, screen-printed and/or inkjet-printed onto the film. A single solution may be prepared with both the copolymer thin film and the nanoparticle precursor. Reduction may also be carried out in the solution. The viscosity of the solution may be adjusted for different deposition processes. This provides nano-particles that do not aggregate
20 together and negates the need for the nano-particles to be soluble in the polymer film. This is useable for nanostructures and/or nano-particles of any suitable material such as, for example, gold, silver, aluminium, cobalt, iron-cobalt alloy, and so forth. By using this method, a one step preparation, mixing and deposition process can be used to

prepare the organic charge storing layer 24. The charge storage layer 24 may be manufactured with the control layer 22 and/or tunnelling layer 20 in a one step process.

An organic thin-film transistor (“OTFT”)-based memory device fabrication process uses
5 a self-assembled copolymer composite film as a floating gate dielectric layer for memory applications by in-situ synthesis of nanostructures and/or nano-particles embedded in the self-assembled copolymer composite film. In an exemplary embodiment:

- The control layer 22 of a material such as, for example, polyvinyl alcohol, is spin
10 coated on the gate electrode 18. The gate electrode 18 is of any suitable material such as, for example, gold.
- The memory layer 24 consisting of the nanostructures and/or nano-particles is then spin coated on the control layer 22.
- The tunnelling layer 20 of a material such as, for example, polyvinyl alcohol, is
15 then spin coated on the memory layer 24.
- The active layer 28 of an organic semiconductor such as, for example, pentacene or polythiophene is applied to the tunnelling layer 20 by one or more of: thermal evaporation, spin-coating, and being printed.
- The source 14 and drain 16 are then generated by using patterning.

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The second method is illustrated in Figure 6. Here, nanostructures 30 are manufactured that are held by layers 32 and 34 of self-assembled monolayers (“SAM”s). In one exemplary form of the method, the oxide layers of Figure 1 are replaced by layers 32 and 34 of the self-assembled monolayer. The nanostructures 30 have an affinity to the

self-assembled monolayers 32, 34 and are deposited on the first layer 32. The other layer 34 of self-assembled monolayer is then deposited on the nanostructures 30. The active region 28 is then applied. If required or desired, layer 34 may be deleted.

5 Figure 7 shows the reduction scheme for the synthesis of a self-assembled copolymer composite film as a floating gate dielectric layer for memory applications. Nano-particles are synthesized in-situ in copolymeric solution and the film is then deposited as the active layer in an organic memory device. The nanoparticle precursors are incorporated in the copolymer solution and the reduction of the precursor to
10 nanoparticles is carried out in the solution. Following that, the film is cast on a thin oxide layer to form the active layer for one of:

charge storage,

both charge storage and control dielectric, or

charge storage and both the control and tunneling dielectric.

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This method of preparing the active layer reduces the need to modify the surface of the nano-particles prior to mixing with the polymer so the particles will not aggregate together. Aggregation of the particles could result in shorting between the particles. The organic memory device will be highly flexible and shorting of nano-particles
20 should not occur, even when bent. This method can be performed at temperatures below 100°C.

The exemplary method for the in-situ synthesis of the self-assembled copolymer film comprises:

- Polystyrene-Poly(4-vinyl pyridine) (PS-P4VP) diblock copolymer was first dissolved in toluene and a solvent extraction process is implanted to remove any ionic impurities. This is done by washing the PS-P4VP solution in water. The water phase is then removed and the toluene phase containing the PS-P4VP can now be precipitated from Hexane. The PS-P4VP is re-dissolved in toluene (concentration being in the range of 1-10 mg/mL, preferably being 5mg/mL)
- A stoichiometric equivalent of tetrachloroauric acid was added to the micellar solution with the ratio HAuCl_4 :4-VP being in the range of 1:20 to 1:1, preferably being 1:5. Protonation of the 4-VP units resulted in the formation of a poly-ionic block.
- The solution was then treated with hydrazine monohydrate. Because of its polar character, in the core of the micelles the hydrazine is preferentially taken up where it reduces Au^{3+} to Au^0 . The excess of hydrazine (if any) was removed directly after reduction by adding aqueous hydrochloric acid.
- Neutralization of the excess hydrazine and precipitation of $\text{N}_2\text{H}_5\text{Cl}$ assists in the long-term stability of the colloidal dispersion. The precipitated hydrazinium chloride was removed by centrifuging.

The copolymer solution comprising the charge storage layer 24, a control layer 22 and the tunnelling layer 20, may be applied to a p-type silicon substrate (as gate 18) by spin coating at a speed in the range 500 to 6000rpm, preferably 2000 rpm for a period of time on the range 10 to 120seconds, preferably 60seconds. After spin-coating, the copolymer film may be annealed at the range of 100-200 °C, preferably at 150°C in a vacuum. The annealing time is in the range of 30 minutes to 72 hours, preferably for 72

hours. After the deposition of copolymer film which comprise the nanostructures and/or nanoparticles 26 of gold, the active layer 28, source 14 and drain 16 were formed by subsequent thermal evaporation. Figure 3 is a schematic illustration of the device structure.

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As shown in Figure 8, there is a shift in the absorption spectrum with the reduction of the Au precursor. The absorbance (curve a) of the $\text{PyH}^+\text{AuCl}_4^-$ ions vanished almost instantaneously. The absorption band at 525 nm is characteristic of the surface plasmon resonance of the small Au nanocrystals that appear (curve b).

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A metal-insulator-semiconductor ("MIS") heterostructure after annealing was fabricated to investigate the charging effect. A p-type silicon substrate is used with a thermally grown 1.4nm silicon dioxide on top. The block copolymer is spin-coated on top, followed by deposition of the top gold electrode by thermal evaporation through a shadow mask of 300 μm diameter size. The annealing temperature for the copolymer film used is above the glass transition temperature of the block copolymer (110-150 $^\circ\text{C}$) for at least 30 minutes.

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The capacitance-voltage (C-V) measurements were obtained using an HP 4284A Precision LCR Meter at a frequency ranging from 1kHz to 1MHz. Figure 9 shows the C-V measurements at a frequency of 1 MHz. An amplitude of 15 mV was superimposed on the DC bias. All experiments were carried out at room temperature and in ambient environment.

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There is a negative flat-band voltage shift (ΔV_{FB}) after annealing of the copolymer film. This indicates that there is less electron trapping in the annealed film. Hence, there is a possibility of reducing the defects, and charge trapping sites, in the copolymer film by the annealing process. The decrease in capacitance in the accumulation takes place as

5 the process of annealing has reduced the number of charge-trapping sites and thus the tunnelling path through the charge-trapping sites will be limited. Hence, the total capacitance decreases. The polar portion of the micelle (P4VP core) will contract upon annealing. With the smaller extension of the polar portion, there will be reduction of charge density (i.e. weaker electrostatic repulsions) around the P4VP core. This will

10 mean a smaller hysteresis loop (fewer electrons or holes will be induced in the MIS structure) or shift in the flat-band voltage. But it is also possible that the difference in capacitance in the accumulation regime between the non-annealed and annealed samples is due to the difference in the dielectric constants of the non-annealed and annealed copolymer.

15

The stability of the micelles is enhanced upon the loading of Au nanoparticles, since the polar portion is converted to an ionomer block. The result of this is shown in Figure 10, where there is little or negligible flat-band voltage change for PS-P4VP-Au before and after annealing.

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Figure 11 (a) shows the capacitance-voltage of the MIS structure using PS-P4VP as the dielectric layer at 100 kHz on MIS structures with and without Au nano-particles. The MIS structure is using a n-type silicon substrate with a 4.5nm silicon dioxide on top. The active layer is then spin-coated on top, followed by deposition of the top gold

electrode by thermal evaporation through a shadow mask of 300 μm diameter size. For the curve without Au nano-particles, there is negligible hysteresis observed indicating absence of trapped charges in the fabricated structure. The hysteresis is defined to be the flat band voltage shift.

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Figure 11 (b) shows the capacitance-voltage curves of the MIS structure with Au nano-particles at 100 kHz for different gate bias sweeps. The start/stop gate voltage is (A) - 2V/+3V, (B) -3V/+4V and (C) -4V/+5V. The hysteresis window for (A) is 1.66V, (B) is 2.75V and (C) is 3.45V.

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An anticlockwise hysteresis window in a range of 0.4 to 3.45V is observed for the sample with Au nanoparticles, depending on the range of operating voltage used, indicating a net hole trapping effect. The higher the operating voltage, the bigger is the hysteresis window. At the influence of negative gate voltage (applied from top metal electrode), holes may be injected from the substrate inversion layer and may be stored in the Au nanoparticles by a direct tunnelling process through the ultra thin oxide. When the voltage is swept to positive value, the stored holes in the Au nanoparticles will be flushed out, resulting in the shift in capacitance characteristics.

20

A higher concentration of Au nanoparticles in the self-assembled copolymer film may result in a better charge storage capability. Hence the concentration of noble particles may control the charge storage ability of the organic memory.

Another exemplary process for the fabrication of OTFT-based memory devices with self-assembled monolayers and nanostructures as a floating gate dielectric layer may be implemented by:

- Depositing a self-assembled monolayer 32 on a substrate.
- 5 • Depositing nanostructures 30 with an affinity to the self-assembled monolayer 32 on the self-assembled monolayer 32.
- Depositing another layer of the self-assembled monolayer 34 on the nanostructures 30.
- The organic semiconductor layer 28, such as pentacene or polythiophene, is
10 applied to the other layer 34 of the self-assembled monolayer by at least one of: thermal evaporation, spin-coating, and being printed on the self-assembled monolayer.
- The source 14 and drain 16 for the organic memory is then deposited on the semiconductor layer 28.

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The synthesis of gold nano-particles may be carried out by the use of a modified Turkevich method which used trisodium citrate ($\text{Na}_3\text{C}_6\text{H}_5\text{O}_7 \cdot 2\text{H}_2\text{O}$) as the stabilising agent and sodium borohydride (NaBH_4) as the reducing agent. In an exemplary form, 0.5 ml of 0.01M hydrogen tetrachloroaurate (III) ($\text{HAuCl}_4 \cdot 3\text{H}_2\text{O}$) was mixed with 0.5
20 ml of 0.01M trisodium citrate. The mole ratio of $\text{HAuCl}_4 \cdot 3\text{H}_2\text{O}$ to $\text{Na}_3\text{C}_6\text{H}_5\text{O}_7 \cdot 2\text{H}_2\text{O}$ was 1:1. The solution was diluted with 18 ml of deionised water and stirred. 0.5 ml of 0.1M NaBH_4 aqueous solution was added drop-by-drop and the solution was stirred for 30 seconds. The solution was left undisturbed for two hours.

As shown in Figure 12, the Au nano-particles were characterized using UV-Vis and showed a peak at approximately 509.4 nm due to the presence of spherical Au nanoparticles, produced by the reduction of HAuCl_4 using sodium borohydride as the reducing agent. The size of the Au nanoparticles can be determined from the TEM
5 image of Figure 13. Droplets of the gold colloids were dropped onto a copper grid with holey carbon film and dried in vacuum. Figure 13 shows monodispersed Au nanoparticles of approximately 3-5 nm in diameter.

For the removal of possible organic contaminants from the substrate as well as the
10 glassware used for solution deposition, piranha solution (2:1 concentrated H_2SO_4 : 30% H_2O_2) was employed, followed by RCA clean ($\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:1:10$ and $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:1:5$). After the RCA clean, the silicon substrate surface is rich in hydroxyl groups, which are used to link the 3-aminopropyl-triethoxysilane ("APTES") molecules. The amino-terminating APTES self-assembled monolayer was formed on a
15 silicon surface by immersing the silicon substrate in 5-10 % volume of APTES in absolute ethanol for 1-2 hour. The modified substrate was then rinsed successively in ethanol and deionized water to remove any loosely bound molecules and blow dried with nitrogen gas. Finally, the substrates were baked in vacuum oven at 120°C for 30 – 60 minutes to complete the Si-O bond formation.

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A monolayer of amino-substituted silane on the silicon was confirmed by ellipsometry, which revealed a film thickness of 0.9 nm. The thickness of the SiO_2 layer was measured separately on an unmodified substrate first and subtracted from the total layer

thickness determined for the APTES monolayer-covered SiO₂/Si substrate. The difference in thickness yields the thickness of the APTES layer.

The gold nano-particles were assembled on the amino-terminated silicon substrate surface by immersing the substrates into a colloidal solution of gold nano-particles for 5 6-12 hours. The pH of the gold colloid solution was adjusted to around 5-6. Since the solution of the gold nano-particles was slightly acidic, adding this solution to the amino-silylated substrates led to the protonation of the amino groups on the surface. Such positively charged substrate surfaces enabled electrostatic attraction of negatively 10 charged citrate-stabilized gold nanoparticles. The substrates were removed from the solution, rinsed with deionised water and blow dried with nitrogen gas. The AFM image of Figure 14 shows a densely-packed layer of gold nano-particles.

A metal-pentacene-insulator-silicon ("MPIS") structure is shown in Figure 15, where 15 pentacene is the active semiconductor layer 28. The n-type silicon substrate 36 is used as the gate electrode 18, with 4.5-nm thermally grown silicon dioxide 38 above it. The gold nano-particle layer 30 was deposited on the SiO₂ layer 38 at room temperature and pressure by chemical self-assembly. The pentacene layer 28 is thermally evaporated, at a deposition rate between 0.1 – 0.5 nm/s and a pressure of around 10⁻⁶ -10⁻⁷ torr, to form 20 a 45±5-nm-thick film. The top metal electrode 40 of gold was subsequently deposited by thermal evaporation through a shadow mask of 300 µm diameter size.

The capacitance-voltage measurements were at a frequency range of 1 kHz - 1 MHz and an amplitude of 15 mV was superimposed on the DC bias. All measurements were carried out at room temperature and in vacuum environment ($\sim 10^{-3}$ - 10^{-4} torr).

- 5 Figure 16 shows the capacitance-voltage and conductance-voltage characteristics (frequency of 100 kHz is used) of the MPIS structure with deposited gold nanoparticles, where the conductance peak corresponds to the flat-band voltage. The conductance peak may be associated with energy loss due to the capture and emission of electrons by the gold nano-particles or the pentacene/gold nano-particle interface; but not to the
- 10 pentacene/APTES interface states. This is from a comparison with the observation of the control sample without gold nano-particles of Figure 17 as it has no conductance peak.

As shown in Figure 16, a clockwise hysteresis window of 1.25V occurs upon double

15 sweeping. This indicates a net hole trapping. Under the influence of a negative gate voltage, holes can be injected into the gold nano-particles from the pentacene accumulation layer. Most of the holes that are injected into the conduction band of the gold nano-particles are collected by the gate or the substrate, leading to a gate current or a substrate current, respectively. Upon applying a positive gate voltage, the stored

20 charges in the gold nanoparticles are forced out, resulting in flat-band voltage shift. Both the magnitude of hysteresis in capacitance-voltage and the shift in the peak positions in conductance-voltage are about 1.25V. The single conductance peak observed in two directions means that only single-electron or single-hole trapping and de-trapping events were observed. As such the peak in conductance around the flat band

condition indicates that a trap event had occurred where an electron or hole is stored per gold nanoparticle. Therefore, these hysteresis and peak shifts may be attributed to holes trapped in the sandwiched gold nano-particles or at the interface of the gold nano-particles. States at the APTES or at the APTES-oxide interface may not be responsible
5 for such behaviour.

Figure 18 shows that the increment of the maximum operation bias from 5V to 10V increases the hysteresis window of the C-V curve from 1.25 V to 2.05V. This indicates that more and more holes are being trapped by increasing the gate voltage.
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As shown in Figure 19, lower current through the whole device is observed for the sample with Au nanoparticles. The current obtained from the control sample (pentacene/APTES/SiO₂) was at least two orders of magnitude higher. This might be due to charges being stored inside the Au nanoparticles and “screens” the effective
15 electric gate field, resulting in lower effective voltage applied and hence, lower current. During voltage sweeping from 0 to -4.5V, the applied electric field can cause charging and discharging of some Au nanoparticles, leading to the breaking or formation of some conductive paths and thus decrease or increase of current respectively.

20 The memory device 10 may be a non-volatile memory device that can be repeatedly written, read and erased having at least one of: low operating voltage (e.g. less than 10V), current ratio between the on and off state of at least two orders in magnitude, a low processing temperature from about 50 °C to about 225 °C, and a switching speed in the range of 100µs – 100ns.

Whilst there has been described in the foregoing description exemplary embodiments of the present invention, it will be understood by those skilled in the technology concerned that many variations in details of design, construction and/or operation may be made

5 without departing from the present invention.

The Claims:

1. An organic memory device comprising: an active layer; at least one charge storage layer comprising a film of an organic dielectric material, and nanostructures and/or nano-particles of a charge-storing material on or in the film of dielectric material, each of the nanostructures and/or nano-particles being separated from the others of the nanostructures and/or nano-particles by the organic dielectric material of the organic dielectric film.
2. An organic memory device as claimed in claim 1 further comprising a tunnelling layer on a first side of the at least one charge storage layer, and a control layer on a second side of the charge storage layer, the first side being opposite the second side.
3. An organic memory device as claimed in claim 2, wherein the control layer is integral with the at least one charge storage layer.
4. An organic memory device as claimed in claim 2 or claim 3, wherein the tunnelling layer is integral with the at least one charge storage layer.
5. An organic memory device as claimed in any one of claims 1 to 4, wherein each of the nanostructures and/or nano-particles is electrically isolated.
6. An organic memory device as claimed in any one of claims 1 to 5, wherein the at least one charge storage layer comprises a single layer with the nanostructures and/or nano-particles being within the single layer.
7. An organic memory device as claimed in any one of claims 1 to 5, wherein the at least one charge storage layer comprises at least two layers with the nanostructures and/or nano-particles being between the two layers.

8. An organic memory device as claimed in any one of claims 1 to 7, wherein the film of organic dielectric material comprises a self-assembled copolymer selected from the group consisting of: diblock, triblock, and multiblock.
9. An organic memory device as claimed in claim 8, wherein the self-assembled
5 copolymer is of a material selected from the group consisting of: vinylene-based, methacrylate-based, and polyethylene oxide-based monomers.
10. An organic memory device as claimed in any one of claims 1 to 7, wherein the film of organic dielectric material comprises a self-assembled monolayer.
11. An organic memory device as claimed in claim 10, wherein the self-assembled
10 monolayer comprises silane derivatives.
12. An organic memory device as claimed in claim 10 or claim 11, wherein the nanostructures and/or nano-particles have an affinity with the self-assembled copolymer or self-assembled monolayer, the affinity being at least one selected from the group consisting of: physical, and chemical.
13. An organic memory device as claimed in any one of claims 1 to 12, wherein the
15 nanostructures and/or nano-particles are at least one selected from the group consisting of: metal, oxide of a metal, semiconductor, ceramic, semiconducting nano-particles, nanoclusters, nanorods, nanofibers, quantum dots, fullerene, and derivatives of fullerene.
14. An organic memory device as claimed in claim 13, wherein the quantum dots
20 are selected from the group consisting of: gold, silver, copper, titanium dioxide, zinc dioxide, cadmium selenides, and cadmium sulphides.
15. An organic memory device as claimed in any one of claims 1 to 14, wherein a charge storage capability is able to be adjusted by adjusting a concentration of

the nanostructures and/or nano-particles on or in the film of an organic dielectric material.

16. An organic memory device as claimed in any one of claims 1 to 15, wherein the organic memory device comprises a thin film transistor, the thin film transistor further comprising a source electrode, a drain electrode, and a gate electrode.
17. An organic memory device as claimed in claim 16, wherein the active layer comprises a semiconductor; and the thin film transistor further comprises a supporting substrate selected from the group consisting of: glass, plastic, quartz, metal foil, undoped silicon and heavily doped silicon.
18. An organic memory device as claimed in any one of claims 2 to 4, or any one of claims 5 to 17 when dependent on any one of claims 2 to 4, wherein the tunnelling layer and control layer comprise a floating gate dielectric, the floating gate dielectric comprising one of: dielectrics, and a copolymer-based dielectric.
19. An organic memory device as claimed in claim 17, or claim 18 when dependent on claim 17, wherein the semiconductor is at least one selected from the group consisting of: organic, inorganic, hybrids, and mixtures thereof.
20. An organic memory device as claimed in claim 18, wherein the floating gate dielectric is a self-assembled monolayer comprising at least one silane derivative.
21. An organic memory device as claimed in any one of claims 1 to 7, wherein the film of organic dielectric material comprises a self-assembled copolymer, the block copolymer film being first processed using a simple solvent extraction method to remove any ionic impurities before the synthesis of the nanostructures is carried out in the film.
22. A method for the fabrication of an organic memory device, the method comprising forming a control layer on a gate electrode, forming a charge storage

layer including nanostructures and/or nano-particles on the control layer,
forming a tunnelling layer on the charge storage layer, and forming an active
layer on the tunnelling layer.

23. A method as claimed in claim 22, wherein the control layer is formed integrally
5 with the charge storage layer.

24. A method as claimed in claim 22 or claim 23, wherein the tunnelling layer is
formed integrally with the charge storage layer.

25. A method as claimed in any one of claims 22 to 24, wherein the charge storage
layer comprises a self-assembled copolymer film and the nanostructures and/or
10 nano-particles.

26. A method as claimed in claim 25, wherein the nanostructures and/or nano-
particles are formed on the film by at least one selected from the group
consisting of: spin-coating, screen-printing, and inkjet-printing.

27. A method as claimed in any one of claims 22 to 24, wherein the charge storage
15 layer including nanostructures and/or nano-particles is prepared in a single
solution for a self-assembled copolymer film and a precursor for the
nanostructures and/or nano-particles.

28. A method as claimed in claim 27 further comprising performing a reduction in
the single solution; and adjusting a viscosity of the solution for different
20 deposition processes.

29. A method as claimed in claim 27 or claim 28, wherein the single solution is cast
on a thin oxide layer to form the charge storage layer.

30. A method as claimed in any one of claims 22 to 24, wherein the control layer
and the tunnelling layer both comprise a self-assembled monolayer; the

nanostructures and/or nano-particles being formed between the two layers of self-assembled monolayer.

31. A method as claimed in claim 30, wherein the nanostructures and/or nano-particles have an affinity to the self-assembled monolayers, the affinity being at least one of: physical, and chemical.
32. A method as claimed in claim 30 or claim 31, wherein the nanostructures and/or nano-particles are deposited on a first of the two layers of self-assembled monolayer and the other of the two layers of self-assembled monolayer then being deposited on the nanostructures and/or nano-particles.
33. A method as claimed in any one of claims 22 to 32, wherein each of the nanostructures and/or nano-particles is electrically isolated.
34. A method as claimed in any one of claims 22 to 33, wherein the charge storage layer comprises a single layer with the nanostructures and/or nano-particles being within the single layer.
35. A method as claimed in any one of claims 22 to 34, wherein the charge storage layer comprises two layers with the nanostructures and/or nano-particles being formed between the two layers.
36. A method as claimed in any one of claims 25 to 28, wherein the self-assembled copolymer is selected from the group consisting of: diblock, triblock, and multiblock.
37. A method as claimed in any one of claims 25 to 28 or claim 36, wherein the self-assembled copolymer is of a material selected from the group consisting of: vinylene-based, methacrylate-based, and polyethylene oxide-based monomers.

38. An organic memory device as claimed in any one of claims 25 to 28, 36 or 37, wherein the nanostructures and/or nano-particles have an affinity with the self-assembled copolymer, the affinity being at least one selected from the group consisting of: physical, and chemical.
- 5 39. A method as claimed in any one of claims 22 to 38, wherein the nanostructures and/or nano-particles are at least one selected from the group consisting of: metal, oxide of a metal, semiconductor, ceramic, semiconducting nano-particles, nanoclusters, nanorods, nanofibers, quantum dots, fullerene, and derivatives of fullerene.
- 10 40. A method as claimed in claim 39, wherein the quantum dots are selected from the group consisting of: gold, silver, copper, titanium dioxide, zinc dioxide, cadmium selenides, and cadmium sulphides.
41. A method as claimed in any one of claims 25 to 28, wherein a charge storage capability is able to be adjusted by adjusting a concentration of the
- 15 nanostructures and/or nano-particles in the single solution.
42. A method as claimed in any one of claims 22 to 41, wherein the organic memory device comprises a thin film transistor, the thin film transistor further comprising a source electrode, a drain electrode, and a gate electrode.
43. A method as claimed in claim 42, wherein the active layer comprises a
- 20 semiconductor; and the thin film transistor further comprises a supporting substrate selected from the group consisting of: glass, plastic, quartz, metal foil, undoped silicon and heavily doped silicon.

44. A method as claimed in any one of claims 23 to 25, wherein the tunnelling layer and control layer comprise a floating gate dielectric, the floating gate dielectric comprising one of: dielectrics, and a copolymer-based dielectric.
- 5 45. A method as claimed in claim 43, wherein the semiconductor is at least one selected from the group consisting of: organic, inorganic, hybrids, and mixtures thereof.
46. A method as claimed in claim 45, wherein the floating gate dielectric is a self-assembled monolayer.
- 10 47. A method as claimed in claim 46, wherein the self-assembled monolayer comprises at least one silane derivative.
- 15 48. A method as claimed in any one of claims 22 to 28, wherein the film of organic dielectric material comprises a self-assembled copolymer, the block copolymer film being first processed using a simple solvent extraction method to remove any ionic impurities before the synthesis of the nanostructures is carried out in the film.