

PATENT SPECIFICATION

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(54) COMPENSATION MEANS IN COMBINATION WITH A PULSE GENERATOR CIRCUIT UTILISING FIELD EFFECT TRANSISTORS

(71) We, HITACHI LIMITED of 4, 1-chome, Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to a combined pulse generator circuit and compensation means utilising field effect transistors.

In present day technology recent improvements have been made for incorporating all of the circuit elements which are necessary for small-sized calculators into a single semiconductor chip. A clock pulse generator constructed as above consists of three inverters connected in a closed loop, with capacitors connected therebetween, and has been disclosed in Patent Application No. 22,976/74 (Serial No. 1,475,724).

One of the problems associated with the above mentioned electronic circuitry is instability due to changes in ambient temperature and the voltage supply. Moreover, when uncompensated electronic circuits are manufactured in MOSIC structure, the oscillation period amongst the various such MOSICs vary over a wide range due to the differences in the characteristics of the respective circuits.

Therefore, such a circuit requires compensation means to prevent this instability, and also to compensate for the differences of the oscillation period amongst mass-produced pulse generator MOSICs.

It is an object of the present invention to provide a compensation circuit in combination with, to compensate for instability in the electrical characteristics of, a MOSIC pulse generator circuit, due to changes in ambient temperature.

It is another object to provide a

compensation circuit in combination with compensating for the instability of the electric characteristics of, a MOSIC pulse generator circuit, due to changes in voltage supply.

It is a further object to provide a compensation circuit in combination with a MOSIC pulse generator circuit which compensates for differences in the electric characteristics which may be distributed over a wide range amongst mass-produced MOSIC pulse generators.

According to one aspect of the present invention there is provided the combination of a pulse generator circuit and compensation means; said pulse generator circuit comprising first, second and third insulated gate field effect transistors, the drain electrode of the first transistor being coupled to the gate electrode of the second transistor, the drain electrode of the second transistor being coupled to the gate electrode of the third transistor, the drain electrode of the third transistor being coupled to the gate electrode of the first transistor, the source electrodes of the first, second and third transistors being connected to a first voltage source; fourth, fifth and sixth insulated gate field effect transistors, the source electrodes of the fourth, fifth and sixth transistors being connected to the drain electrodes of the first, second and third transistors, respectively, the drain electrodes of the fourth, fifth and sixth transistors being connected to a second voltage source, the gate electrodes of the fourth and fifth transistors being connected in common; said compensation means including a seventh field effect transistor, the source electrode of the seventh transistor being connected to said first voltage source, the drain electrode of the seventh transistor being connected to the commonly connected gate electrodes of said fourth and fifth transistors; the gate electrode of the

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seventh transistor being connected to a biasing potential, and a resistor connected between the drain electrode of said seventh transistor and said second voltage source.

The present invention will now be described in greater detail by way of example, with reference to the accompanying drawings, wherein:—

Figure 1 is a basic circuit arrangement in which the compensation circuit employs a single MOSFET and resistor;

Figures 2 to 4 are circuit diagrams showing modifications of the circuit in Figure 1 with respect to the electrode connections of the compensating MOSFET;

Figure 5 is a basic circuit arrangement employing a pair of parallel connected IGFETs in the compensating circuit;

Figure 6 is a circuit diagram showing a pulse generator circuit in combination with compensation means according to the present invention; and

Figure 7 shows three waveforms (a) to (c) which assist in explaining the operation of the pulse generator circuit portion of Figure 6.

Referring to Figure 1, the compensation circuit includes a resistor 4 having a resistance in the range of 50 Kohms to 100 Kohms, and a MOSFET 3 connected in series, these being connected between a power supply voltage VGG and earth. The junction point of the resistor 4 and the MOSFET 3 is connected to the gate electrode of a MOSFET 1, which, together with a MOSFET 2 connected in series, forms an inverter circuit. The gate electrode of the MOSFET 3 is supplied with a fixed bias voltage.

When the ambient temperature of the circuit increases, the current flowing through the MOSFET 1 (assuming constant gate voltage) decreases, since the threshold voltage V_{th} of the MOSFET 1 increases. However, the current flowing through the MOSFET 3 decreases, therefore, the voltage drop across the resistor 4 decreases. In other words, the voltage V applied to the gate electrode of the MOSFET 1 increases. This increase in the gate electrode voltage causes an increase in the current flowing through the MOSFET 1. Therefore, compensation for changes in the electrical characteristics, due to temperature effects, of the inverter circuit containing the MOSFETs 1 and 2 will be effected.

Referring to Figure 2, the MOSFET 3 is of the enhancement type, and its gate electrode is connected to the power supply voltage VGG. This compensates for changes both in the ambient temperature and the supply voltage. More specifically, when the supply voltage VGG increases, the voltage V supplied to the gate electrode

of the MOSFET 1 would increase in the absence of compensation. However, the voltage applied to the gate electrode of the MOSFET 3 increases, causing an increase in the current flowing through the resistor 4. Thus, the voltage drop across the resistor 4 increases, causing a compensating decrease in the voltage V supplied to the gate electrode of the MOSFET 1. As a result, the voltage V is constant at a certain value irrespective of changes in the power supply voltage. In this case, if the MOSFET 3 is manufactured in the same MOSIC under the same conditions as the MOSFET 1, the compensation circuitry will compensate for differences in the electrical characteristics amongst the MOSICs, which would be present in the absence of compensation.

Referring to Figure 3, the MOSFET 3 in this embodiment is a depletion type MOSFET and has its gate electrode connected to earth, rather than to the power supply voltage VGG. This embodiment compensates for changes in the electrical characteristics of the circuit in response to changes in the ambient temperature, and also for differences in the electrical characteristics amongst a plurality of MOSICS when the MOSFET 3 is manufactured under the same conditions as the MOSFET 1 in the same MOSIC.

In this embodiment however, the resistor 4 should have a temperature coefficient much smaller than those of MOSFETs 1 and 3 and, for the resistance 4, a resistor of a high, constant or linear resistance value, manufactured separately from the MOSIC, may be employed.

In both embodiments shown in Figures 2 and 3, compensation may be made for differences in the electrical characteristics of the various mass-produced MOSICS. For example, if the threshold voltage V_{th} of the MOSFET 1 in a MOSIC is high, the threshold voltage V_{th} of the MOSFET 3 in the MOSIC will also be high, which means that the current flowing through the MOSFET 3 is relatively small. This means that the voltage V will increase since the voltage drop across the resistor 4 is small; as a result, a decrease in the current flowing through the MOSFET 1, due to a high threshold voltage V_{th} of the MOSFET will be compensated by an increase in the bias voltage V.

Furthermore, since compensation for variation in the electrical characteristics of MOSIC circuits may be effected as described above, the above compensating circuits, in accordance with the present invention are employed in combination with pulse generator circuits to provide a stable oscillation frequency thereof.

Moreover, since the differences in the electrical characteristics for a plurality of mass-produced MOSICS, i.e. those without compensation, will be compensated by the above described compensating circuitry, when the compensating circuit is used in a pulse generator MOSIC, the oscillation periods thereof will vary only within a small range, so that substantially uniform pulse generator MOSIC circuitry can be mass-produced.

A number of modifications of basic circuit design are possible; the most important of which are briefly discussed below:—

Referring to Figure 4, the gate electrode of the MOSFET 3 is connected between the junction of the resistor 4 and the gate electrode of the MOSFET 1.

When the MOSFET 1 is of the depletion type, a pair of IGFETs may be employed in the compensation circuit, as shown in Figure 5. An enhancement type IGFET 5 is connected in back-to-back parallel relationship with a depletion type IGFET 6. The gate electrode of the IGFET 6 is connected to earth, whilst the gate electrode of the IGFET 5 is connected to the power supply voltage VGG.

The use of compensating circuitry in a practical embodiment of a pulse generator in combination with a compensation circuit, in accordance with the present invention, which may be employed in small-sized electronic calculators, will now be described with reference to Figures 6 and 7.

Referring to Figure 6 within the boundary of the chain lines are the pulse generator circuit 22 and the compensating circuit 23 connected thereto.

The pulse generator circuit 22 includes a plurality of p-channel enhancement type insulated gate field effect transistors 11, 13 and 15. The compensating circuit 23 comprises a P-channel enhancement type insulated gate field effect transistor 19, connected in back-to-back relationship with an insulated gate field effect transistor (IGFET) 20 and a high valued resistor 21, e.g. 50 Kohms, connected between the power supply voltage VGG and the parallel pair of transistors of the compensating circuit.

Connected between the respective transistors 11—13 and 13—15 and earth are capacitors 17 and 18 which have a value of 0.1 to 10pF, for example. IGFETs 12, 14 and 16 constitute load transistors for the respective IGFETs 11, 13 and 15 and have their gate electrodes connected in common to the junction of the resistor 21 and the MOSFET pair 19—20.

All of the IGFETs shown in Figure 6 are formed in the same semiconductor chip of

monocrystalline silicon, whilst the resistor 21 and the capacitors 17 and 18 are connected externally to the MOSIC.

The respective inverters 11—12, 13—14 and 15—16 are connected to form a closed loop, the source electrodes of the IGFETs 19, 20, 11, 13 and 15 the capacitors 17 and 18, and the gate electrode of the transistor 20 are connected to earth, whilst the gate electrode of the transistor 19 and the drain electrodes of the transistors 12, 14 and 16 are connected to the supply voltage VGG. The output O of the pulse generator circuit 22 is taken from the drain electrode of the transistor 15.

Referring now to Figure 7, the operation of the circuit of Figure 6 will be explained in greater detail, with reference to the three waveforms (a) to (c).

It is assumed, for explanatory purposes, that during the period of time t_1 , the IGFET 15 is conductive and voltage having a lower absolute value than the threshold level of the IGFET 11 is present at junction c, which is connected to the output terminal OUT. In the meantime, the IGFET 13 is cut-off and the capacitor 18 is being charged by current flowing through the IGFET 14. During the same period of time t_1 , the capacitor 17 is being charged, since the IGFET 11 is cut-off.

Under these conditions, when the output voltage of the first inverter circuit at point a (the drain electrode of the IGFET 11) attains a larger absolute value than the threshold voltage level of the IGFET 13, initiating the period of time t_2 as shown in waveform (a), the IGFET 13 starts conducting. Then, the charge which is stored in capacitor 18 commences to be discharged through the IGFET 13.

Subsequently, when the output voltage of the second inverter circuit b (the drain electrode of the IGFET 13) reaches a smaller absolute value than of the threshold voltage level of the IGFET 15, as shown in waveform (b), initiating the period of time t_3 the IGFET 15 becomes nonconductive. The voltage change at the output of the third inverter circuit (the drain electrode of the IGFET 15) or at the output terminal OUT is rapid during this time, since the output of the IGFET 15 is not connected to a large valued capacitor. As a result, the output voltage at the point c of the IGFET 15 attains a larger absolute value than the threshold voltage level of the IGFET 11, as shown in Figure 7c, initiating period of time t_4 , therefore the IGFET 11 conducts.

When the output voltage at the point a of the IGFET 11 becomes smaller than the threshold voltage level of the IGFET 13, initiating the period of time t_5 , the IGFET 13 is cut-off, whilst the IGFET 15 is

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unaffected. When the output voltage at the point *b* of the IGFET 13 becomes larger than the threshold voltage level of the IGFET 15, initiating the period of time *t*₆, the IGFET 15 becomes conductive, so that the output voltage at the point *c* rapidly changes its state to substantially earth potential. When the output voltage at the point *c* of the IGFET 15 becomes smaller than the threshold level of the IGFET 11, initiating the period of time *t*₇, the IGFET 11 is cut-off and the voltage output at point *a* gradually increases. Subsequently, the same operations as described above are repeated for the operation of the pulse generator 22. The output voltage of the pulse generator 22 at terminal O is shown in waveform (c).

However, the oscillation period of the pulse generator circuit 22 changes with the change in ambient temperature and power supply voltage. Moreover, MOSICs which are manufactured to include such a pulse generator circuit will have different oscillation periods due to differences in the circuit constants of respective IGFETs which make up the MOSICs. In order to overcome these difficulties a compensating circuit 23 is provided, as described previously. Since the MOSFET 20, which is connected in back-to-back parallel relationship with IGFET 19, is manufactured in accordance with the same conditions as the IGFETs 12, 14 and 16, the IGFET 20 will have the same threshold voltage *V*_{th} thereof.

When the ambient temperature of the pulse generator circuit 22 increases, the current which flows through the IGFETs 12 and 14 decreases, resulting in an increase in the time which is required to charge the capacitors 17 and 18. As a result, the mark space ratio or the period of the pulse generator increases, unless something is done to compensate for this condition.

In accordance with the present invention, however, because of the compensation circuit 23, the current flowing through the IGFETs 19 and 20 also decreases when the ambient temperature increases. Then, since the voltage drop across the resistor 21 decreases, the voltage which is applied to the gate electrodes of the IGFETs 12 and 14 increases so as to increase the current flowing therethrough. As a result, what would have been a decrease in the duty ratio or the oscillation period is nullified.

Similarly, when the power supply voltage *V*_{GG} increases, the current flowing through the respective IGFETs 12 and 14 increases. However, this increase is compensated by an increase in the voltage drop across the resistor 21, since the current flowing through the IGFET 19 will

also increase. As a result, compensation for changes in the supply voltage are effected.

It can be seen, therefore, that the present invention provides compensation for changes in ambient temperature, supply voltage and differences in the electrical characteristics of respective IGFETs making up differently manufactured MOSIC pulse generators under the same operating conditions, since the transistors of the compensating circuit are manufactured under the same production conditions as the IGFETs making up the pulse generator circuit.

WHAT WE CLAIM IS:—

1. In combination, a pulse generator circuit and compensation means: said pulse generator circuit comprising first, second and third insulated gate field effect transistors, the drain electrode of the first transistor being coupled to the gate electrode of the second transistor, the drain electrode of the second transistor being coupled to the gate electrode of the third transistor, the drain electrode of the third transistor being coupled to the gate electrode of the first transistor, the source electrodes of the first, second and third transistors being connected to a first voltage source; fourth, fifth and sixth insulated gate field effect transistors, the source electrodes of the fourth, fifth and sixth transistors being connected to the drain electrodes of the first, second and third transistors, respectively, the drain electrodes of the fourth, fifth and sixth transistors being connected to a second voltage source, the gate electrodes of the fourth and fifth transistors being connected in common; said compensation means including a seventh field effect transistor, the source electrode of the seventh transistor being connected to said first voltage source, the drain electrode of the seventh transistor being connected to the commonly connected gate electrodes of said fourth and fifth transistors, the gate electrode of the seventh transistor being connected to a biasing potential, and a resistor connected between the drain electrode of said seventh transistor and said second voltage source.

2. The combination according to claim 1, wherein said pulse generator further includes a first capacitor connected between the drain electrode of said first transistor and said first voltage source, and a second capacitor coupled between the drain electrode of said second transistor and said first voltage source.

3. The combination according to claim 1 or 2, wherein the gate electrode of the sixth transistor is connected to the drain electrode of said seventh transistor.

unaffected. When the output voltage at the point *b* of the IGFET 13 becomes larger than the threshold voltage level of the IGFET 15, initiating the period of time *t6*, the IGFET 15 becomes conductive, so that the output voltage at the point *c* rapidly changes its state to substantially earth potential. When the output voltage at the point *c* of the IGFET 15 becomes smaller than the threshold level of the IGFET 11, initiating the period of time *t7*, the IGFET 11 is cut-off and the voltage output at point *a* gradually increases. Subsequently, the same operations as described above are repeated for the operation of the pulse generator 22. The output voltage of the pulse generator 22 at terminal O is shown in waveform (c).

However, the oscillation period of the pulse generator circuit 22 changes with the change in ambient temperature and power supply voltage. Moreover, MOSICs which are manufactured to include such a pulse generator circuit will have different oscillation periods due to differences in the circuit constants of respective IGFETs which make up the MOSICs. In order to overcome these difficulties a compensating circuit 23 is provided, as described previously. Since the MOSFET 20, which is connected in back-to-back parallel relationship with IGFET 19, is manufactured in accordance with the same conditions as the IGFETs 12, 14 and 16, the IGFET 20 will have the same threshold voltage V_{th} thereas.

When the ambient temperature of the pulse generator circuit 22 increases, the current which flows through the IGFETs 12 and 14 decreases, resulting in an increase in the time which is required to charge the capacitors 17 and 18. As a result, the mark space ratio or the period of the pulse generator increases, unless something is done to compensate for this condition.

In accordance with the present invention, however, because of the compensation circuit 23, the current flowing through the IGFETs 19 and 20 also decreases when the ambient temperature increases. Then, since the voltage drop across the resistor 21 decreases, the voltage which is applied to the gate electrodes of the IGFETs 12 and 14 increases so as to increase the current flowing therethrough. As a result, what would have been a decrease in the duty ratio or the oscillation period is nullified.

Similarly, when the power supply voltage VGG increases, the current flowing through the respective IGFETs 12 and 14 increases. However, this increase is compensated by an increase in the voltage drop across the resistor 21, since the current flowing through the IGFET 19 will

also increase. As a result, compensation for changes in the supply voltage are effected.

It can be seen, therefore, that the present invention provides compensation for changes in ambient temperature, supply voltage and differences in the electrical characteristics of respective IGFETs making up differently manufactured MOSIC pulse generators under the same operating conditions, since the transistors of the compensating circuit are manufactured under the same production conditions as the IGFETs making up the pulse generator circuit.

WHAT WE CLAIM IS:—

1. In combination, a pulse generator circuit and compensation means: said pulse generator circuit comprising first, second and third insulated gate field effect transistors, the drain electrode of the first transistor being coupled to the gate electrode of the second transistor, the drain electrode of the second transistor being coupled to the gate electrode of the third transistor, the drain electrode of the third transistor being coupled to the gate electrode of the first transistor, the source electrodes of the first, second and third transistors being connected to a first voltage source; fourth, fifth and sixth insulated gate field effect transistors, the source electrodes of the fourth, fifth and sixth transistors being connected to the drain electrodes of the first, second and third transistors, respectively, the drain electrodes of the fourth, fifth and sixth transistors being connected to a second voltage source, the gate electrodes of the fourth and fifth transistors being connected in common; said compensation means including a seventh field effect transistor, the source electrode of the seventh transistor being connected to said first voltage source, the drain electrode of the seventh transistor being connected to the commonly connected gate electrodes of said fourth and fifth transistors, the gate electrode of the seventh transistor being connected to a biasing potential, and a resistor connected between the drain electrode of said seventh transistor and said second voltage source.

2. The combination according to claim 1, wherein said pulse generator further includes a first capacitor connected between the drain electrode of said first transistor and said first voltage source, and a second capacitor coupled between the drain electrode of said second transistor and said first voltage source.

3. The combination according to claim 1 or 2, wherein the gate electrode of the sixth transistor is connected to the drain electrode of said seventh transistor.





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4. The combination according to any one of the preceding claims, wherein said resistor has a current flow therethrough which is substantially proportional to the voltage drop thereacross.

5. The combination according to any one of the preceding claims, wherein said seventh transistor is of the insulated gate field effect type and its gate electrode is connected to the second voltage source.

6. The combination according to claim 5, wherein said compensation means further includes an eighth insulated gate field effect transistor connected in parallel to said seventh transistor, the commonly connected source electrodes being connected to said first voltage source, the commonly connected drain electrodes

being connected to the commonly connected gate electrodes of said fourth and fifth transistors, the gate electrode of the eighth transistor being connected to the first voltage source.

7. The combination of a pulse generator circuit and compensation means, constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figures 6 and 7 of the accompanying drawings.

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