FIG. 1

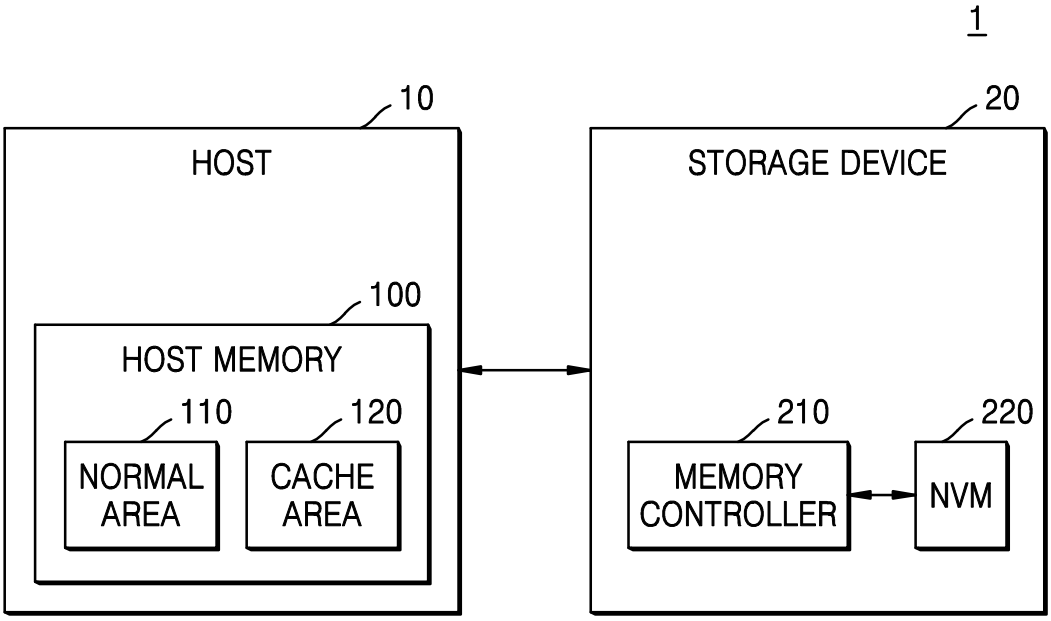

1
10
HOST
100
HOST MEMORY
110
NORMAL AREA
120
CACHE AREA
20
STORAGE DEVICE
210
MEMORY CONTROLLER
220
NVM

FIG. 2

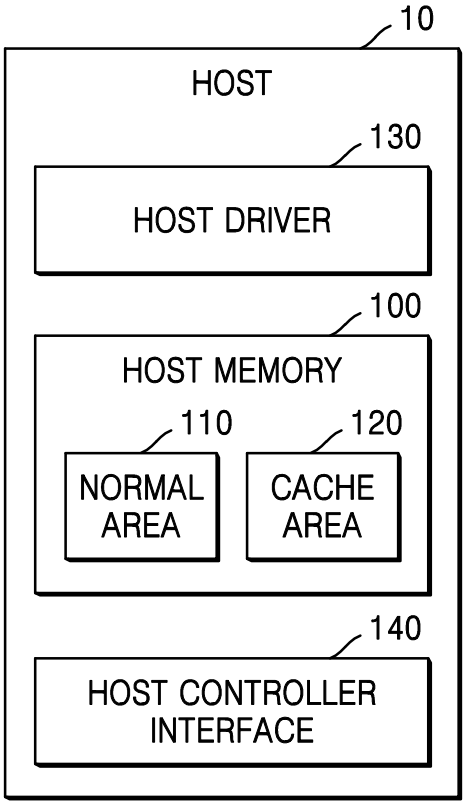

10
HOST
130
HOST DRIVER
100
HOST MEMORY
110
120
NORMAL AREA
CACHE AREA
140
HOST CONTROLLER INTERFACE

FIG. 3

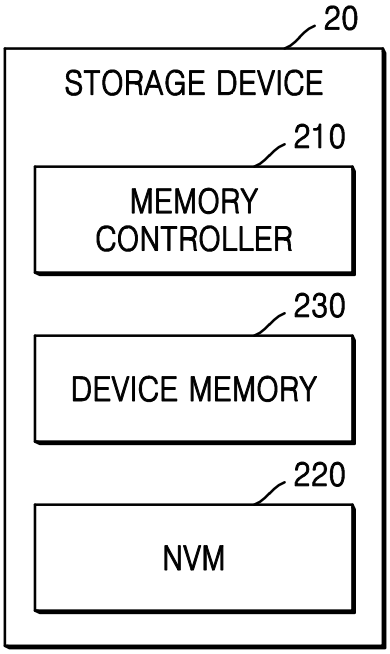

20
STORAGE DEVICE
210
MEMORY CONTROLLER
230
DEVICE MEMORY
220
NVM

FIG. 4

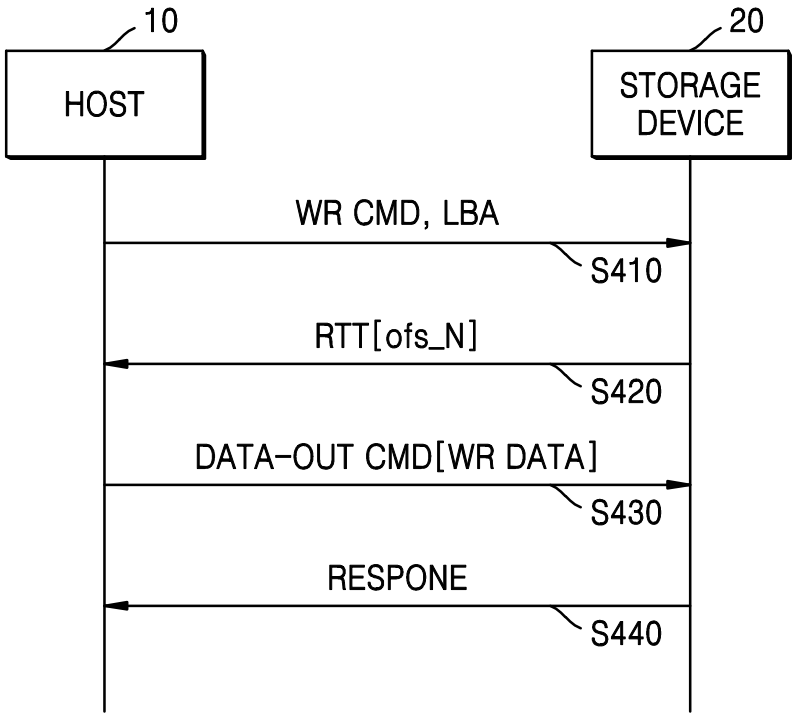

10
HOST
20
STORAGE DEVICE
WR CMD, LBA
S410
RTT[ofs_N]
S420
DATA-OUT CMD[WR DATA]
S430
RESPONE
S440

FIG. 5

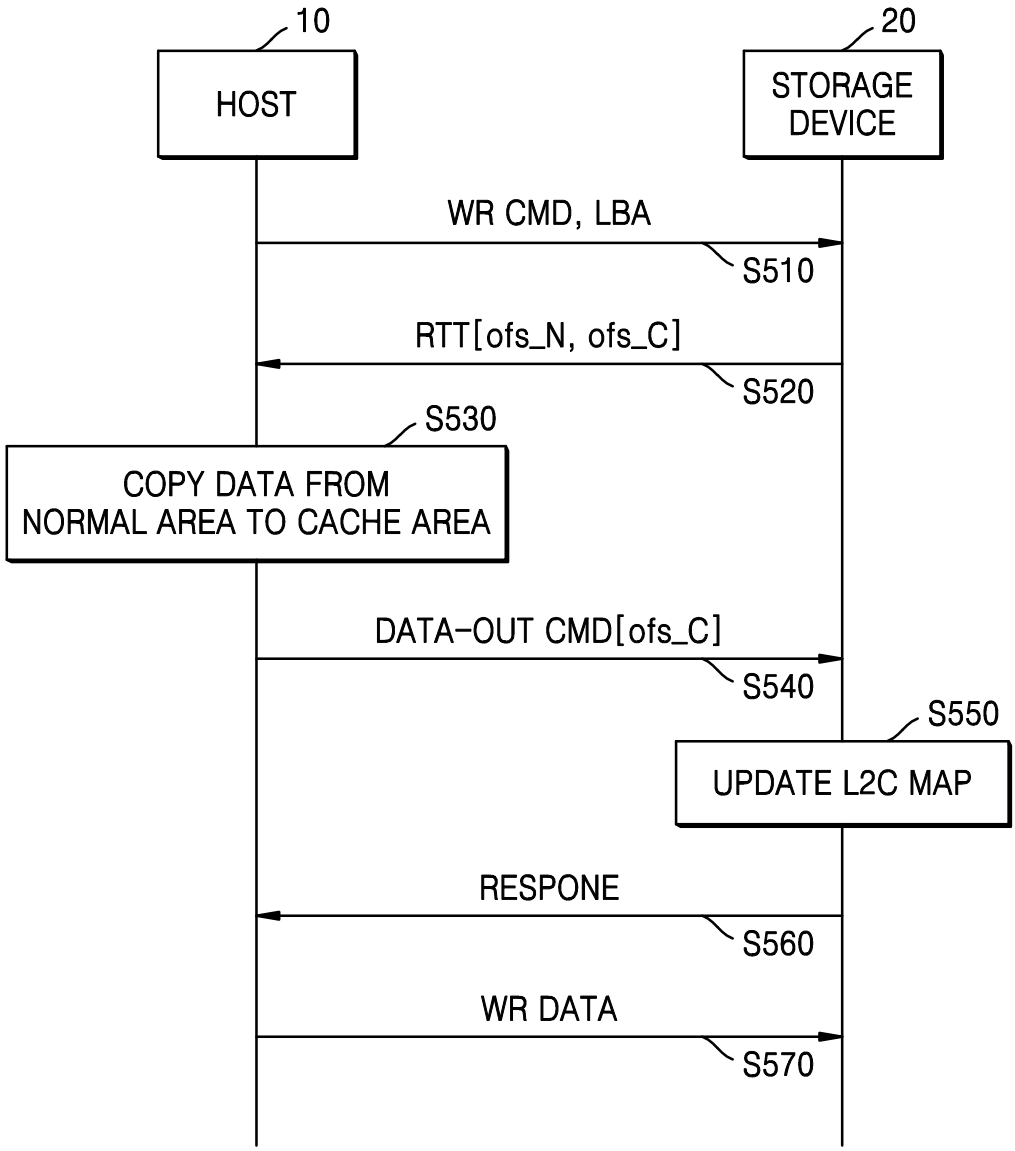

10
HOST
20
STORAGE DEVICE
WR CMD, LBA
S510
RTT[ofs_N, ofs_C]
S520
S530
COPY DATA FROM NORMAL AREA TO CACHE AREA
DATA-OUT CMD[ofs_C]
S540
S550
UPDATE L2C MAP
RESPONE
S560
WR DATA
S570

FIG. 6

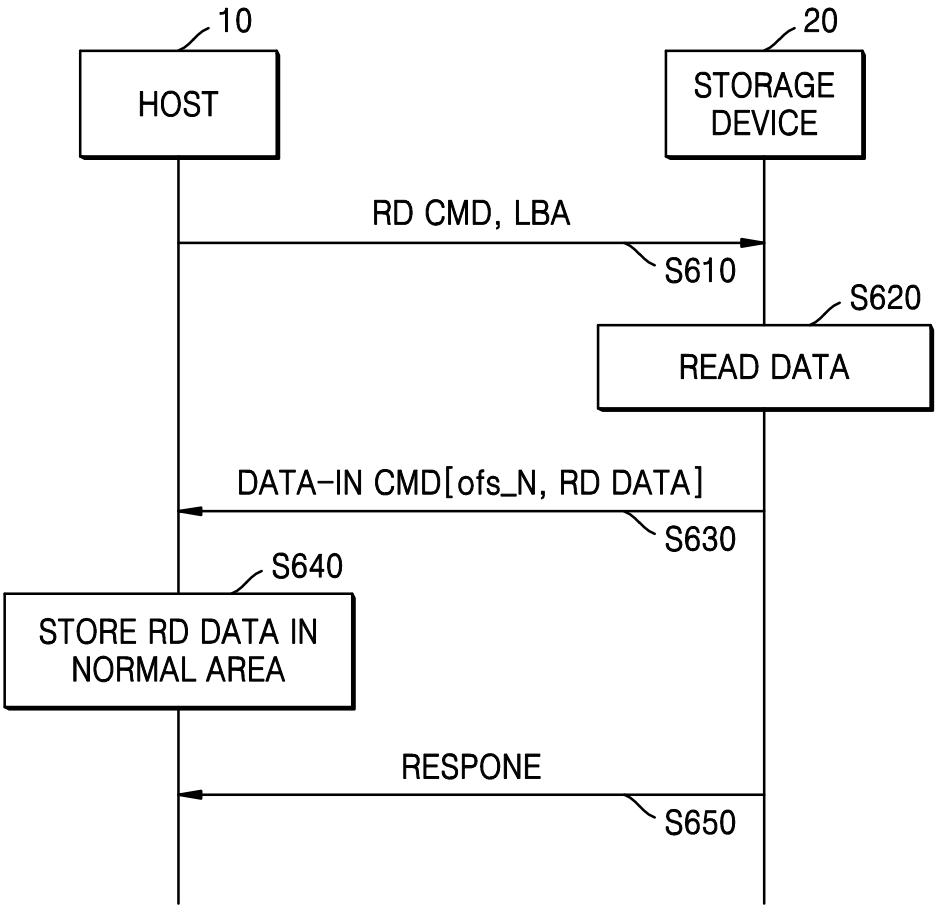

10
HOST
20
STORAGE DEVICE
RD CMD, LBA
S610
S620
READ DATA
DATA-IN CMD[ofs_N, RD DATA]
S630
S640
STORE RD DATA IN NORMAL AREA
RESPONE
S650

FIG. 7

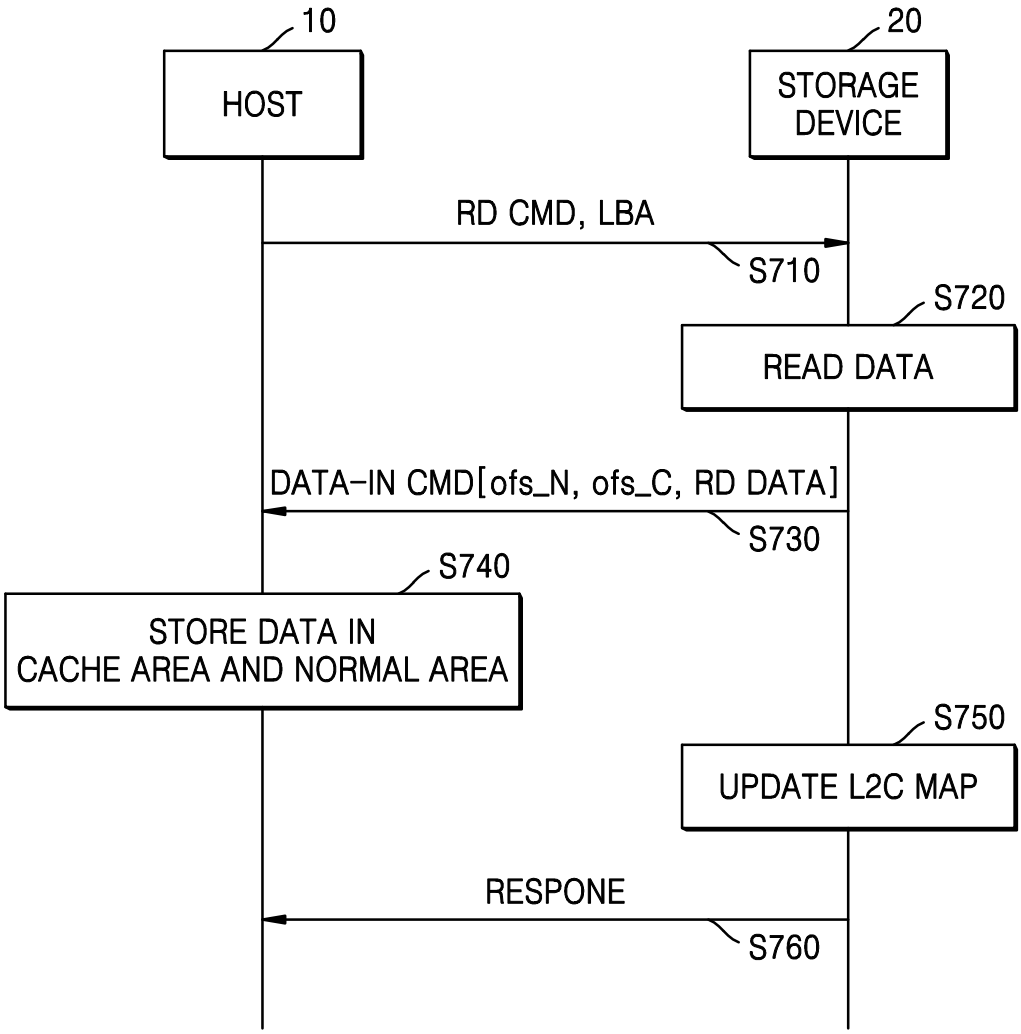

10
HOST
20
STORAGE DEVICE
RD CMD, LBA
S710
S720
READ DATA
DATA-IN CMD[ofs_N, ofs_C, RD DATA]
S730
S740
STORE DATA IN CACHE AREA AND NORMAL AREA
S750
UPDATE L2C MAP
RESPONE
S760

FIG. 8

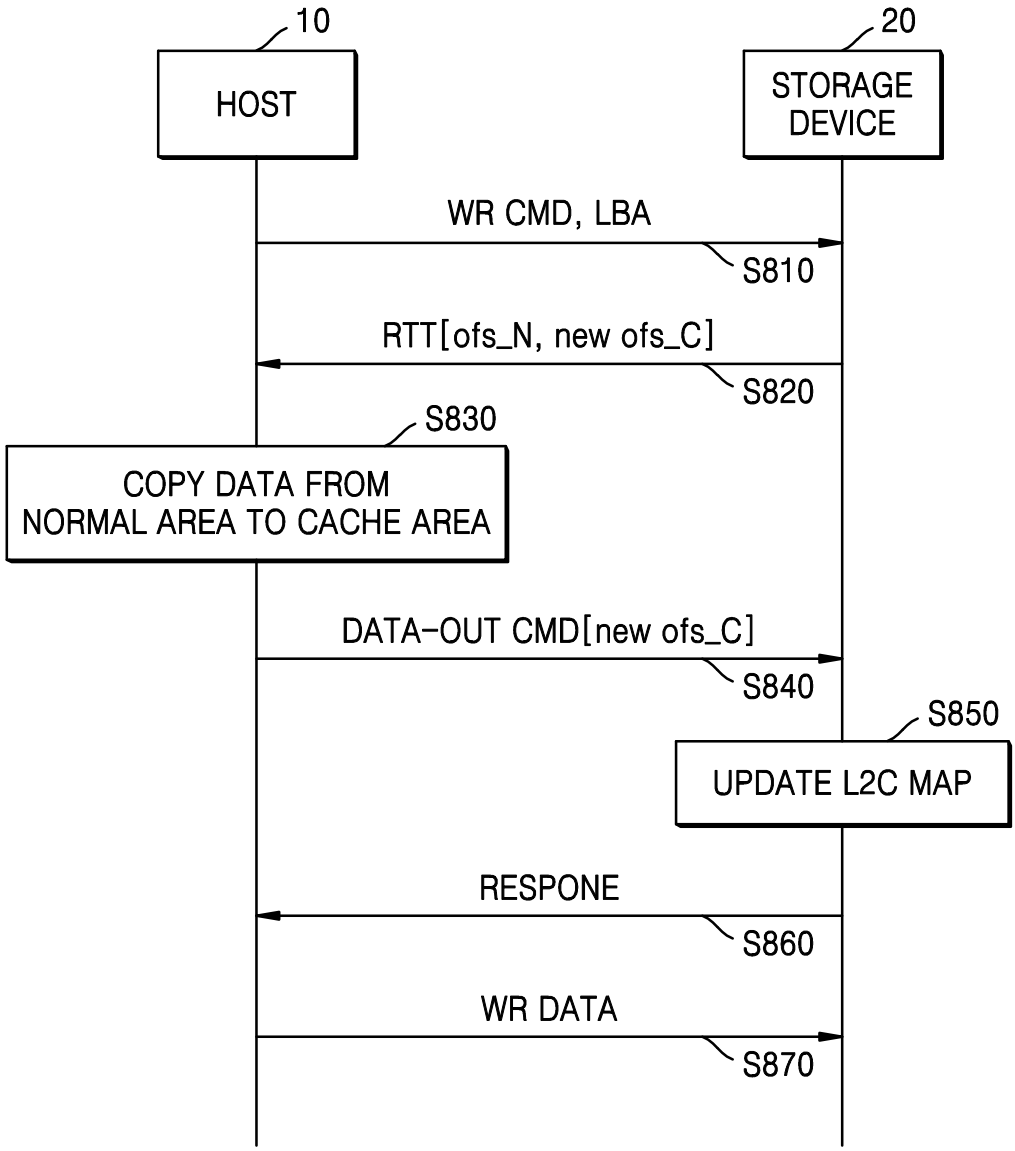

10
HOST
20
STORAGE DEVICE
WR CMD, LBA
S810
RTT[ofs_N, new ofs_C]
S820
S830
COPY DATA FROM NORMAL AREA TO CACHE AREA
DATA-OUT CMD[new ofs_C]
S840
S850
UPDATE L2C MAP
RESPONE
S860
WR DATA
S870

FIG. 9

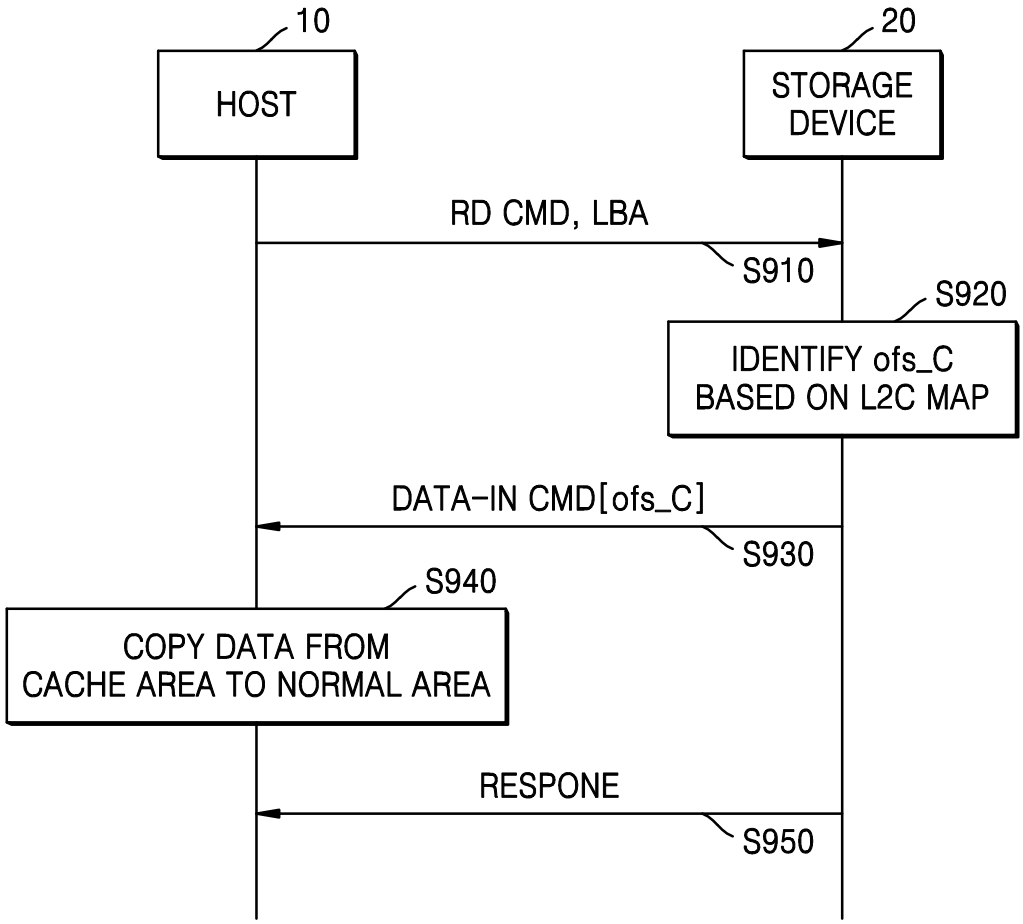

10
HOST
20
STORAGE DEVICE
RD CMD, LBA
S910
S920
IDENTIFY ofs_C BASED ON L2C MAP
DATA-IN CMD[ofs_C]
S930
S940
COPY DATA FROM CACHE AREA TO NORMAL AREA
RESPONE
S950

FIG. 10

LBA	ofs_N	ofs_C	PGM unit	STR ID
LBA1	ofs_N1	ofs_C1	QLC	STR1
⋮	⋮	⋮	⋮	⋮
LBAn	ofs_Nn	ofs_Cn	TLC	STRn

L2C MAP

FIG. 11

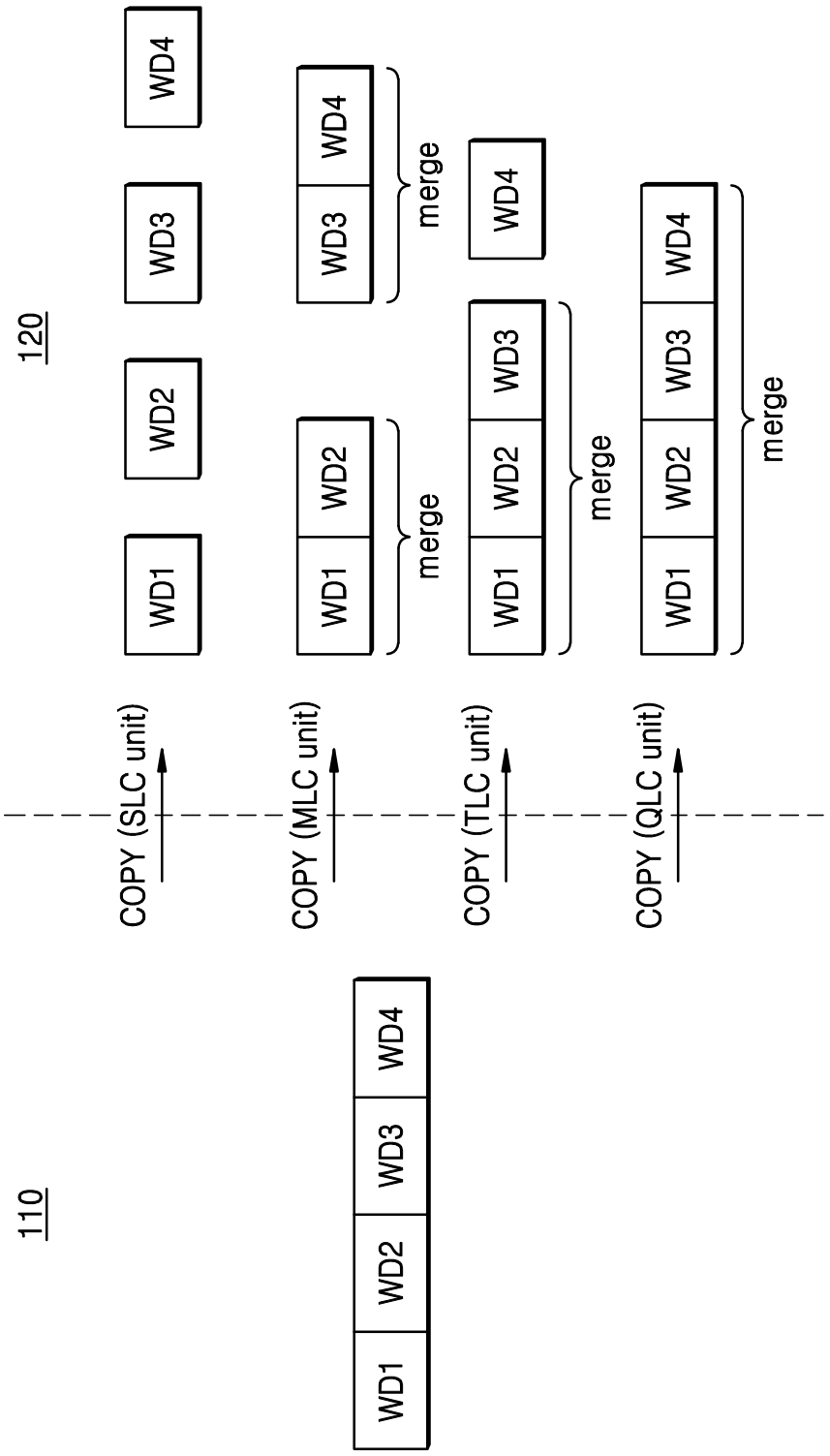

110
WD1
WD2
WD3
WD4
120
COPY (SLC unit)
COPY (MLC unit)
COPY (TLC unit)
COPY (QLC unit)
merge
merge
merge

FIG. 12

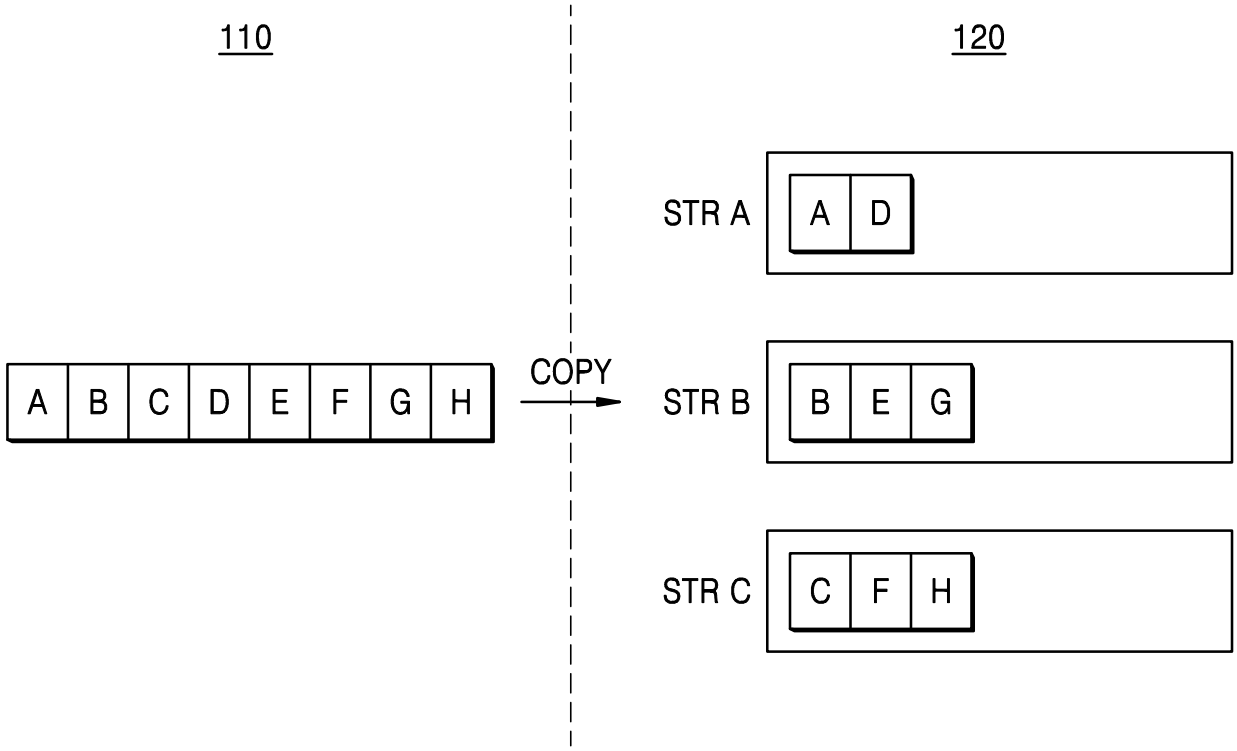


FIG. 13A

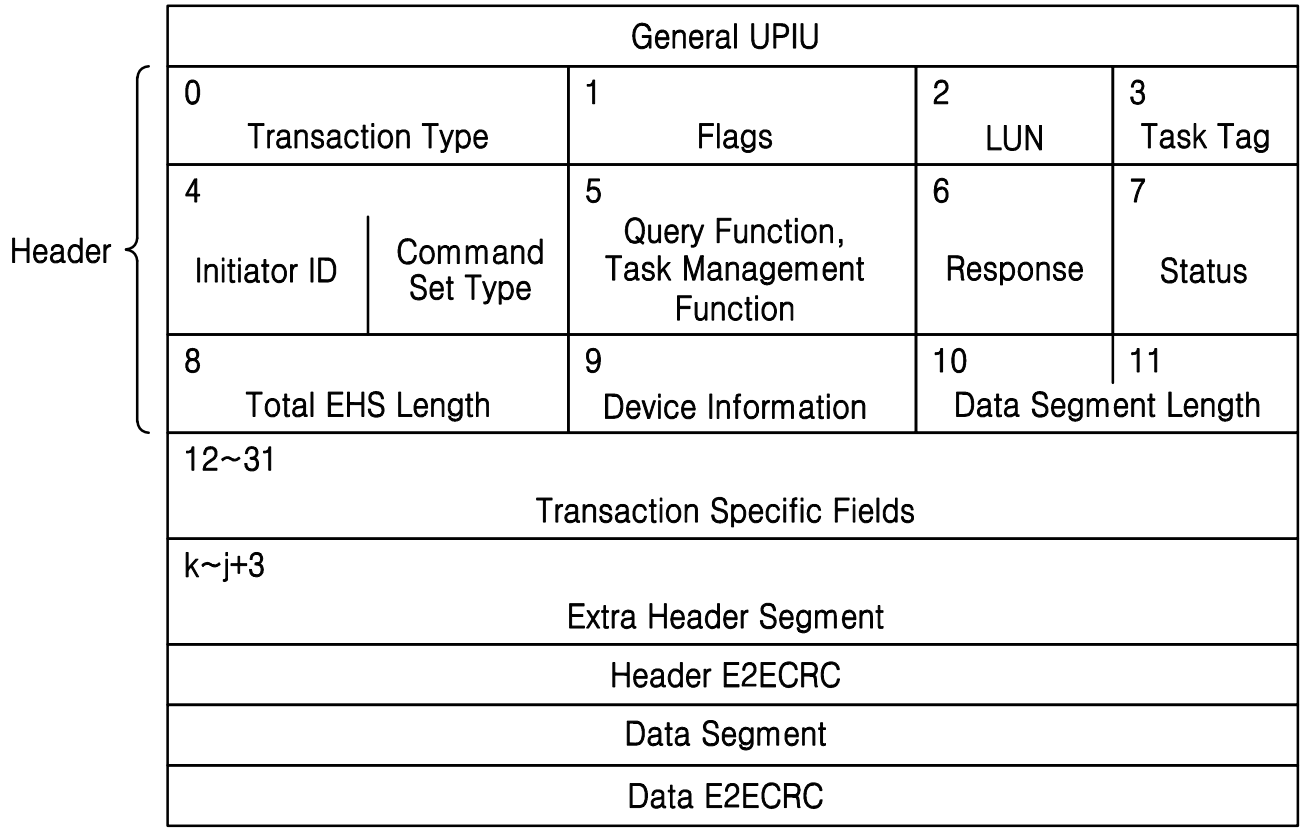

General UPIU
Header
0
Transaction Type
1
Flags
2
LUN
3
Task Tag
4
Initiator ID
Command Set Type
5
Query Function, Task Management Function
6
Response
7
Status
8
Total EHS Length
9
Device Information
10
11
Data Segment Length
12~31
Transaction Specific Fields
k~j+3
Extra Header Segment
Header E2ECRC
Data Segment
Data E2ECRC

FIG. 13B

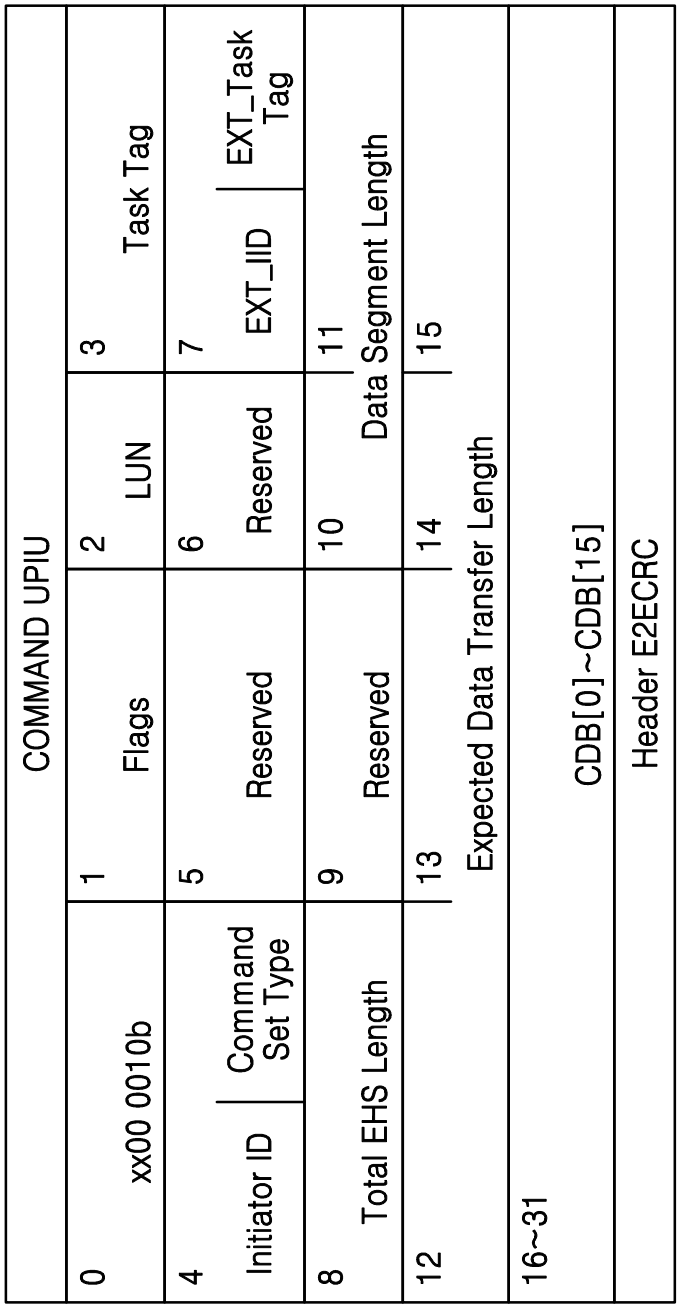

COMMAND UPIU
Header
0
xx00 0010b
1
Flags
2
LUN
3
Task Tag
4
Initiator ID
Command Set Type
5
Reserved
6
Reserved
7
EXT_IID
EXT_Task Tag
8
Total EHS Length
9
Reserved
10
Data Segment Length
11
12
13
Expected Data Transfer Length
14
15
16~31
CDB[0]~CDB[15]
Header E2ECRC

FIG. 13C

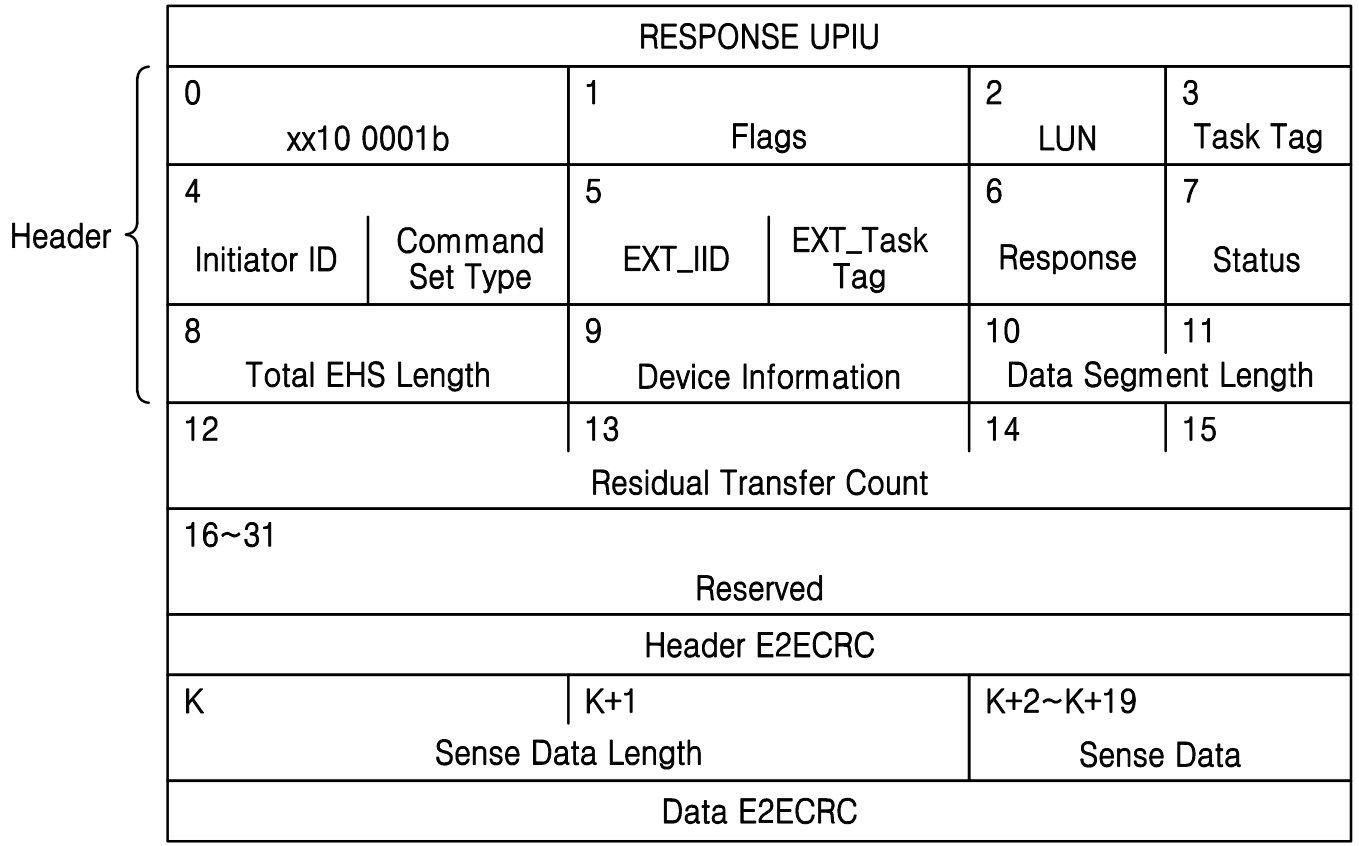

RESPONSE UPIU
Header
0
xx10 0001b
1
Flags
2
LUN
3
Task Tag
4
Initiator ID
Command Set Type
5
EXT_IID
EXT_Task Tag
6
Response
7
Status
8
Total EHS Length
9
Device Information
10
11
Data Segment Length
12
13
14
15
Residual Transfer Count
16~31
Reserved
Header E2ECRC
K
K+1
Sense Data Length
K+2~K+19
Sense Data
Data E2ECRC

FIG. 13D

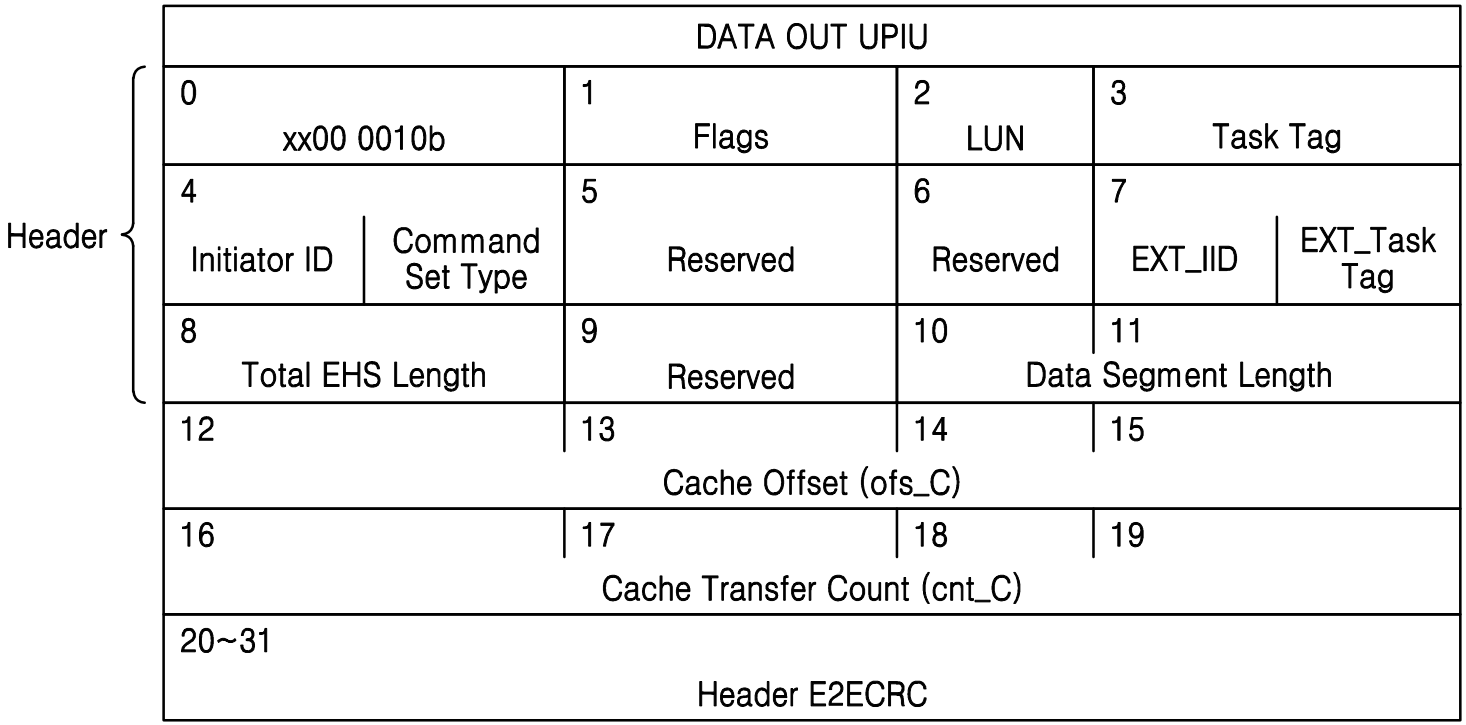

DATA OUT UPIU
Header
0
xx00 0010b
1
Flags
2
LUN
3
Task Tag
4
Initiator ID
Command Set Type
5
Reserved
6
Reserved
7
EXT_IID
EXT_Task Tag
8
Total EHS Length
9
Reserved
10
11
Data Segment Length
12
13
14
15
Cache Offset (ofs_C)
16
17
18
19
Cache Transfer Count (cnt_C)
20~31
Header E2ECRC

FIG. 13E

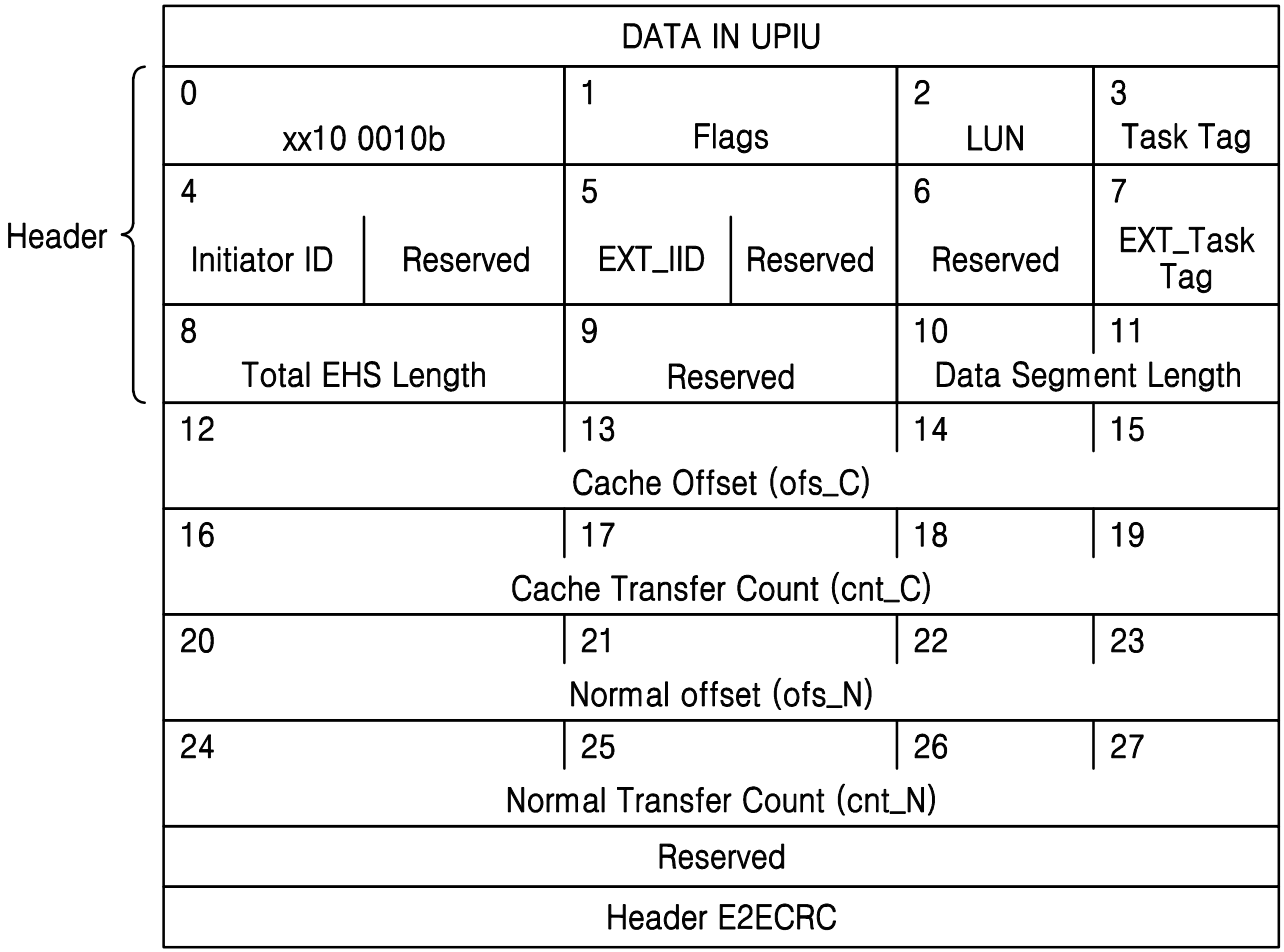

DATA IN UPIU
Header
0
xx10 0010b
1
Flags
2
LUN
3
Task Tag
4
Initiator ID
Reserved
5
EXT_IID
Reserved
6
Reserved
7
EXT_Task Tag
8
Total EHS Length
9
Reserved
10
11
Data Segment Length
12
13
14
15
Cache Offset (ofs_C)
16
17
18
19
Cache Transfer Count (cnt_C)
20
21
22
23
Normal offset (ofs_N)
24
25
26
27
Normal Transfer Count (cnt_N)
Reserved
Header E2ECRC

FIG. 13F

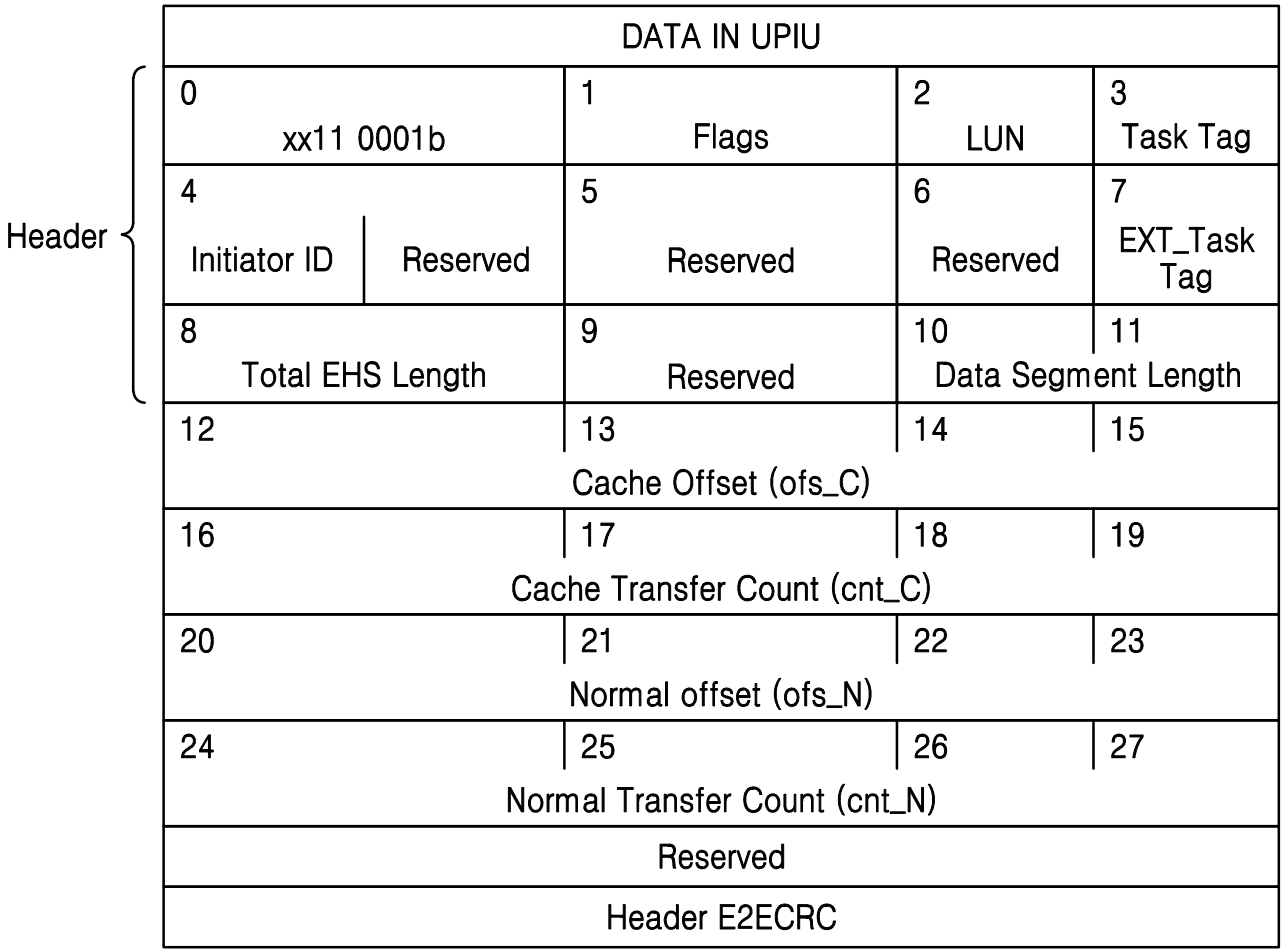

DATA IN UPIU
Header
0
xx11 0001b
1
Flags
2
LUN
3
Task Tag
4
Initiator ID
Reserved
5
Reserved
6
Reserved
7
EXT_Task Tag
8
Total EHS Length
9
Reserved
10
11
Data Segment Length
12
13
14
15
Cache Offset (ofs_C)
16
17
18
19
Cache Transfer Count (cnt_C)
20
21
22
23
Normal offset (ofs_N)
24
25
26
27
Normal Transfer Count (cnt_N)
Reserved
Header E2ECRC

FIG. 14

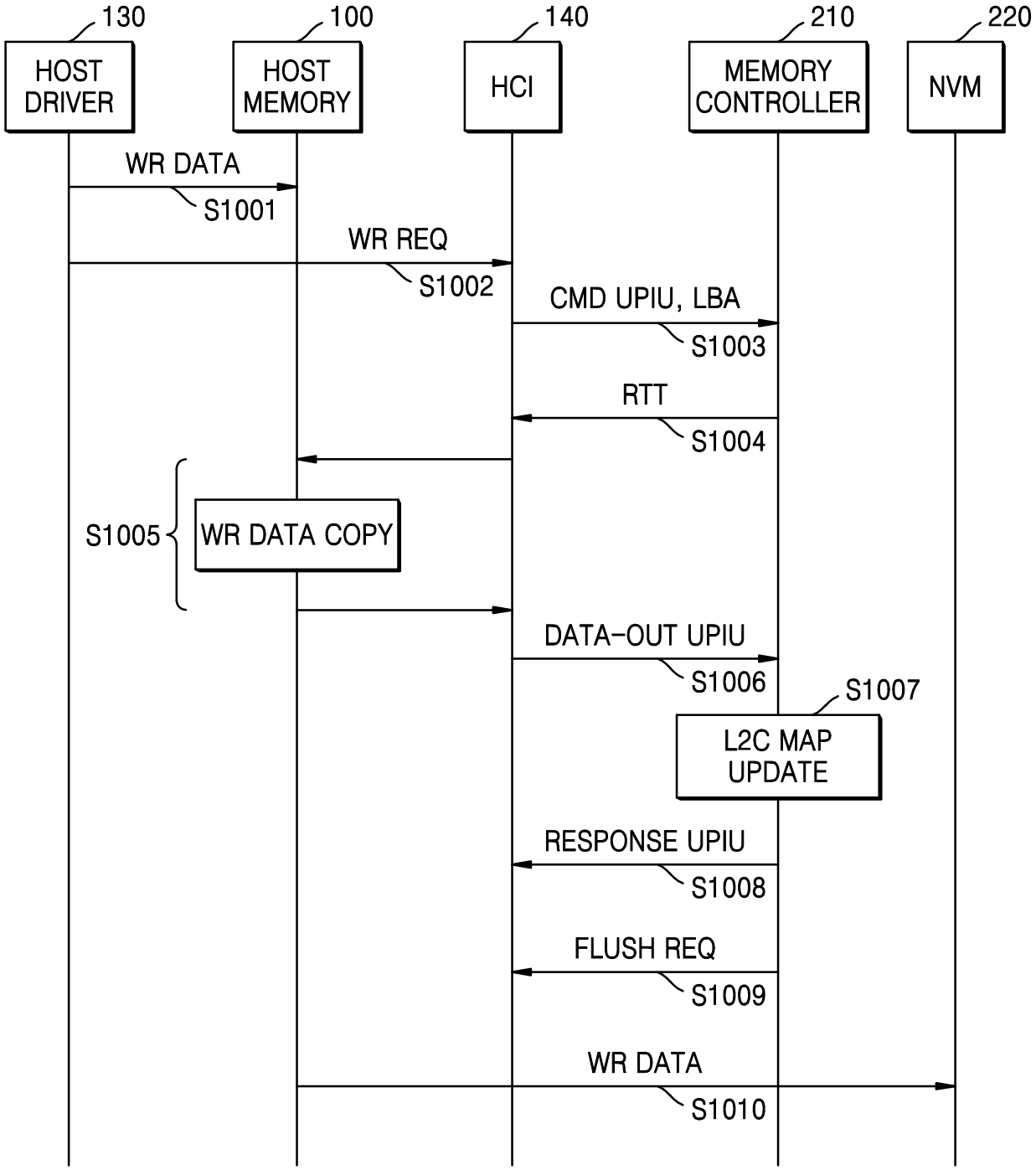

130
HOST DRIVER
100
HOST MEMORY
140
HCI
210
MEMORY CONTROLLER
220
NVM
WR DATA
S1001
WR REQ
S1002
CMD UPIU, LBA
S1003
RTT
S1004
S1005
WR DATA COPY
DATA-OUT UPIU
S1006
S1007
L2C MAP UPDATE
RESPONSE UPIU
S1008
FLUSH REQ
S1009
WR DATA
S1010

FIG. 15

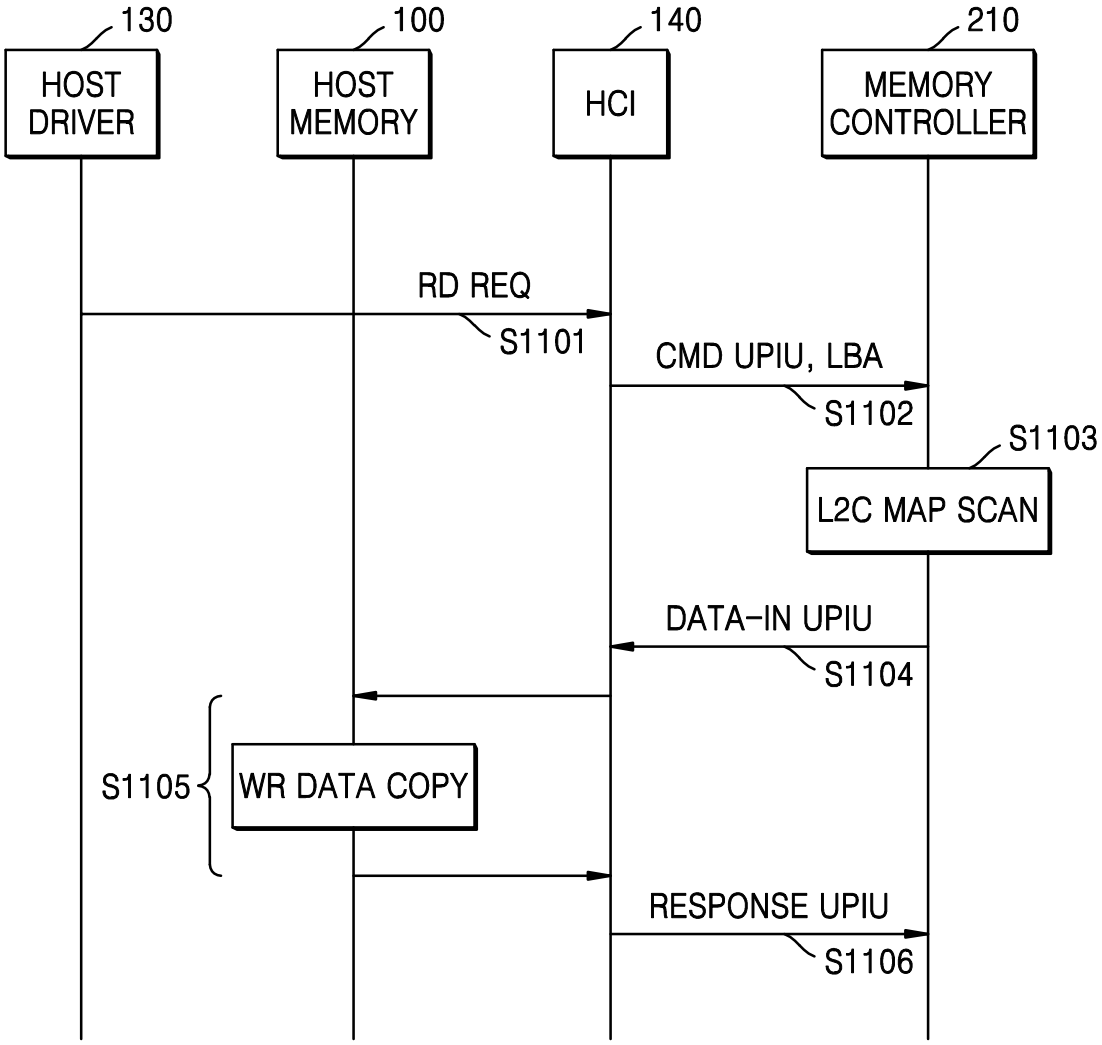

130
HOST DRIVER
100
HOST MEMORY
140
HCI
210
MEMORY CONTROLLER
RD REQ
S1101
CMD UPIU, LBA
S1102
S1103
L2C MAP SCAN
DATA-IN UPIU
S1104
S1105
WR DATA COPY
RESPONSE UPIU
S1106

FIG. 16

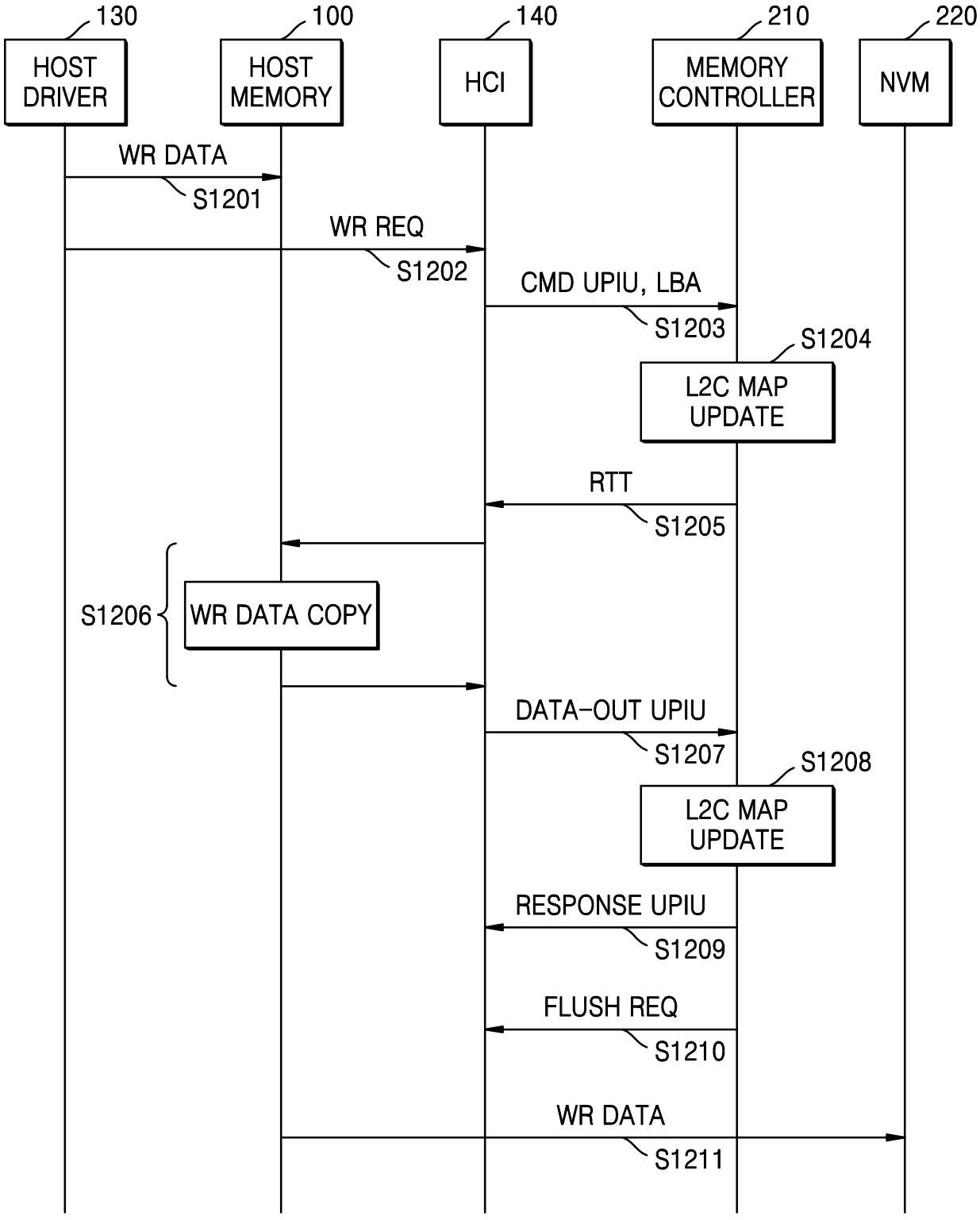

130
HOST DRIVER
100
HOST MEMORY
140
HCI
210
MEMORY CONTROLLER
220
NVM
WR DATA
S1201
WR REQ
S1202
CMD UPIU, LBA
S1203
S1204
L2C MAP UPDATE
RTT
S1205
S1206
WR DATA COPY
DATA-OUT UPIU
S1207
S1208
L2C MAP UPDATE
RESPONSE UPIU
S1209
FLUSH REQ
S1210
WR DATA
S1211

FIG. 17

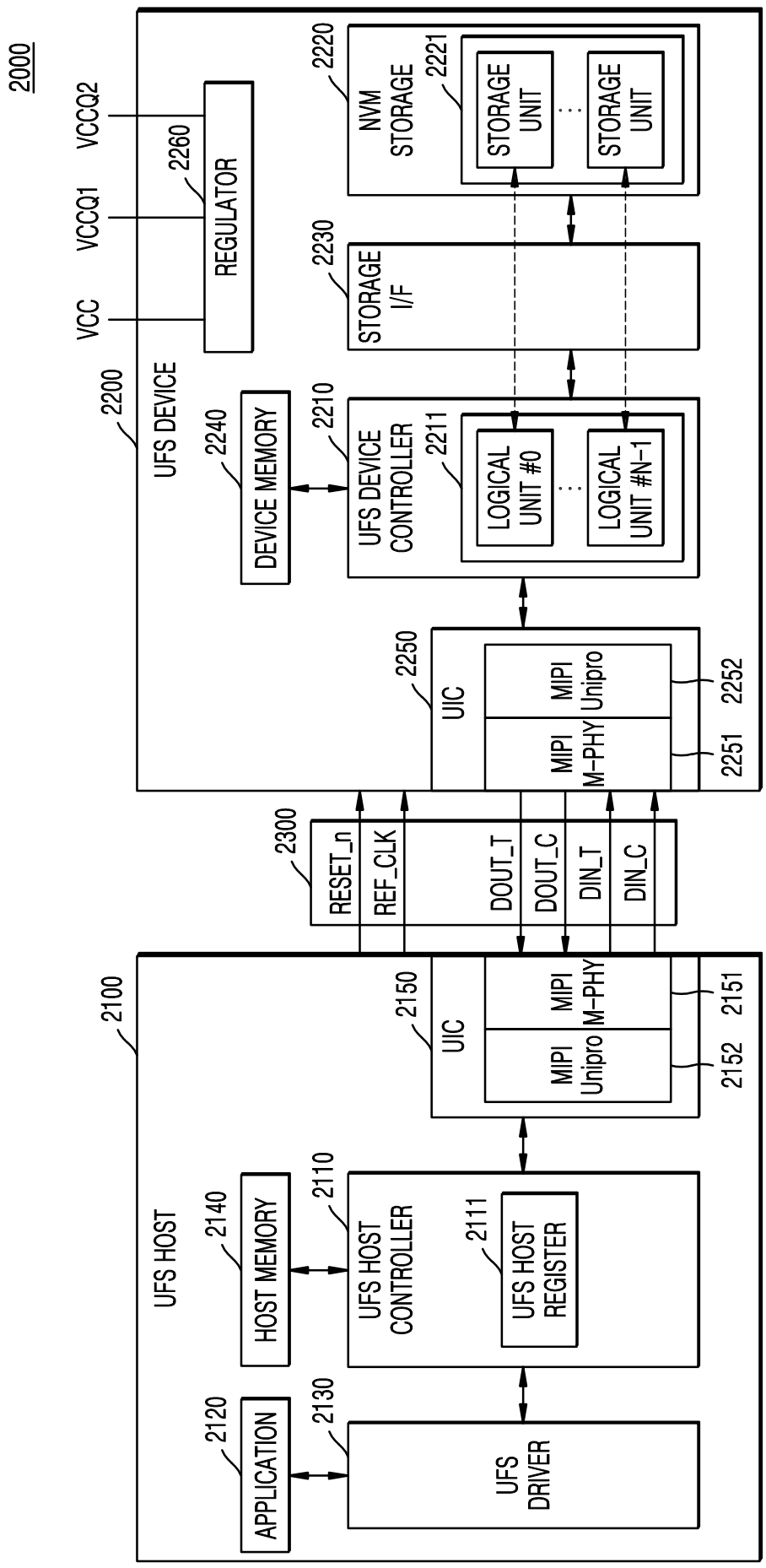

2000
2100
UFS HOST
2120
APPLICATION
2130
UFS DRIVER
2140
HOST MEMORY
2110
UFS HOST CONTROLLER
2111
UFS HOST REGISTER
2150
UIC
MIPI M-PHY
MIPI Unipro
2151
2152
2300
RESET_n
REF_CLK
DOUT_T
DOUT_C
DIN_T
DIN_C
2200
UFS DEVICE
2240
DEVICE MEMORY
2210
UFS DEVICE CONTROLLER
2211
LOGICAL UNIT #0
LOGICAL UNIT #N-1
2250
UIC
MIPI M-PHY
MIPI Unipro
2251
2252
2230
STORAGE I/F
2220
NVM STORAGE
2221
STORAGE UNIT
STORAGE UNIT
2260
REGULATOR
VCC
VCCQ1
VCCQ2

FIG. 18

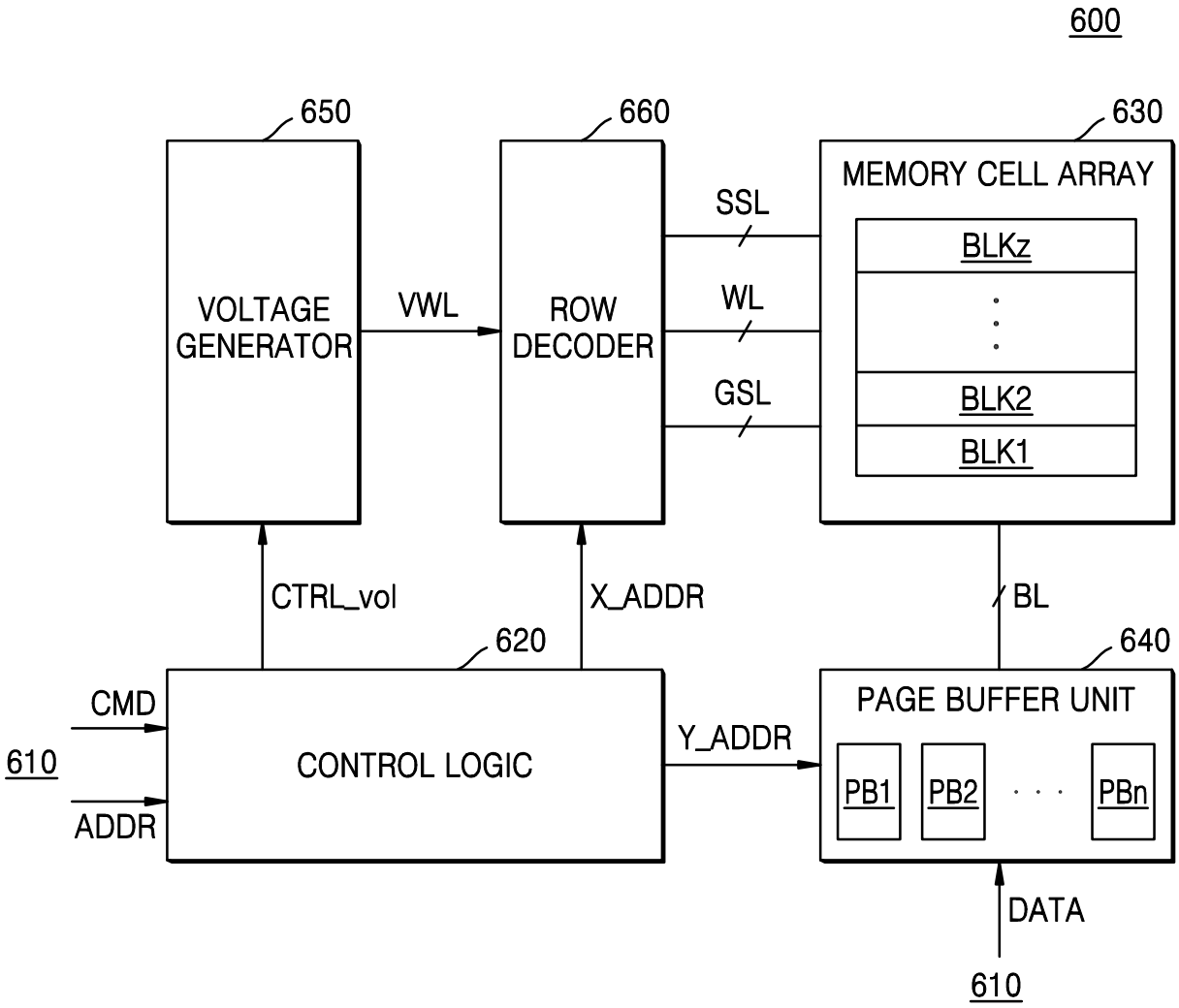
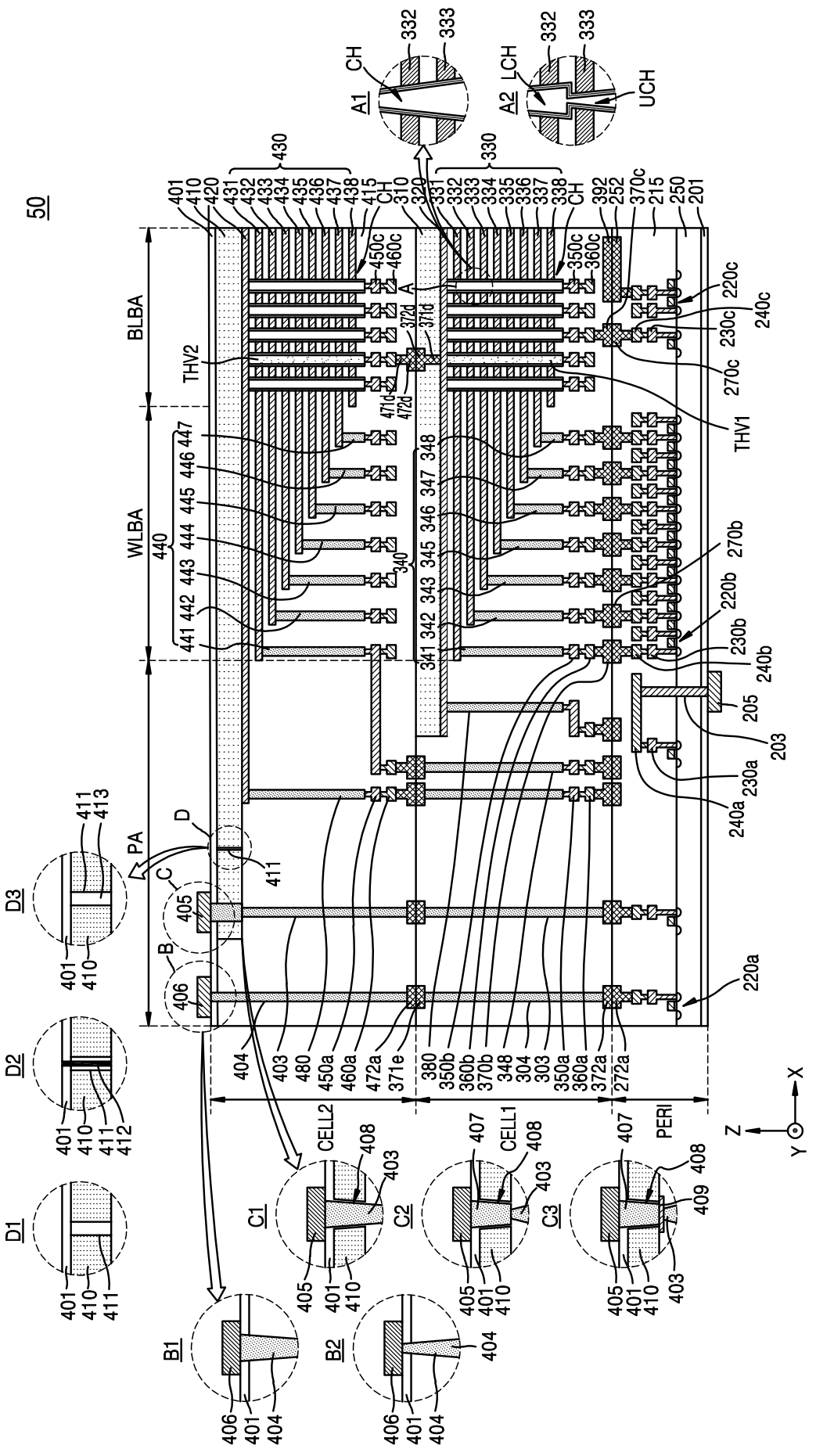

600
650
660
630
MEMORY CELL ARRAY
SSL
BLKz
VOLTAGE GENERATOR
VWL
ROW DECODER
WL
GSL
BLK2
BLK1
CTRL_vol
X_ADDR
BL
620
640
CMD
610
CONTROL LOGIC
Y_ADDR
PAGE BUFFER UNIT
PB1
PB2
PBn
ADDR
DATA
610

FIG. 19


50
BLBA
WLBA
PA
THV1
THV2
CELL1
CELL2
PERI
A1
A2
B1
B2
C1
C2
C3
D1
D2
D3
CH
LCH
UCH
X
Y
Z