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(54) Title: SYSTEM FOR DESIGN AND MANUFACTURING OF MULTI-PROCESSOR AND MULTI-CORE INTEGRATED CIRCUITRY (IC) PARALLEL PROCESSING MAXIMAL COMPUTATIONAL BLOCKS, AND METHOD THEREOF

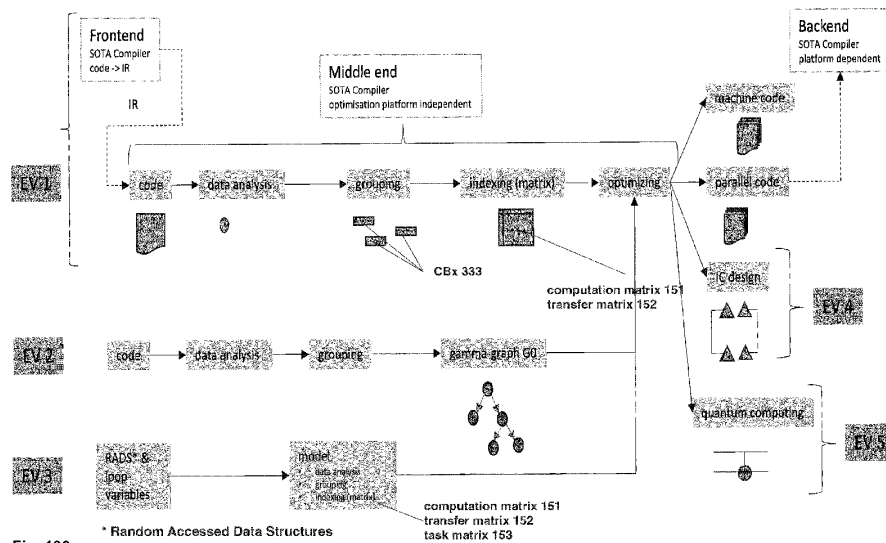


Fig. 106

(57) Abstract: Proposed is a computer-aided IC manufacturing system (0) and method for optimized generation of a multi-core and/or multi-processor integrated circuit (2) architecture or layout, integrated circuit (2) performance and integrated circuit (2) manufacturing yield. The multi-core and/or multi-processor integrated circuit (2) has a plurality of processing units (21) and/or processing pipelines (53) simultaneously processing instructions on data by executing a parallelized processing machine code (32). The execution of the parallelized processing code (32) by the parallel processing multi-core and/or multi-processor integrated circuit (2) comprises the occurrence of latency times (26), where the latency times being given by idle time of a processing unit (21) between transmitting data back after having processed a specific block of instructions of the processing code (32) on the data by the processing unit (21) and

[Continued on next page]

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receiving data necessary for execution of a consecutive block of instructions of the processing code (32) by said processing units (21).