

**METHOD FOR SYNCHRONIZING DATA CONVERTERS BY MEANS OF A SIGNAL
TRANSMITTED FROM ONE TO THE NEXT**

TECHNICAL FIELD

The invention relates to the synchronization of analogue-digital and/or digital-analogue data converters. It more particularly relates to rapid converters the working frequency of which is about one hundred megahertz and higher. The invention is in particular applicable to systems that require a plurality of these rapid converters to be synchronized, such as for example antenna arrays or systems for communicating data using I/Q modulation.

TECHNICAL PROBLEM

Rapid converters are generally formed from two or more converter cores that each work at a lower working (sampling) frequency, and the output signals of which are combined (interleaved) to obtain the expected conversion frequency. The sampling clocks of these converters are thus usually generated internally by a clock generator that performs a frequency division of the reference clock. If there are n converting cores per converter, the sampling frequency is obtained from the reference clock CLK by dividing its frequency by n .

In an architecture including a plurality of converters, it is necessary to be able to synchronize the converters, to make them start in phase. In the case of rapid converters, it is a question of starting the frequency dividers in phase, i.e. it is not enough to say that they are reset synchronously to a reference-clock active front, it is also necessary to know which active front is being spoken of, otherwise the sampling clocks obtained will possibly not all be in phase depending on whether the frequency dividers start on a given clock active front or the following one.

One of the known solutions of this problem is to use a signal (usually called a synchronizing signal) that is a pulse distributed in phase to all the converters and the distribution of which is designed to obtain the appropriate propagation time for each converter, so that the clock active fronts on which the frequency dividers are initialized correspond, i.e. pairwise these active fronts are all separated by a number of reference-clock periods that is a multiple of n : 0 , n , $2 \times n$, etc. Everything is determined by the design of the pathways for distributing the reference clock and the synchronizing signal to each of the converters.

This technique thus requires the distribution of the reference clock and the synchronizing signal to be very carefully designed, which requires propagation delays on the electrically conductive pathways carrying these signals to each of the converters in a given architecture to be precisely
 5 evaluated. It is a question of taking into account all the parameters influencing propagation: length and materials of the conductors, characteristics of the input and output stages of the signals, characteristics of solder joints, etc. Although it is known how to do this rather well at low frequencies, in the rapid systems with which we are concerned, which have
 10 working frequencies of 100 megahertz and higher, the task is more difficult. In particular there is then a severe additional constraint as regards the acquisition of the synchronizing signal, which must occur in a time window very much smaller than the clock period. All these difficulties add up and make it not only expensive but also difficult to obtain a synchronization that is
 15 sufficiently precise by design. At the system level this results in additional system complexity and a degraded performance.

Other known solutions do not use synchronizing signals. Examples of such solutions are solutions using phase lock loops PLL in the converters, such as for example described in the document published on the Internet:
 20 "*Synchronizing Multiple High-Speed Multiplexed DACs for Transmit applications*", XP002492319, 21 Sept. 2006, pp 1-6, url=<http://www.maxim.ic.com/an3901>. However, they cause other problems. In particular, they generally lead to jitter in the sampling clocks, thereby also impacting the performance of the converters. These PLL solutions also cause
 25 problems with temperature stability, not to mention the complexity that they add in each converter.

SUMMARY OF THE INVENTION

The invention proposes to solve the technical problem relating to the distribution of the synchronizing signal. A solution is sought that is simpler to
 30 implement including when it is necessary to synchronize many converters to a high-frequency clock, for example of a frequency of 100 megahertz and higher, with all the required precision.

In a given architecture, the propagation delays of a signal from one point to another are set by the physical characteristics of the propagation
 35 pathway of this signal in the architecture in question. Rather than acting

upstream, at the design stage, to set this delay for each converter as in the prior art, the ingenious idea of the invention is to arrange the converters in at least one series chain, and to replace the in-phase distribution of the synchronizing signal to all the converters with a transmission of this signal from one converter to the next in order to reach one by one all the converters of a chain, in combination with a parameterization, of each converter of the chain, which reflects the propagation delays of the synchronizing signal in this chain of converters and via which a synchronizing signal that is re-synchronized is transmitted as output from each converter to the following converter. In each converter, the parameterization also allows the right reference-clock active front to be chosen, i.e. the front that returns the right signal for resetting the sampling clock generator, allowing the sampling clocks of all the converters to be synchronized in phase.

In this way, upstream constraints on the design and production of the application circuits are relaxed and therefore their cost is decreased. Furthermore, an effective synchronization of the converters is achieved at the expense of a step of setting configuration parameters of the synchronization, which is easy to implement and needs to be carried out only once as demonstrated, and of the addition of sequential and combinatorial logic elements in each converter, allowing the parameterization to be determined and applied.

Thus, the invention relates to a method for synchronizing digital/analogue and/or analogue/digital data converters to an active front of a common reference clock CLK, characterized in that the converters form at least one series transmission chain allowing a synchronizing signal emitted by a unit for controlling the converters to be transmitted, such that:

- the converter of rank 1 in the chain has a synchronization input connected to a synchronization control output of the control unit;
- each converter of rank j higher than 1 in the chain has a synchronization input connected to the synchronization output of the converter of rank $j-1$ in the chain; and

the synchronizing method being characterized in that a procedure for synchronizing the converters of the chain to a CLK reference-clock active front activated by the control unit comprises the following steps, which are controlled by the control unit:

- a step of initializing, in each converter, a synchronization configuration register including at least one polarity parameter defining the polarity of a reference-clock front for detection of signals input via the synchronization input of the converter as the polarity of the reference-clock active front or the inverse polarity; then

- sending to the synchronization control output of the control unit a synchronizing signal, which is a pulse of width at least equal to one reference-clock period;

the synchronizing method also being characterized in that each converter in the chain is configured to carry out the following steps:

- a) a step of, on a CLK reference-clock front, that front has the polarity defined by the value of said polarity parameter configured in the converter, detecting a synchronizing signal input via the synchronization input, and

- b) a step of aligning with the following reference-clock active front the signal detected in step a), so as to deliver a synchronizing signal aligned with a reference-clock active front, and applying said signal to the synchronization output of the converter.

In one implementation, each converter in the chain is formed from n cores converting at a sampling frequency that is delivered by a divider by n of the reference-clock frequency, where n is a nonzero integer, and configured to carry out, following step b), the following steps:

- c) a step of shifting said aligned synchronizing signal obtained in step b) by an integer number of reference-clock period(s), which integer number is defined by the value of a phase parameter delivered by said configuration register of the converter; and

- d) a step of using the obtained shifted signal as a signal for resetting said divider of frequency by n ,

said integer number defined by the phase parameter having a value comprised between 0 and $n-1$, inclusive of limits.

Each converter in the chain is configured to carry out a step e) of verifying the stability of an active level of the signal received via the synchronization input and acquired on the reference-clock front defined in the detecting step a) by the value of said polarity parameter, by comparing the

first value acquired on said detecting front to at least one second value of said signal, which value is acquired on a front that is ahead, by a set time, of said detecting front and to at least one third value of said signal, which value is acquired on a front that is behind, by a set time, said detecting front, and if
 5 the values are not all identical, activating a corresponding flag bit in said configuration register of the converter.

The method comprises a setting phase allowing the polarity parameter of each converter, in succession from the first converter at the input of the chain to the last converter of the chain, to be configured by means of the flag
 10 bit of the configuration register of the converters, then a value p of the phase parameter of each converter to be configured on the basis of a determination of the integer number M of reference-clock periods separating the synchronizing pulse front output from the converter via its output from the synchronizing pulse front output from an upstream converter in the chain,
 15 and the value p of the phase parameter is such that the sum $M+p$ is a multiple of n .

The invention also relates to an analogue/digital or digital/analogue data converter that comprises an input for receiving a synchronizing signal and an associated synchronizing circuit allowing the converter to be
 20 synchronized to an active front of a reference-clock signal, according to the method of the invention.

Other features and advantages of the invention are presented in the following description, with reference to the appended drawings, in which:

25 - Figure 1 illustrates a data architecture in which the converters are configured to form a series chain for propagating a synchronizing signal according to the invention;

- Figure 2 is a simplified block diagram of a converter comprising circuit elements for implementing a synchronizing method in a chain of
 30 converters according to the invention;

- Figures 3 and 4 illustrate timing diagrams of the signals generated in each converter, depending on configuration parameters of the synchronization according to the invention;

- Figure 5 is a timing diagram that more particularly illustrates the phase alignment of the sampling clocks in a chain of converters according to the method of the invention;

5 - Figures 6 and 7 are a timing diagram of the signals and a flowchart of the steps of a setting procedure according to the invention, for configuring the polarity parameter of each converter, using a synchronizing signal emitted by the control unit and that is synchronous with the reference clock;

10 - Figures 8 and 9 illustrate a variant of the setting procedure using a synchronizing signal emitted by the control unit and that is asynchronous; and

 - Figures 10 and 11 schematically show various ways of forming (a) converter chain(s) that are compatible with a synchronizing method according to the invention.

DETAILED DESCRIPTION

15 The invention applies to systems for processing data that comprise a control unit that controls a set of analogue/digital and/or digital/analogue data converters that must work synchronously. In these architectures, the control unit, generally made up of a field-programmable gate array (FPGA) logic circuit, is designed to control the converters according to a master-slave
20 communication schema, by means of a peripheral interface bus such as, for example, a serial peripheral interface (SPI) bus, which is a very widely used synchronous series data bus. The peripheral interface bus allows data to be exchanged between the control unit and the converters, in particular data (DATA) that are the data to be converted (digital-analogue converter) or that
25 are the result of conversions (digital-analogue converter). These aspects will not be described in greater detail. They are well known to those skilled in the art.

 Figure 1 illustrates a processing architecture including K converters
30 controlled by a control unit UC, which converters are arranged in a series chain that allows them to be synchronized according to the invention to a common reference clock CLK. In practice, this clock is electrically distributed to the control unit and converters using prior-art techniques, in order to ensure the synchronous distribution thereof to all the components.

35 According to the invention, each converter of the chain is configured to

receive a synchronizing signal on an input terminal IN; and to transmit a synchronizing signal to the following converter, via an output terminal OUT. The series chain for distributing the synchronizing signal to the converters according to the invention may thus be formed in the following way: a
 5 synchronizing signal SYNC-m is emitted by the control unit UC of the converters; it is applied to the first converter of the chain and transmitted after resynchronization to the following converter and so on up to the last converter of the chain. The signal received on the input terminal IN of the converter of rank j in the chain is denoted SYNC-in_j; and the signal
 10 transmitted by the converter of rank j via its output terminal OUT, after detection of the signal SYNC-in_j and alignment with a reference-clock active front as will be explained below, is denoted SYNC-out_j. Lastly, for the synchronizing method according to the invention, the synchronizing pulse has a duration (or width) that is at least equal to a CLK clock period, allowing
 15 the active level of the synchronizing signal to be acquired by each converter on at least one of the two, rising and falling, fronts of a CLK clock pulse.

Below, first the procedure for synchronizing converters according to the invention is described and then the procedures for determining the configuration parameters used by this procedure are described.

20 The conventions that have been selected will be specified beforehand: the CLK reference-clock active front to which the synchronization is made is the rising front; the default binary value of the parameters of the synchronization configuration register is zero (0). The synchronizing signal is a synchronizing pulse that is a positive logic pulse. The detection of such a
 25 signal corresponds to the detection or acquisition of an active level, which is, under the chosen convention, the high level. Those skilled in the art will be able to make the necessary transpositions and adaptations for systems using different conventions.

30 Figure 2 schematically illustrates the elements of the synchronizing circuit and synchronization configuration register that are provided in each converter in order to implement the synchronization of the converters of the chain according to the method of the invention.

The synchronizing circuit comprises sequential and combinatorial logic
 35 circuits. A first circuit LS1 allows a function for detecting and re-synchronizing

a synchronizing signal $SYNC_{in_j}$ received as input to be provided. A second circuit LS2 is provided that allows a function for shifting this signal to be provided, in order to allow the frequency dividers of all the converters in the chain to be started in phase when these converters are made up of cores
 5 converting at a lower working frequency than the CLK clock frequency. How the functions of these two first circuits LS1 and LS2 are implemented depends on parameters defined in the synchronization configuration register REG_j . A third circuit LS3 makes it possible to detect whether the CLK clock front positioned by the polarity parameter is indeed the right front. If it is not, it
 10 allows a flag bit $Flag_j$ provided in the configuration register, which is especially used in the setting phase, to be activated in order to correctly determine the value of the polarity parameter for the converter in question.

CIRCUIT LS1 AND POLARITY PARAMETER

15 It has been seen that the polarity parameter $Sel-edge_j$ is the parameter that allows, in each converter, the suitable polarity of the CLK clock front used to reliably acquire the active level of the synchronizing signal to be set.

This parameter is used by the first sequential and combinatorial logic
 20 circuit LS1 of the converter. This circuit LS1 receives as input the synchronizing signal $Sync-in_j$ received via the input terminal IN. It delivers as output the synchronizing signal $Sync-out_j$ that is transmitted to the output terminal. This circuit LS1 is designed, for the signal conventions indicated above, to:

- 25 - detect a synchronizing pulse received as input, on a CLK clock front that may be the rising front or the falling front depending on the value of the polarity parameter $Sel-edge_j$; and
- deliver as output a synchronizing pulse that is synchronous with the reference clock, i.e. aligned with the clock active front, which under the
 30 adopted conventions is the rising front.

Figure 2 shows an exemplary embodiment of this circuit, by way of illustration. In this example, the circuit LS1 comprises two pairs of flip-flops D controlled in master-slave mode, in series.

The first pair provides the detecting function. It is sequenced by an H1 clock signal that is generated by a logic gate, in the example an XOR gate that receives, via one input, the CLK clock signal, and via the other, the inverse of the polarity parameter Sel-edge_i. When Sel-edge_i=0, then
 5 H1=/CLK: that means that detection is on a falling front of CLK (Figure 3); and when Sel-edge_i=1, H1 = CLK: that means that detection is on a rising front of CLK (Figure 4). Thus, the output Qm1 of the master flip-flop of the first pair takes the value of the signal SYNC-in_j applied as input on (during) the low level of the clock H1; and preserves its preceding state on the high
 10 level; as for the output Qe1 of the slave flip-flop of the first pair, the opposite is true: it takes the value of the signal SYNC-in_j applied as input on (during) the high level of the clock H1 and preserves its preceding state on the low level.

The second pair provides the function allowing alignment with a
 15 following CLK clock active front. In this second pair, the master flip-flop is sequenced by an H2 clock signal that is generated by a logic gate, in the example an AND gate that receives, via one input, the CLK clock signal, and via the other, the polarity parameter Sel-edge_i. When Sel-edge_i=0, then H2=0 (Figure 3) and the output Qm2 of this flip-flop permanently copies its input, i.e. the signal Qe1; and when Sel-edge_i=1 (Figure 4), H2 = CLK. The slave
 20 flip-flop of the second pair is sequenced by the reference clock. Its output Qe2 delivers the synchronous synchronizing signal SYNC-out_j to be transmitted via the output OUT.

The timing diagram in Figure 3 corresponds to the case where Sel-edge_i has been set to 0 for this converter, indicating that the active level (1)
 25 of the signal SYNC-in_j that will be (is) received is stable at the moment of a falling front of the clock CLK : detection by the first pair is on a falling front of CLK. Synchronisation by the second pair is on the following rising front of CLK.

30 The timing diagram in Figure 4 corresponds to the opposite case in which Sel-edge_i has been set to 1: i.e. the active level (1) of the signal SYNC-in_j that will be (is) received is stable at the moment of a rising front of the clock CLK : detection by the first pair is on a rising front of CLK and synchronisation by the second pair is on the following falling front of CLK.

It will be noted that in both cases the detection and alignment are carried out over one reference-clock period.

CIRCUIT LS2 AND PHASE PARAMETER

5 It has been seen that the phase parameter $Sel-shift_j$ is the parameter that allows the frequency dividers of the converters to be started in phase. If the converters are each formed with a single converting core the sampling frequency of which is the CLK clock frequency, this parameter is set to its default value (zero) in all the converters. When the converters are each
10 formed with n converting cores, n being an integer at least equal to 2, the sampling clock of the converting cores is delivered by a divider by a factor n of the frequency of the clock CLK.

During the synchronizing procedure, the frequency dividers of the converters will not be reset to the same CLK clock active front, but instead
15 their reset will be delayed depending on the propagation of the synchronizing signal from one converter to the next. However, the phase parameter ensures that they are reset to clock active fronts that considered pairwise are separated from each other by a number that is a multiple of n CLK clock periods. In this way, the sampling clocks all start in phase.

20 The phase parameter is applied to the second circuit LS2 of the synchronizing circuit of the converter. It receives as input the signal $SYNC-out_j$ delivered by the first circuit LS1; it delivers as output the signal $SYNC-Core_j$ applied to reset the sampling clock generator Fe_j (frequency divider) used in the one or more cores of the converter.

25 In practice, the circuit LS2 comprises $n-1$ delay circuits, for example flip-flops D sequenced by the CLK clock signal, each circuit delaying the signal received as input by one CLK clock period; and a multiplexer having n input channels and one output channel, which is controlled by the phase parameter $Sel-shift_j$. This multiplexer receives as input the signal $SYNC-Core_j$
30 and the output of each of the $n-1$ delay circuits, and selects the input channel that corresponds to the shift set by the parameter $Sel-shift_j$.

The timing diagram in Figure 5 illustrates the effects of the circuit LS2 and the phase parameter. It shows the input, output and core synchronizing
35 signals ($SYNC-in_j$, $SYNC-out_j$, $SYNC-Core_j$) of three successive converters of

the chain, which comprise $n=2$ cores working at half the frequency of the CLK clock frequency. In this timing diagram, the output synchronizing signal SYNC-out_j output from the most upstream converter CN_j is taken as a reference. For the two converters CN_j and CN_{j+1}, the active fronts of their output signals SYNC-out_j and SYNC-out_{j+1} are separated by 2 CLK clock periods: these two signals may be applied without shift (Sel-shift_j and Sel-shift_{j+1} = 0): their sampling clocks Fe_j will start in phase. For the two converters CN_j and CN_{j+2}, the active fronts of their output signals SYNC-out_j and SYNC-out_{j+2} are separated by 5 CLK clock periods, which is not a multiple of 2. In the example, a shift of 1 CLK clock period is then added to the signal SYNC-out_{j+2}, to obtain a number that is a multiple of 2 (by setting the phase parameter Sel-shift_{j+2} of the converter CN_{j+2} to the value 1). Thus, the clocks of these three converters Fe_j, Fe_{j+1} and Fe_{j+2} will all start in phase, as illustrated in Figure 5. Thus, the value of the phase parameter of each converter with respect to an upstream converter in the chain is determined.

CIRCUIT LS3 AND FLAG BIT

The flag bit Flag_j of the configuration register of a converter makes it possible to signal to the control unit that the acquisition of the input synchronizing signal SYNC-in_j is not reliable, i.e. that the CLK clock front defined by the polarity parameter for detection of the active level of this signal (circuit LS1) falls in a zone in which this signal is unstable, and that therefore it must be modified. Figure 6 illustrates this situation: the active pulse front of the signal SYNC-in₁ is concomitant with the CLK clock front set by the parameter Sel-edge₁ for the detection, which here is the falling front. This is a zone of instability ZI of the signal and hence the detection is unreliable. The third circuit LS3 of the synchronizing circuit of the converter allows this situation to be detected, and the flag bit Flag_j to be activated where appropriate.

In practice, this circuit LS3 comprises three detecting stages that each receive the input synchronizing signal SYNC-in_j and that are sequenced using the reference clock CLK. A first stage is configured to detect an active level of the signal SYNC-in_j on the CLK clock front determined by the default value of the polarity parameter Sel-edge_j. The two other stages detect on a front (-Δ) slightly ahead of this clock front and a front (+Δ) slightly

therebehind, respectively. At the high frequencies with which we are concerned, this slight positive or negative delay is typically about ten picoseconds (10^{-12} s). If the three stages deliver as output the same logic value, corresponding to the active level of the signal, it means that this level is well established at the time of the detection front. If at least one delivers a different logic value, it means that the signal SYNC-in_j was in the process of rising to the high value (or decreasing to the low value): the detection front is therefore in a zone of instability ZI. The circuit LS3 then activates the flag bit Flag_j in the configuration register, in the example by positioning it to the value 1. In practice, the various detecting stages are designed substantially like the detecting stage of the circuit LS1, while furthermore including delay circuits for generating the detection fronts ahead and behind the reference-clock front. This flag bit is especially used in the setting phase to modify the value of the polarity parameter of the converter. Another use is described below, in the procedure for synchronizing the chain of converters.

PROCEDURE FOR SYNCHRONIZING THE CHAIN OF CONVERTERS

During the setting phase, which will be described below, the control unit UC stores the polarity and phase parameters determined for each converter in memory, for example in a non-volatile memory.

Each time it is turned on, the control unit programmes the configuration registers of each of the converters. It then triggers the procedure for synchronizing the converters.

In one embodiment, this procedure is triggered by the emission by the control unit of a synchronizing signal SYNC-m that is synchronous with the clock CLK, i.e. the pulse is emitted on a CLK clock active front.

By virtue of the polarity and phase parameters configured for each converter, this synchronizing signal will propagate from the first converter to the last converter of each converter chain formed according to the invention, while generating, on passage through each converter, a signal for synchronizing the one or more converting cores, which signal is correctly positioned so that at the end of the procedure, all the sampling clocks will be in phase, as for example illustrated by the timing diagram in Figure 5.

In one variant, provision may be made for the synchronizing procedure to be triggered by the emission by the control unit of a synchronizing signal

SYNC-m that is asynchronous. In this case, there is an uncertainty in the detection of the synchronizing pulse by the first converter CN_1 at the chain input. This uncertainty is removed by making provision for the control unit to verify the state of the flag bit of this converter CN_1 : if it is not activated, it means that the active pulse level was well and stably established at the time of the detection front positioned by the polarity parameter. If it is activated, the control unit emits a new asynchronous synchronizing pulse. Provided that the first converter has correctly detected the input synchronizing pulse, and as it transmits as output a synchronizing signal $SYNC-out_1$ that is by construction synchronous, the synchronizing procedure may continue in the following converters, as described above for a synchronous signal SYNC-m.

Advantageously, the synchronization output terminal of the last converter of the chain is looped back to the control unit: the control unit thus receives an indication of the end of the phase of synchronizing the converters of each chain.

PROCEDURE FOR SETTING THE CONFIGURATION PARAMETERS

For each converter chain formed according to the invention a setting phase is required to configure, in each converter, the polarity and phase parameters of the synchronizing procedure. After the system is turned on, the converters are initialized: in particular the configuration registers of the converters are initialized to a default value, which is generally zero. Therefore, in all the converters: $Sel-edge_j=0$ and $Sel-shift_j=0$. Under the adopted conventions, this means that, in the circuits LS1 of all the converters, the CLK clock front for detection is the falling front; and the circuits LS2 of all the converters select the no-shift synchronization input channel.

The control unit is configured to activate a setting sequence P1, to determine step by step the polarity parameters of the converters, as illustrated by the timing diagram in Figure 6 and the flowchart of steps in Figure 7.

This phase starts with the emission of a synchronizing signal SYNC-m (a pulse) synchronized to a CLK clock active front. The control unit then monitors the converters to detect whether a flag bit is activated.

At the converter level, the sequence is as follows:

The synchronizing pulse emitted by the control unit arrives via the input of the chain at the first converter CN_1 after a set delay (which there is no need to know) that depends only on the characteristics of the conduction pathway of the signal from the output OUT-sync of the control unit to the input IN of this converter (Figure 1). The converter detects the signal SYNC-in₁ received as input (circuit LS1) and verifies (circuit LS3) whether this detection took place in a zone of instability ZI of this signal (step ST-a). If this is not the case, the signal propagates to the following converter CN_2 .

However if, as illustrated in Figure 6, the propagation delay between the output OUT-sync of the control unit and the input IN of this converter is such that the high level of the signal SYNC-in₁ is being reached at about or at the time of the detection front, the falling front in the example, which is the CLK clock front that has the polarity defined by the default value of the polarity parameter Sel-edge₁, the converter (via its circuit LS3) activates its flag bit Flag 1 (step ST-b).

The control unit will then detect the activation of the flag bit Flag₁ of the configuration register of the converter CN_1 and will:

- reset it to zero (step A);
- position to 1 the polarity parameter Sel-edge₁ (step B); and
- launch a new synchronizing sequence P1 (step C).

A new synchronous synchronizing signal SYNC-m is then sent to the first converter of the chain as illustrated in ① in Figure 6. This time round, the polarity parameter of the first converter is suitably positioned: the synchronizing pulse is reliably detected and the converter transmits as output a pulse SYNC-out₁ that is resynchronized to the CLK clock active front, as illustrated in ② in Figure 6.

As above, the synchronizing pulse arrives at the input of the second converter CN_2 after a set delay that depends only on the characteristics of the conduction pathway of the signal from the output of the preceding converter to the input of this converter.

In turn, this converter CN_2 detects the signal SYNC-in₂ received as input (circuit LS1) and verifies (circuit LS3) whether this detection took place in a zone of instability ZI of the signal (step ST-a). If this is not the case, the signal propagates to the following converter, CN_3 .

In the example, as illustrated in ③ in Figure 6, the converter detects a zone of instability ZI for the polarity defined by the parameter SEL-edge₂ (circuit LS3) and activates its flag bit Flag₂ (step ST-b).

As seen above, the control unit detects this; zeros this flag bit Flag₂ (step A); positions to 1 the value of the polarity parameter Sel-edge₂ of the converter CN₂ (step B); and activates a new synchronizing sequence P1 (step C).

A new synchronous synchronizing signal SYNC-m is emitted, as illustrated in ④ in Figure 6.

This time round, the synchronizing signal will be correctly detected and transmitted by the two already parameterized first converters. The propagation delay of the synchronizing pulse from its emission to the input of the third converter is thus well determined and set. It is then possible to determine the polarity parameter suitable for this third converter, as described above. In this way, the polarity parameter that is suitable for each successive converter in the chain is thus determined up to the last one.

It will be noted that this setting procedure is compatible with a synchronizing procedure initiated by the control unit with a synchronizing signal SYNC-m that is synchronous or asynchronous, as has already been described above.

Figures 8 and 9 illustrate one variant of the setting sequence, in which variant the control unit emits an asynchronous synchronizing signal SYNC-m. In this case, the control unit does not modify the polarity parameter of the first converter CN₁ if its flag bit is activated; it resets the flag bit and emits a new asynchronous synchronizing signal SYNC-m, and it repeats this until the first converter correctly detects the signal that it receives as input. The sequence is unchanged for the other converters of the chain. It will be noted that this setting procedure is compatible only with a synchronizing procedure initiated by the control unit with a synchronizing signal SYNC-m that is also asynchronous.

Once all the polarity parameters have been configured, it is then possible to configure the phase parameters Sel-shift_i of the converters of the chain. Specifically, all the propagation delays of the synchronizing signal in

the chain have been determined: the detections are reliable and the synchronizing signals output via the outputs OUT of the converters are all synchronized to a CLK clock active front. It is therefore possible to determine the number of CLK clock periods separating the synchronizing pulse front output from each converter from a synchronizing pulse front output from another converter, and to do so for all the chain. The principle is, as illustrated in Figure 5, to measure the separation between the synchronizing pulse fronts output from two converters, and, when this separation is equal to an integer number M of CLK clock periods that is not a multiple of n, the value of the phase parameter of the most downstream converter is set to the value p such that M+p is a multiple of n. p may therefore be set to 0, 1, ... n-1.

This may be done in various ways, for example by observing, using an oscilloscope, the output signals or synchronizing signals; or it may be done by precise calculation of the propagation delay between the output OUT of a converter and the input IN of the following converter, this calculation taking into account the material of the conductor, its length, characteristics of solder joints, characteristics of the input and output stage, etc.; or even using test sequences generated by the converters. This determination is not carried out, as for the polarity parameter, via an automatic procedure controlled by the control unit. However, once this determination has been carried out, the value of the phase parameter thus determined for each converter is stored in a memory of the control unit. These values are used to configure the converters each time the system is turned on.

The configuration register of each converter thus in practice comprises 1 bit reserved for the flag bit, 1 bit reserved for the polarity parameter and r bits, where $n=2^r$, reserved for the phase parameter.

The invention that has just been described easily accommodates all forms of arrangement of the converters that may be found in architectures for processing data in the various fields of application: an arrangement in series, in parallel, in a tree having a number of branches, etc., or combinations of these arrangements. Figures 10 and 11 give examples of such tree (Figure 10) or hybrid (Figure 11) configurations. The synchronizing method and the associated setting method, which were explained above, apply in the same

way to each of the chains (of one or more converters) formed in these systems.

The invention is not limited to architectures using an SPI bus as master-slave interface bus between the control unit and the converters.

CLAIMS

1. Method for synchronizing digital/analogue and/or analogue/digital data converters to an active front of a common reference clock CLK, characterized in that the converters form at least one series transmission chain allowing a synchronizing signal (SYNC-m) emitted by a unit (UC) for controlling the converters to be transmitted, method such that:
 - the converter (CN₁) of rank 1 in the chain has a synchronization input (IN) connected to a synchronization control output (OUT-sync) of the control unit;
 - each converter (CN_j) of rank j higher than 1 in the chain has a synchronization input (IN) connected to the synchronization output (OUT) of the converter of rank j-1 (CN_{j-1}) in the chain;
 the synchronizing method being characterized in that a procedure for synchronizing the converters of the chain to a reference-clock active front activated by the control unit comprises the following steps, which are controlled by the control unit:
 - a step of initializing, in each converter, a synchronization configuration register (REG_j) including at least one polarity parameter (Sel-Edge_j) defining the polarity of a reference-clock (CLK) front for detection of signals input via the synchronization input (IN) of the converter as the polarity of the reference-clock active front or the inverse polarity; then
 - sending to the synchronization control output (SYNC-out) of the control unit a synchronizing signal (SYNC-m), which is a pulse of width at least equal to one reference-clock period;
 the synchronizing method also being characterized in that each converter in the chain is configured to carry out the following steps:
 - a) a step of detecting, on a CLK reference-clock front, that front has the polarity defined by the value of said polarity parameter (Sel-Edge_j) configured in the converter, a synchronizing signal (SYNC_in_j) input via the synchronization input (IN), and
 - b) a step of aligning with the following reference-clock active front the signal detected in step a), so as to deliver a synchronizing signal aligned with a reference-clock active front, and applying said signal (SYNC-out_j) to the synchronization output (OUT) of the converter.

2. Method according to Claim 1, wherein each converter (CN_j) in the chain is formed from n cores converting at a sampling frequency (Fe_j) that is delivered by a divider by n of the reference-clock frequency, where n is a
 5 nonzero integer, and configured to carry out, following step b), the following steps:

- c) a step of shifting said aligned synchronizing signal obtained in step b) by an integer number of reference-clock (CLK) period(s), which integer number is defined by the value of a phase parameter (Sel-shift_j) delivered by
 10 said configuration register of the converter; and
- d) a step of using the obtained shifted signal (SYNC-Core_j) as a signal for resetting said divider of frequency by n, said integer number defined by the phase parameter having a value comprised between 0 and n-1, inclusive of limits.

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3. Method according to Claim 1 or 2, wherein each converter in the chain is furthermore configured to carry out the following step:

- e) a step of verifying the stability of an active level of the signal (SYNC-in_j) received via the synchronization input (IN) and acquired on the
 20 reference-clock front defined in the detecting step a) by the value of said polarity parameter, by comparing the first value acquired on said detecting front to at least one second value of said signal, which value is acquired on a front that is ahead, by a set time, of said detecting front and to at least one third value of said signal, which value is acquired on a front that is behind, by
 25 a set time, said detecting front, and if the values are not all identical, activating a corresponding flag bit (Flag_j) in said configuration register of the converter.

4. Method according to Claim 3, characterized in that the flag bit of the
 30 configuration register of the converters is used by the control unit in a setting phase (P1) to change the value of the polarity parameter in each converter of a chain, from a first binary value initialized by default to a second binary value, and in that, in said setting phase, the control unit emits a new synchronizing signal each time a flag bit is activated in the configuration
 35 register of a converter of the chain, said setting phase allowing the polarity

parameter of each converter, in succession from the first converter at the input of the chain to the last converter of the chain, to be configured.

5 5. Method according to Claim 4, characterized in that after said step of setting the polarity parameters of the converters, a value p of the phase parameter of each converter is determined on the basis of a determination of the integer number M of reference-clock periods separating the synchronizing pulse front output from the converter via its output (OUT) from the synchronizing pulse front output from an upstream converter in the chain, and the value p of the phase parameter is such that the sum $M+p$ is a multiple of n .

15 6. Method according to any one of the preceding claims, characterized in that the synchronizing signal (SYNC-m) emitted by the control unit is a signal synchronized to an active front of the reference clock CLK.

20 7. Method according to any one of the preceding claims, characterized in that the procedure for synchronizing the converters of the chain comprises the emission, by the control unit, of an asynchronous synchronizing signal (SYNC-m) and in that the control unit emits a new asynchronous synchronizing signal each time the flag bit is activated in the configuration register of the converter (CN₁) of rank 1 at the input of the chain.

25 8. Analogue/digital or digital/analogue data converter comprising an input (IN) for receiving a synchronizing signal and an associated synchronizing circuit allowing the converter to be synchronized to an active front of a reference-clock (CLK) signal, characterized in that the converter comprises a configuration register (REG_j) that may be read from and written to via an interface bus by a control unit (UC) of the converter, said register comprising at least one polarity parameter (SEL-edge_j) defining a reference-clock-front polarity for detection of said synchronizing signal (SYNC-inj) received as input, and in that the synchronizing circuit comprises a detecting circuit (LS1) that comprises:

- a) a stage for detecting, on a reference-clock (CLK) front that has the polarity defined by the binary value of said polarity parameter (Sel_edge_j), an active level of said received synchronizing signal, and

- b) a stage for aligning the synchronizing signal detected by the
 5 detecting stage, which delivers as output (Qe2) a synchronizing signal aligned with a reference-clock (CLK) active front, and said aligned synchronizing signal (SYNC-out_j) is applied to a synchronization output (OUT) of the converter.

10 9. Converter according to Claim 8, which is formed from n cores converting at a sampling frequency (Fe_j) that is delivered by a divider by n of the reference-clock frequency, where n is a nonzero integer, characterized in that the configuration register contains another phase parameter (Sel-shift_j) the value of which is equal to an integer number comprised between 0 and n-1,
 15 inclusive of limits, and in that the synchronizing circuit comprises a shifting circuit (LS2) configured to apply to the signal delivered as output (Qe2) from said aligning stage, a shift of an integer number of reference-clock (CLK) periods, which is given by the value of said phase parameter, and to use the obtained shifted signal (SYNC-Core_j) as a signal for resetting the divider of
 20 frequency by n.

10. Converter according to Claim 8 or 9, wherein the synchronizing circuit comprises a circuit (LS3) for verifying the stability of an active level of the synchronizing signal (SYNC-in_j) received via the input (IN), which comprises
 25 a first stage for acquiring a level of said synchronizing signal (SYNC-in_j) on a reference-clock front having the polarity defined by the value of said polarity parameter, at least one second stage for acquiring a level of said synchronizing signal (SYNC-in_j) on a front that is ahead, by a set time, of said reference-clock front defined in the first stage, and at least one third
 30 stage for acquiring a level of said synchronizing signal (SYNC-in_j) on a front that is behind, by a set time, said reference-clock front defined in the first stage, and if the values delivered by the various stages are not all identical, the output of said verifying circuit activates a flag bit (Flag_j) in said configuration register of the converter.