WHAT IS CLAIMED IS:

1. A memory device comprising:

a memory cell array;

a data path region including data processing blocks that transmit write data to the memory cell array during a write operation and transmit read data from the memory cell array during a read operation; and

a control signal path region including control blocks that controlling the data processing blocks during the write operation and the read operation,

wherein the data path region selectively receives a first high power voltage or a first low power voltage in accordance with an operating mode of the memory device, and

the control signal path region receives the first high power voltage regardless of the operating mode.

2. The memory device of claim 1, wherein the memory device receives the first high power voltage, the first low power voltage, and a second power voltage from an external power management integrated circuit, and

the second power voltage has a higher level than the first high power voltage, and the first high power voltage has a higher level than the first low power voltage.

3. The memory device of claim 1, wherein each of the data processing blocks bidirectionally transmits the data in the data path region, and

each of the control blocks controls a transmission direction of the data by providing a control signal to the data processing block.

4. The memory device of claim 1, wherein the data path region comprises an input/output sense amplifier performing an amplification operation on data, an input/output gating circuit gating data in accordance with a column decoding result, and an input/output buffer transmitting and receiving data to and from an external circuit.

5. The memory device of claim 1, wherein the data path region receives the first high power voltage in a high performance operating mode of the memory device and receives the first low power voltage in a low performance operating mode of the memory device.

6. The memory device of claim 5, further comprising:

a switch unit including one or more switches that selectively provide the first high power voltage or the first low power voltage to the data path region; and

a switch controller that generates a switch control signal controlling the one or more switches.

7. The memory device of claim 6, wherein the switch controller generates the switch control signal based on a result of decoding a command provided from a memory controller, and

the switch unit comprises:

a first switch turned ON in the high performance operating mode to provide the first high power voltage to the data path region; and

a second switch turned ON in the low performance operating mode to provide the first low power voltage to the data path region.

8. The memory device of claim 1, further comprising:

a first power rail transmitting the first high power voltage;

a second power rail transmitting the first low power voltage;

a first internal power rail connected to the first power rail via a first switch and connected to the second power rail via a second switch; and

a second internal power rail connected to the first internal power rail via a third switch,

wherein the data path region receives the first high power voltage or the first low power voltage via at least one of the first internal power rail and the second internal power rail.

9. The memory device of claim 8, wherein the data path region comprises a plurality of data processing blocks, and

at least one of the plurality of data processing blocks receives the first high power voltage or the first low power voltage through the first internal power rail and other ones of the plurality of data processing blocks receive the first high power voltage or the first low power voltage through the second internal power rail.

10. The memory device of claim 8, wherein switching of the first switch and the second switch is controlled based on dynamic voltage and frequency scaling (DVFS) control, and

switching of the third switch is controlled based on power gating control.

11. The memory device of claim 1, wherein the data path region comprises M data processing blocks and the control signal path region includes M control blocks respectively corresponding to the M data processing blocks, where M is an integer greater than 1, and

the memory device further comprises a level shifter selectively arranged on at least one of the M control paths between the M data processing blocks and the M control blocks.

12. The memory device of claim 11, wherein at least one of the M control paths bidirectionally transmit a signal and other ones of the M control paths unidirectionally transmit a signal, and

the level shifter is selectively arranged on at least one of the M control paths bidirectionally transmitting a signal.

13. A memory device comprising:

a memory cell array;

a data path region including data processing blocks transmitting read data from the memory cell array during a read operation and transmitting write data to the memory cell array during a write operation;

a control signal path region including control blocks controlling the data processing blocks during the read operation and write operation;

first and second power rails transmitting power voltages used in the memory device; and

a switch unit including a plurality of switches controlling a connection state between the first and second power rails,

wherein the data path region is connected to the first power rail, the control signal path region is connected to the second power rail, the data path region receives at least two power voltages through the first power rail, and the control signal path region receives one power voltage through the second power rail, and

wherein the data path region selectively receives a first high power voltage or a first low power voltage in accordance with an operating mode of the memory device.

14. The memory device of claim 13, wherein the data path region comprises an input/output sense amplifier for performing an amplification operation on data, an input/output gating circuit for gating data in accordance with a column decoding result, and an input/output buffer for transmitting and receiving data to and from an external circuit.

15. The memory device of claim 13, further comprising:

a third power rail transmitting a second high power voltage; and

a fourth power rail transmitting a second low power voltage,

wherein the memory device receives a first power voltage, the second high power voltage, and the second low power voltage from an external power management integrated circuit, the first power voltage has a higher level than the second high power voltage, and the second high power voltage has a higher level than the second low power voltage, and

wherein the switch unit comprises:

a first switch connecting the first power rail and the third power rail;

a second switch connecting the first power rail and the fourth power rail; and

a third switch connecting the second power rail and the third power rail.

16. The memory device of claim 15, wherein switching of the first switch and the second switch is controlled based on dynamic voltage and frequency scaling (DVFS) control.

17. The memory device of claim 15, further comprising a fifth power rail,

wherein the switch unit further comprises a third switch for connecting the first power rail and the fifth power rail, and

the data path region is further connected to the fifth power rail, at least one of the data processing blocks of the data path region receives the second high power voltage or the second low power voltage through the first power rail, and other ones of the data processing blocks of the data path region receive the second high power voltage or the second low power voltage through the fifth power rail.

18. A method of operating a memory device, wherein the memory device includes a data path region including data processing blocks processing data during memory operations and a control signal path region including control blocks controlling the data processing blocks during the memory operations, the method comprising:

providing a first high power voltage to the data path region and the control signal path region in a normal operating mode;

controlling a switch based on a dynamic voltage and frequency scaling (DVFS) operation as the memory device enters a low performance operating mode; and

continuously providing the first high power voltage to the control signal path region and providing a first low power voltage to the data path region in the low performance operating mode.

19. The method of claim 18, further comprising receiving a command from a memory controller,

wherein the first high power voltage or the first low power voltage is provided to the data path region as a result of decoding the command.

20. The method of claim 18, wherein the data path region is connected to a first power rail transmitting the first high power voltage or the first low power voltage in accordance with a selected operating mode and the control signal path region is connected to a second power rail for transmitting the first high power voltage regardless of the selected operating mode.