WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a substrate;

a device isolation layer defining active regions of the substrate; and

a gate line structure comprising a gate insulating layer and a gate electrode that are buried in a trench of the substrate to cross the active regions,

wherein the trench comprises first trench portions on the device isolation layer and second trench portions on the active regions,

wherein, in the second trench portions, the gate insulating layer overlaps a top surface of the gate electrode;

wherein the gate electrode comprises first electrode portions in the first trench portions and second electrode portions in the second trench portions, and

wherein top surfaces of the second electrode portions are located at a level closer than top surfaces of the first electrode portions to a top surface of the substrate.

2. The semiconductor memory device of claim 1, wherein each of the second trench portions comprises an upper trench comprising a first width and a lower trench comprising a second width that is wider than the first width.

3. The semiconductor memory device of claim 2, wherein, in the second trench portions, the gate electrode is in the lower trench and the gate insulating layer encloses the gate electrode.

4. The semiconductor memory device of claim 3, wherein the gate insulating layer is in the upper trench and the upper trench is free of the gate electrode.

5. The semiconductor memory device of claim 1, wherein the gate line structure further comprises capping insulating patterns in the first trench portions on the top surface of the gate electrode.

6. The semiconductor memory device of claim 5, wherein, in the first trench portions, the capping insulating patterns are in a region defined by an inner side surface of the gate insulating layer and the top surface of the gate electrode.

7. The semiconductor memory device of claim 5, wherein adjacent first and second ones of the capping insulating patterns are spaced apart from each other by one of the active regions, in a plan view.

8. The semiconductor memory device of claim 5, wherein the capping insulating patterns and the gate insulating layer are alternately arranged along a top surface of the gate line structure.

9. The semiconductor memory device of claim 5,

wherein the capping insulating patterns comprise first capping insulating patterns comprising a first width and second capping insulating patterns comprising a second width that is narrower than the first width, and

wherein the first capping insulating patterns and the second capping insulating patterns alternate with each other in a direction that intersects the first width and the second width.

10. The semiconductor memory device of claim 5, wherein the gate electrode protrudes toward a top surface of the substrate, between the capping insulating patterns.

11. The semiconductor memory device of claim 1, further comprising a spacer on an outer side surface of the gate insulating layer,

wherein, in the first trench portions, the spacer is horizontally spaced apart from the gate electrode by the gate insulating layer, and

wherein, in the second trench portions, a bottom surface of the spacer is vertically spaced apart from the top surface of the gate electrode by the gate insulating layer.

12. The semiconductor memory device of claim 1, wherein the top surfaces of the second electrode portions comprise rounded surfaces, respectively.

13. The semiconductor memory device of claim 1, wherein the second electrode portions are wider than the first electrode portions.

14. The semiconductor memory device of claim 1, wherein the second electrode portions comprise protruding portions that protrude toward the top surface of the substrate.

15. The semiconductor memory device of claim 14, wherein the protruding portions comprise doped silicon.

16. The semiconductor memory device of claim 1,

wherein the gate electrode comprises a lower gate electrode and an upper gate electrode,

wherein the lower gate electrode comprises a lower metal electrode layer and a lower barrier electrode layer, and

wherein the upper gate electrode comprises an upper metal electrode layer and a work-function adjusting layer enclosing at least a portion of the upper metal electrode layer.

17. A semiconductor memory device comprising:

a substrate;

a device isolation layer defining active regions of the substrate; and

a gate line structure buried in a trench in the substrate to cross the active regions,

wherein the gate line structure comprises a gate insulating layer and a gate electrode in the trench,

wherein the gate electrode comprises first electrode portions on the device isolation layer and second electrode portions on the active regions,

wherein the second electrode portions are wider than the first electrode portions;

wherein top surfaces of the first electrode portions are farther than top surfaces of the second electrode portions from a top surface of the substrate.

18. The semiconductor memory device of claim 17, wherein bottom surfaces of the second electrode portions are closer than bottom surfaces of the first electrode portions to a top

surface of the substrate.