

PROCESS FOR MANUFACTURING ELECTRONIC-COMPONENT
PACKAGES AND ELECTRONIC-COMPONENT PACKAGE OBTAINED BY
MEANS OF THIS PROCESS

5 [0001]

The invention relates to the field of processes for manufacturing electronic-component packages, such as, for example, QFN integrated-circuit packages (QFN being the acronym of "Quad Flat No-Lead").

[0002]

10 Processes for manufacturing electronic-component packages are already known, in which segments of electrical circuits are produced continuously, to which segments an electronic component (electronic chip, light-emitting diode, etc.) is connected, which electronic component is then encapsulated, by injection overmolding or by potting, in a resin. Electrical-circuit segments equipped with an
15 electronic component are then singulated, in order to be used for example as surface mount components or SMCs.

[0003]

For example, document EP2846355A1 describes a process in which

- a dielectric material is provided in the form of a strip, this strip extending
20 in a longitudinal direction and having two main faces, one of which is at least partially covered with a sheet of electrically conductive material,

- a plurality of connection units is produced in the sheet of electrically conductive material, these connection units being distributed along the longitudinal direction with a determined pitch, each connection unit comprising a
25 connection face with connection pads, these connection pads being intended for the electrical connection of the integrated-circuit package, for example to a printed circuit board,

- an electronic component is placed on the strip in each connection unit and connected to at least some of the connection pads of the connection unit in
30 which it is placed, and

- the electronic component is potted in an encapsulation material, in each connection unit.

[0004]

In this process, the electronic component is placed in a cavity formed in a package that is injection overmolded on the strip and in a mold, in each connection unit. Next, the electronic component is potted in a resin deposited in
5 this cavity.

[0005]

The invention proposes another process for manufacturing integrated-circuit packages.

[0006]

10 This process corresponds to claim 1.

[0007]

Thus, the electronic component is also placed in a cavity before its encapsulation (or potting; in this text the terms potting and encapsulation are used synonymously, as are potted and encapsulated), but on the one hand this
15 cavity is produced differently, and on the other hand the encapsulation is carried out by dispensation, i.e. by depositing the encapsulation material in the cavity, without using a mold. The cavity is blind. Its bottom is formed from a layer of flexible and removable material that is removed after encapsulation of the electronic component.

20 [0008]

By virtue of the invention, the electronic component may be encapsulated by potting, in a plastic, a resin, etc. after having been deposited on a carrier, without it being necessary, beforehand, to form a package by injecting a plastic into a mold, or to use an independent mold to inject the potting material. The
25 process according to the invention makes it possible to use at least one or more than one of the materials (dielectric material, electrically conductive material, etc.), which are furthermore required to produce the connection tracks, to form at least one portion of a blind cavity which will then be used to accommodate the encapsulation material.

30 [0009]

The process according to the invention notably allows QFN integrated-circuit packages in which an electronic component (in the present case an

electronic chip) is encapsulated to be produced, with a view to forming miniaturized components for surface mounting (SMCs). It may also be employed to produce SIM cards (SIM being the acronym of "Subscriber Identity Module") with flush contacts for an electrical connection with the device in which this SIM
5 card is inserted.

[0010]

The process according to the invention optionally comprises one or another of the features mentioned in claims 2 to 7, considered in isolation or in combination with one or more others.

10 [0011]

According to another aspect, the invention relates to an electronic-component package intended for surface mounting on an electrical circuit, this package being manufactured using a process such as that mentioned above. The features of this package correspond to those mentioned in claim 8.

15 [0012]

The electronic-component package according to the invention optionally comprises one or another of the features mentioned in claims 9 to 11, considered in isolation or in combination with one or more others.

[0013]

20 Other features and advantages of the invention will become apparent on reading the following detailed description, and from the appended drawings. In these drawings:

- figures 1a to 1m schematically show the various steps of a first example of implementation of the process according to the invention;

25 - figure 2 shows a top view of an example of an electrical-circuit strip at various stages of a process according to the invention; figure 2A shows an enlarged portion of figure 2;

- figure 3 shows an electrical-circuit-connection unit for implementing a process according to the invention, before an electronic component has been
30 placed in this connection unit;

- figure 4 shows the electrical-circuit-connection unit of figure 3, after an electronic component has been placed and overmolded in this connection unit;

- figure 5 schematically shows a bottom view of an example of an integrated-circuit package obtained using a process according to the invention;

5 - figure 6 schematically shows in perspective the integrated-circuit package of figure 5; and

- figures 7a to 7j schematically show the various steps of a second example of implementation of the process according to the invention.

[0014]

10 A first example of implementation of the process according to the invention is shown in figure 1. It is described below in relation to the manufacture of a QFN integrated-circuit package. This example of implementation comprises the following steps:

[0015]

15 - a strip 10 of dielectric material is provided (figure 1a); for example, the dielectric material is glass-epoxy, flexible and in a roll (for an implementation of a so-called “roll-to-roll” or “reel-to-reel” process); the strip 10 extends in a longitudinal direction L along which it is unwound; this strip 10 has two main faces 10A, 10B; the strip 10 has a thickness for example of 75 μm or 110 μm ;

20 [0016]

- the strip 10 of dielectric material is coated, at least partially, on one of its main faces 10A, 10B (in the present case on the main face 10A) with an adhesive 20 (modified epoxy resin) that is reactivatable under heat (figure 1b);

[0017]

25 - perforations 30 are produced in the strip 10 of dielectric material coated with the adhesive 20 to form drive notches on the edges of the strip 10 of dielectric material and cavities; these perforations 30 are produced for example by punching; the cavities are distributed with a pitch defined by the desired distance between the integrated-circuit packages (figure 1c);

30 [0018]

- a sheet 40 of electrically conductive metal material is laminated to face 10A of the strip 10 of dielectric material comprising the adhesive 20 (figure 1d);

this sheet 40 of electrically conductive material is for example a sheet of copper
- or of one of its alloys - of 70 μm thickness;

[0019]

- the sheet 40 of electrically conductive material is etched, for example by
5 photolithography, to define and produce patterns 50 (alternatively the patterns 50
are completely, or only partially, cut mechanically before lamination of the sheet
40 of electrically conductive material to the face of the strip 10 of dielectric
material comprising the adhesive 20); these patterns 50, and the connection units
which they comprise are distributed along the longitudinal direction L with a set
10 pitch; the patterns 50 notably comprise connection units connected by conductive
tracks (figure 1e and figure 2); in this step, in at least some connection units, a
blind or non-through cavity 60 remains on one side of the strip 10 of dielectric
material; either or both of the two faces of the sheet 40 of electrically conductive
material are optionally metallized; this (for example Ni/Au or Ag) metallization is
15 for example suitable for processes for transferring QFN components to an
electrical circuit and/or for processes for connecting connection pads to the
electronic component 90 (see below in relation to figure 1i);

[0020]

- other pattern elements 55 (for example comb-shaped elements, see
20 figure 1f and figure 2) are then cut, by mechanical punching or by chemical
etching, into the sheet 40 of electrically conductive material, in the cavity 60, in
order to form the connection pads 45; a through-aperture 70 is also formed in the
center of each connection unit between the connection pads 45; the connection
pads 45 allow, on the one hand, the QFN component to be connected to an
25 electrical circuit and, on the other hand, an electronic component 90 to be
connected (figure 1f and figure 1i);

[0021]

- a layer 80 of removable and flexible material, intended to close the cavity
60 on the side of the sheet 40 of electrically conductive material, is temporarily
30 deposited on this sheet 40 of electrically conductive material (figure 1g); this layer
80 of removable material consists for example of a strip with a non-permanent
adhesive or comprises a face coated with a non-permanent adhesive; it may be

for example a polypropylene film coated with a layer of rubber-based adhesive, or a polyimide film coated with a layer of silicone-based adhesive; optionally, the adhesive layer is protected by a protective non-stick film; it may be the product of reference 1285 from the company SCAPA, or of reference SMX-P3OS from the company SEEMEX Inc. (a company based in Seoul, South Korea) or of reference PS1030-06A from the brand INNOX (sold by Shinha Inc. based in Gyungi Do, South Korea); this layer 80 of removable material forms a bottom for the openings 70 cut in the previous step; a blind or non-through cavity 60 is thus formed; the cavity 60 is therefore closed by a bottom consisting of the removable layer 80 and on its periphery by the edge face cut in the strip 10 of dielectric material and in the sheet 40 of electrically conductive material; the removable layer 80 makes contact with the connection pads 45 and thus protects one of their faces during the subsequent encapsulation step;

[0022]

15 - an electronic component 90 (for example an electronic chip) is deposited in the cavity 60, for example on an adhesive face of the removable layer 80 deposited in the previous step (figure 1h);

[0023]

20 - the electronic component 90 is connected for example using a wire-bonding or flip-chip technique to the connection pads 45 (in the example illustrated in this document, the connection pads 45 and the connection lands of the electronic component 90 are wire bonded - see figure 1i);

[0024]

25 - the connection pads 45 are isolated from each other by punching in order to allow the QFN components to be electrically tested individually (figure 1j); in figure 1j and in figures 3 and 4, the dashed lines schematically represent the short-circuit 48 present in the electrically conductive sheet 40, before this step allowing the connection pads 45 to be electrically isolated from one another; thus, after this step, although the electronic-component packages 110 have not yet been singulated (see below), it is possible to mount an electronic component 90, and to connect it to the connection pads 45, then to test it; this step is optional,

30

notably if the electronic components 90 are tested only after singulation of their respective package 110 (see figures 5 and 6);

[0025]

- the electronic component 90, the connection pads 45 and a portion of the strip 10 of dielectric material are encapsulated, for example by dispensing (for example using the technology referred to as “dam & fill”) thermosetting resin, with an encapsulation material 100, here and there, to form the QFN components with the desired pitch (figure 1k); a product of reference “Delo DF570-580” may be used as encapsulation material; in this case, this product corresponds to a “black thermal resin for encapsulation”;

[0026]

- the removable layer 80 intended to close the cavity on the side of the electrically conductive sheet 40 is removed (peeled off) (figure 11);

[0027]

- the QFN packages 110 or modules are then electrically tested and singulated by dicing (figure 1m), before a subsequent pick-and-place step in which they are transferred to an electrical circuit.

[0028]

It will be noted that the steps of figures 1a) to 1g), for example, which relate to the manufacture of a carrier (structure corresponding to the strip 10 of dielectric material, the adhesive 20 and the sheet 40 of electrically conductive material) may be carried out by one manufacturer, while the following steps, which relate to the transfer and connection of an electronic component 90 to this carrier, may be carried out by another manufacturer.

[0029]

Figure 2 schematically shows a strip 10 of dielectric material with patterns etched in the sheet 40 of electrically conductive material. By way of illustration, the respective results of various steps of the aforementioned process are shown in the same figure (figure 2), whereas in fact these steps are implemented one after another. The patterns 50 comprise conductive tracks 52 and connection units 54. The conductive tracks 52 serve notably to distribute electric current during an electrodeposition implemented for the metallization of the connection

pads 45. In this figure, connection units 54 are shown after the connection pads 45 have been cut (see also figure 3). In one of the connection units 54 (see enlarged area 2A), the areas of the cutouts 56 produced by punching to isolate the connection pads 45 from one another are also shown (see also figure 4).
5 Moreover, dashed lines 58 delineate the area that will subsequently be cut out after encapsulation of the electronic component 90 and of its connections (see also figures 5 and 6). It will be noted that if the connection pads 45 have not already been isolated from each other in a step such as that shown in figure 1j), they may be isolated concomitantly in the final step of singulation of the
10 electronic-component packages 110 (figure 1m).

[0030]

Figure 6 shows in particular an electronic-component package 110 obtained using the above process. This electronic-component package 110 is an element intended for surface mounting on an electrical circuit (a printed circuit
15 board for example). It comprises a connection face 112, and at least one electronic component 90 potted (encapsulated) in an encapsulation material 100 is connected to connection pads 45 that are flush, just like one face of the electronic component 90, on the connection face 112, with the encapsulation material 100. This package 110 comprises two rows of connection tracks 45.
20 They are located on the connection face 112, each respectively next to a side 114 and an edge of the package 110, the two sides 114 of the package 110 each comprising one row of connection tracks 45 that are opposite one another. These connection tracks 45 are therefore either directly connected to the electronic component 90 (so-called flip-chip technology), or connected to the electronic
25 component 90 by bonding wires (so-called wire-bonding technology).

[0031]

A second example of implementation of the process according to the invention is shown in figure 7. It is described below in relation to the manufacture of an QFN integrated-circuit package. This example of implementation comprises
30 the following steps:

[0032]

- a strip 10 of dielectric material is provided (figure 7a); for example, the dielectric material is glass-epoxy, flexible and in a roll (for an implementation of a so-called "roll-to-roll" or "reel-to-reel" process); the strip 10 extends in a longitudinal direction L along which it is unwound; this strip 10 has two main faces 10A, 10B; the strip 10 has a thickness for example of 75 μm or 110 μm ;

[0033]

- the strip 10 of dielectric material is coated, at least partially, on one of its main faces 10A, 10B (in the present case the main face 10A) with an adhesive 20 (figure 7b) suitable for temporarily bonding the dielectric material 10 to an electrically conductive material 40 (figure 7d); the complex thus produced with the strip 10 covered with the adhesive forms a layer of flexible and removable material 80';

[0034]

- perforations 30 are produced in the strip 10 of dielectric material coated with the adhesive 20; in particular, cavities are produced, for example by punching, to form drive notches on the edges of the strip 10 of dielectric material (figure 7c);

[0035]

- a sheet 40 of electrically conductive metal material is laminated to face 10A of the strip 10 of dielectric material comprising the adhesive 20 (figure 7d); this sheet 40 of electrically conductive material is for example a sheet of copper - or of one of its alloys - of 105 μm minimum thickness;

[0036]

- the sheet 40 of electrically conductive material is etched, for example by photolithography, to define and produce patterns (alternatively the patterns are completely, or only partially, cut mechanically before lamination of the sheet 40 of electrically conductive material to the strip 10 of dielectric material) (figures 7e and 7f); these patterns, and the connection units which they comprise are distributed along the longitudinal direction L with a set pitch; the patterns comprise notably connection units connected by conductive tracks; in this step, the connection units therefore comprise a blind or non-through cavity 60 on one

side of the dielectric material; either or both of the two faces of the sheet 40 of electrically conductive material are optionally metallized; this (for example Ni/Au or Ag) metallization is for example suitable for processes for transferring QFN components to an electrical circuit and/or for connecting connection pads 45 to the electronic component 90 (see also below in relation to figure 7g);

[0037]

- an electronic component 90 is deposited in a cavity 60 (figure 7f);

[0038]

- the electronic component 90 is connected for example using a wire-bonding or flip-chip technique to the connection pads 45 (in the example illustrated in this document, the connection pads 45 and the connection lands of the electronic component 90 are wire bonded - see figure 7g);

[0039]

- the electronic component 90, the connection pads 45 and a segment of the dielectric material are encapsulated for example in a resin 100 (to form what is called a glob-top), by filling the cavities 60 here and there by dispensation, to form the QFN components with the desired pitch (figure 7h);

[0040]

- optionally, the resin 100 is flattened or tamped down (figure 7h');)

[0041]

- the strip 10 of dielectric material is removed (peeled off) (figure 7i) (with the adhesive 20); the strip 10 of dielectric material therefore played the role of a layer of flexible and removable material; the electronic components 90 or QFN modules are then electrically tested and singulated for a subsequent pick-and-place step in which they are transferred to an electrical circuit; this step may be concomitant with or consecutive to a step of deshort-circuiting the connection pads 45; this step may be concomitant with or consecutive to a step of cutting edges of the cavity 60 in the conductive material (figure 7j).

[0042]

The electronic components 90 obtained by this second mode of implementation of the process according to the invention are alike or similar to

those that are, or could have been, obtained using the first example and illustrated in figures 2 to 6.

It will be noted that the steps of figures 7a) to 7e), for example, which relate to the manufacture of a carrier, may be carried out by one manufacturer, while the
5 following steps, which relate to the transfer and connection of an electronic
component 90 to this carrier, may be carried out by another manufacturer.

Claims

1. A process for manufacturing integrated-circuit packages, wherein
 - a dielectric material is provided in the form of a strip (10) extending in a longitudinal direction (L), this strip (10) having two main faces (10A, 10B), one of which (10A) is at least partially covered with a sheet (40) of electrically conductive material,
 - a plurality of connection units (54) is produced in the sheet (40) of electrically conductive material, these connection units (54) being distributed along the longitudinal direction (L) with a determined pitch, each connection unit (54) comprising a connection face (112) with connection pads (45), these connection pads (45) being intended for the electrical connection of the integrated-circuit package (110),
 - an electronic component (90) is placed in each connection unit (54) in a blind cavity (60), the bottom of this blind cavity (60) being formed from a layer of flexible and removable material (80, 80'),
 - an electronic component (90) is connected to at least some of the connection pads (45) of the connection unit (54) in which it is placed,
 - the electronic component (90) is potted in an encapsulation material (100),
 - in each connection unit (54),
 - the layer of flexible and removable material (80, 80') is removed after encapsulation of the electronic component (90),
 - characterized in that the electronic component (90) is potted in an encapsulation material (100) by dispensing this material into the blind cavity (60).
2. The process as claimed in claim 1, wherein the connection pads (45) make contact with the layer of flexible and removable material (80, 80'), before the latter is removed, and are flush, on the connection face (112), with the encapsulation material (100) after the layer of flexible and removable material (80, 80') has been removed.

3. The process as claimed in claim 1 or 2, comprising, before encapsulation of the electronic component (90), a step consisting in isolating at least some of the connection pads (45) from one another.
- 5 4. The process as claimed in claim 1 or 2, comprising, after encapsulation of the electronic component (90), a step consisting in isolating at least some of the connection pads (45) from one another.
5. The process as claimed in claim 4, wherein the step consisting in isolating
10 at least some of the connection pads (45) from one another is concomitant with a step consisting in singulating electronic components (90) each respectively corresponding to one connection unit (54).
6. The process as claimed in one of the preceding claims, wherein the layer of
15 flexible and removable material (80) comprises a face coated with a non-permanent adhesive.
7. The process as claimed in one of the preceding claims, implemented roll to roll, wherein the connection pads (45) are isolated from one another and wherein
20 the electronic components (90) are electrically tested individually before singulation.
8. An electronic-component package intended for surface mounting on an electrical circuit, this component package (110) being manufactured using a
25 process according to one of the preceding claims, comprising a connection face (112) and at least one electronic component (90) that is encapsulated in an encapsulation material (100) and is connected to connection pads (45), which connection pads (45) and electronic component (90) are flush, on the connection face (112), with the encapsulation material (100).

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9. The package as claimed in claim 8, wherein the encapsulation material (100) is contained in a cavity (60) that is at least partly limited on its periphery by an edge of the strip (10) of dielectric material.

5 10. The package as claimed in one of claims 8 and 9, comprising at least two rows of connection tracks each located on the connection face (112) on one side (114) of the component package (110), these connection tracks being either directly connected to the electronic component (90) or connected to the electronic component (90) via connection wires.

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11. The package as claimed in one of claims 8 to 10, wherein one face of the electronic component (90) is flush, on the connection face (112), with the encapsulation material (100) and with the connection pads (45).