

WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:
 - a semiconductor chip whose top surface is exposed;
 - a package substrate having a top surface on which the semiconductor chip is mounted and a bottom surface opposite to the top surface, wherein the package substrate comprises a first flexible substrate and a second flexible substrate;
 - an upper metal pattern layer on the top surface of the package substrate, the upper metal pattern layer having an upper connection region extending along one section of the top surface of the package substrate and dedicated for electrically connecting an external electrical device to the semiconductor package, and the upper metal pattern layer having a chip connection region at which the semiconductor chip is electrically connected to the upper metal pattern layer;
 - a lower metal pattern layer on the bottom surface of the package substrate, the lower metal pattern layer having a lower connection region extending along one section of the bottom surface of the package substrate and dedicated for electrically connecting another external electrical device to the semiconductor package; and
 - an intermediate metal pattern layer in the package substrate and electrically connecting the upper metal pattern layer and the lower metal pattern layer,
- wherein the upper metal pattern layer comprises a plurality of first metal patterns comprising leads extending in a longitudinal direction on the top surface of the package substrate,
- the first metal patterns are disposed in a plurality of groups on the chip connection region,
- in each of the groups of the first metal patterns, the first metal patterns are spaced relative to each other in a direction intersecting the longitudinal direction in

which the leads of the upper metal pattern layer extend, whereas the groups of the first metal patterns are offset from each other in the longitudinal direction in which the leads of the upper metal pattern layer extend,

the intermediate metal pattern layer comprises a plurality of second metal patterns,

the lower metal pattern layer comprises a plurality of third metal patterns comprising leads extending longitudinally on the bottom surface of the package substrate,

in each of the groups of the third metal patterns, the third metal patterns are spaced relative to each other in a direction intersecting the longitudinal direction in which the leads of the lower metal pattern layer extend, whereas the groups of the third metal patterns are offset from each other in the longitudinal direction in which the leads of the lower metal pattern layer extend, and

the semiconductor package further comprising:

a plurality of first metal vias extending through the first flexible substrate and electrically connecting the first metal patterns to the second metal patterns; and

a plurality of second metal vias extending through the second flexible substrate and electrically connecting the second metal patterns to the third metal pattern,

wherein, at least, one of the plurality of first metal vias is vertically aligned with one of the plurality of second metal vias.

2. The package of claim 1, wherein

the first flexible substrate includes a top surface on which the upper metal pattern layer is provided and a bottom surface on which the intermediate metal pattern layer is provided; and

the second flexible substrate includes a top surface facing the bottom surface

of the first flexible substrate and a bottom surface on which the lower metal pattern layer is provided.

3. The package of claim 1 or claim 2, further comprising a plurality of connection terminals interposed between the semiconductor chip and the package substrate,

wherein the connection terminals comprise:

a plurality of first output terminals arrayed in a first direction;

a plurality of second output terminals arrayed in the first direction, the plurality of second output terminals being offset in a second direction relative to the plurality of first output terminals, the second direction intersecting the first direction;

a plurality of third output terminals arrayed in the first direction, the plurality of third output terminals being offset in the second direction relative to plurality of the second output terminals; and

a plurality of input terminals arrayed in the first direction, the plurality of input terminals being offset in the second direction relative to the plurality of third output terminals.

4. The package of claim 3, wherein the first metal patterns of the upper metal pattern layer comprise:

a plurality of first outer metal patterns electrically connected to the first output terminals and constituting a first one of said groups of the first metal patterns;

a plurality of first intermediate metal patterns electrically connected to the second output terminals and constituting a second one of said groups of the first metal patterns;

a plurality of first inner metal patterns electrically connected to the third output

terminals and constituting a third one of said groups of the third metal patterns; and
a plurality of input metal patterns electrically connected to the input terminals
and constituting a fourth one of said groups of the third metal patterns.

5. The package of claim 4, wherein the input metal patterns comprise outer leads constituting the upper connection region.

6. The package of claim 4 or claim 5, wherein the first outer metal patterns comprise leads extending longitudinally from below the first output terminals in a direction away from the upper connection region,

the first intermediate metal patterns comprise metal pads disposed directly under the second output terminals, respectively, and

the first inner metal patterns comprise leads extending longitudinally in a direction from below the third output terminals toward the upper connection region and/or the first inner metal patterns comprise metal pads disposed directly under the third output terminals.

7. The package of any one of claims 3 to 6, wherein the plurality of second metal patterns of the intermediate metal pattern layer comprises:

a plurality of second outer metal patterns electrically connected to the first output terminals;

a plurality of second intermediate metal patterns electrically connected to the second output terminals; and

a plurality of second inner metal patterns electrically connected to the third output terminals,

wherein the second intermediate metal patterns extend from below the second

output terminals to locations toward a region vertically aligned with the lower connection region.

8. The package of any one of claims 3 to 7, wherein the plurality of third metal patterns of the lower metal pattern layer comprise:

a plurality of third outer metal patterns electrically connected to the first output terminals and constituting a first one of said groups of the third metal patterns;

a plurality of third intermediate metal patterns electrically connected to the second output terminals and constituting a second one of said groups of the third metal patterns; and

a plurality of third inner metal patterns electrically connected to the third output terminals and constituting a third one of said groups of the third metal patterns,

wherein the third inner metal patterns extend from below the third output terminals and constitute the lower connection region of the lower metal pattern layer.

9. The package of claim 8, wherein the third outer metal patterns comprise metal pads constituting the lower connection region, the third intermediate metal patterns comprise metal pads constituting the lower connection region, and the third inner metal patterns comprise metal pads constituting the lower connection region,

the metal pads of the third outer metal patterns are disposed in a row as spaced from each other, the metal pads of the third intermediate metal patterns are disposed in a row as spaced from each other, and the metal pads of the third inner metal patterns are disposed in a row as spaced from each other, and

in each said row of the metal pads, the metal pads of the row are spaced from each other in a direction intersecting the longitudinal direction in which the leads of the lower metal pattern layer extend, whereas the rows of the metal pads are spaced from

each other in the longitudinal direction in which the leads of the lower metal pattern layer extend.

10. The package of claim 8, wherein the third outer metal patterns comprise a plurality of metal pads electrically connected to the first output terminals and constituting the lower connection region of the lower metal pattern layer,

the third intermediate metal patterns comprise a plurality of metal pads electrically connected to the second output terminals and constituting the lower connection region of the lower metal pattern layer, and

the third inner metal patterns comprise a plurality of metal pads electrically connected to the third output terminals and constituting the lower connection region of the lower metal pattern layer.

11. The package of any one of claims 1 to 10, wherein
the plurality of first metal vias comprises an upper metal via extending vertically and electrically connecting the upper metal pattern layer and the intermediate metal pattern layer; and

the plurality of second metal vias comprises a lower metal via extending vertically between and electrically connecting the intermediate metal pattern layer and the lower metal pattern layer.

12. The package of any one of claims 1 to 11, further comprising a plurality of additional electrical patterns on opposite ends of the package substrate.

13. The package of claim 12, wherein the upper metal pattern layer, the lower metal pattern layer, and the intermediate metal pattern layer collectively extend

toward the opposite ends of the package substrate, and each of the additional electrical patterns is integral with one of upper metal pattern layer, the lower metal pattern layer, and the intermediate metal pattern layer.

14. A semiconductor package, comprising:
 - a semiconductor chip whose surface is exposed;
 - a first flexible substrate having a first top surface on which the semiconductor chip is mounted and a first bottom surface opposite to the first top surface;
 - a second flexible substrate having a second top surface facing the first bottom surface and a second bottom surface opposite to the second top surface;
 - a first metal pattern layer on the first top surface, the first metal pattern layer including a chip connection region at which the semiconductor chip is electrically connected to the first metal pattern layer and an upper connection region dedicated for electrically connecting the semiconductor package to an external electrical device, the upper connection region located along a section of the first top surface;
 - a second metal pattern layer on the first bottom surface and electrically connected to the first metal pattern layer; and
 - a third metal pattern layer on the second bottom surface and electrically connected to the second metal pattern layer, the third metal pattern layer having a lower connection region on a section of the second bottom surface, the lower connection region dedicated for electrically connecting another external electrical device to the semiconductor package,
- wherein the first metal pattern layer comprises a plurality of first metal patterns comprising leads extending in a longitudinal direction on the first top surface,
- the first metal patterns are disposed in a plurality of groups on the chip connection region,

in each of the groups of the first metal patterns, the first metal patterns are spaced relative to each other in a direction intersecting the longitudinal direction in which the leads of the first metal pattern layer extend, whereas the groups of the first metal patterns are offset from each other in the longitudinal direction in which the leads of the first metal pattern layer extend,

the second metal pattern layer comprises a plurality of second metal patterns on the first bottom surface,

the third metal pattern layer comprises a plurality of third metal patterns comprising leads extending longitudinally on the second bottom surface,

in each of the groups of the third metal patterns, the third metal patterns are spaced relative to each other in a direction intersecting the longitudinal direction in which the leads of the third metal pattern layer extend, whereas the groups of the third metal patterns are offset from each other in the longitudinal direction in which the leads of the third metal pattern layer extend, and

the semiconductor package further comprising:

a plurality of first metal vias extending through the first flexible substrate and electrically connecting the first metal patterns to the second metal patterns; and

a plurality of second metal vias extending through the second flexible substrate and electrically connecting the second metal patterns to the third metal patterns,

wherein, at least, one of the plurality of first metal vias is vertically aligned with one of the plurality of second metal vias.

15. The package of claim 14, further comprising:

a plurality of connection terminals interposed between the semiconductor chip and the first flexible substrate.

16. The package of claim 15, wherein the connection terminals comprise:
a plurality of first output terminals, the first output terminals being spaced relative to each other along a first direction;
a plurality of second output terminals, the second output terminals being spaced relative to each other along the first direction, and the plurality of second output terminals being offset in a second direction from the plurality of first output terminals, the second direction intersecting the first direction;
a plurality of third output terminals, the third output terminals being spaced relative to each other along the first direction, and the plurality of third output terminals being offset in the second direction from the plurality of second output terminals; and
a plurality of input terminals, the input terminals being spaced relative to each other along the first direction, and the plurality of input terminals being offset in the second direction from the plurality of third output terminals,
wherein the first direction is parallel to the direction intersecting the longitudinal direction in which the leads of the third metal pattern layer extend, and the second direction is parallel to the longitudinal direction in which the leads of the third metal pattern layer extend.

17. The package of claim 16, wherein the first metal pattern layer comprises:
a plurality of first outer metal patterns electrically connected to the first output terminals and constituting a first one of the groups of the first metal patterns;
a plurality of first intermediate metal patterns electrically connected to the second output terminals and constituting a second one of the groups of the first metal patterns;
a plurality of first inner metal patterns electrically connected to the third output terminals and constituting a third one of the groups of the first metal patterns; and

a plurality of input metal patterns electrically connected to the input terminals and partially exposed on the first top surface so as to constitute the upper connection region,

wherein each of the first outer metal patterns and the input metal patterns comprise a respective one of the leads of the first metal pattern layer, and each of the first intermediate metal patterns and the first inner metal patterns comprise a respective one of the leads of the first metal pattern layer and/or each of the first outer metal patterns and the input metal patterns comprise a metal pad.

18. The package of claim 16 or claim 17, wherein the second metal pattern layer comprises:

a plurality of second outer metal patterns electrically connected to the first output terminals;

a plurality of second intermediate metal patterns electrically connected to the second output terminals; and

a plurality of second inner metal patterns electrically connected to the third output terminals,

wherein respective ones of the second intermediate metal patterns extend along the second direction from below the second output terminals toward a region vertically aligned with the lower connection region, and

others of the second intermediate metal patterns extend along the second direction from below the second output terminals toward a region vertically aligned with the upper connection region.

19. The package of any one of claims 16 to 18, wherein the third metal pattern layer comprises:

a plurality of third outer metal patterns electrically connected to the first output terminals and constituting a first one of the groups of the third metal patterns;

a plurality of third intermediate metal patterns electrically connected to the second output terminals and constituting a second one of the groups of the third metal patterns; and

a plurality of third inner metal patterns electrically connected to the third output terminals and constituting a third one of the groups of the third metal patterns,

wherein respective ones of the third inner metal patterns extend along the second direction from below the third output terminals and constitute the lower connection region, and

others of the third inner metal patterns extend along the second direction from below the third output terminals toward a region vertically aligned with the upper connection region.

20. The package of any one of claims 14 to 19, wherein the first and second flexible substrates are made of insulating materials.