CLAIMS

1. An apparatus for performing a scan test of IC chip including a test target circuit by inputting a scan pattern to a scan path via a scan input port of the IC chip, comparing an output pattern outputted via a scan output port with a predetermined expected pattern, and determining whether or not the IC chip is defective based on a result of comparing the output pattern with the predetermined expected pattern, the apparatus comprising:

a shift-frequency searching unit configured to search a usable shift frequency for a target scan section from among at least one scan section each including a whole or a part of at least one scan pattern inputted to the scan path, wherein

when searching the usable shift frequency for the target scan section, the shift-frequency searching unit is configured to search a shift frequency with which a result of the scan test indicates a pass or a shift frequency with which the result of the scan test indicates a fail, by increasing or decreasing a shift frequency of the target scan section differently from that of at least one scan section among other scan sections shifted to the scan path before or after the target scan section or by setting the shift frequency of the target scan section differently from that of the at least one scan section among the other scan sections.

2. The apparatus according to claim 1, wherein when searching the usable shift frequency for the target scan section, the shift-frequency searching unit is configured to search a shift frequency in a frequency range where the result of

the scan test changes from the pass to the fail or a shift frequency in a frequency range where the result of the scan test changes from the fail to the pass, by increasing or decreasing the shift frequency of the target scan section.

3. The apparatus according to claim 1 or 2, wherein when searching the usable shift frequency for the target scan section, the shift-frequency searching unit is configured to determine, when both a result of a scan test for a scan pattern constituting the target scan section and a result of a scan test for a scan pattern inputted right before the scan pattern constituting the target scan section indicate the pass, the shift frequency used for the target scan section as the usable shift frequency for the target scan section.

4. The apparatus according to any one of claims 1 to 3, wherein when searching the usable shift frequency for the target scan section, the shift-frequency searching unit is configured to increase or decrease the shift frequency of the target scan section based on a binary search algorithm.

5. An apparatus for performing a scan test of IC chip including a test target circuit by inputting a scan pattern to a scan path via a scan input port of the IC chip, comparing an output pattern outputted via a scan output port with a predetermined expected pattern, and determining whether or not the IC chip is defective based on a result of comparing the output pattern with the predetermined expected pattern, the apparatus comprising:

a shift-frequency searching unit configured to perform a first scan test by

shifting a first scan pattern of which a whole or a part constituting a first scan section to the scan path and a second scan test by shifting a second scan pattern of which a whole or a part constituting a second scan section and to search a usable shift frequency for the second scan section, wherein,

the first scan pattern is inputted to the scan path right before the second scan pattern, and

the shift-frequency searching unit is configured

to shift the first scan section with a first shift frequency in the first scan test and shift the second scan section with a second shift frequency different from the first shift frequency to the scan path in the second scan test, and

when searching the usable shift frequency for the second scan section, to determine, when both a result of the first scan test and a result of the second scan test indicate the pass, the second shift frequency as the usable shift frequency for the second scan section.

6. The apparatus according to claim 5, wherein when searching the usable shift frequency for the second scan section, the shift-frequency searching unit is configured to increase or decrease the second shift frequency differently from that of at least one scan section among other scan sections shifted to the scan path before or after the second scan section or to set the second shift frequency differently from that of the at least one scan section among the other scan sections.

7. The apparatus according to claim 6, wherein when searching the usable shift frequency for the target scan section, the shift-frequency searching unit is configured to increase or decrease the second shift frequency based on a binary search algorithm.

8. The apparatus according to any one of claims 1 to 7, wherein the IC chip includes a chip on a wafer or a packaged chip.

9. The apparatus according to any one of claims 1 to 8, wherein the apparatus is further configured to allocate an optimum shift frequency from among usable shift frequencies searched by the shift-frequency searching unit for each of scan sections.

10. A method to be used in an apparatus for performing a scan test of IC chip including a test target circuit by inputting a scan pattern to a scan path via a scan input port of the IC chip, comparing an output pattern outputted via a scan output port with a predetermined expected pattern, and determining whether or not the IC chip is defective based on a result of comparing the output pattern with the predetermined expected pattern, the method comprising:

searching a usable shift frequency for a target scan section from among at least one scan section each including a whole or a part of at least one scan pattern inputted to the scan path, wherein

when searching the usable shift frequency for the target scan section, the searching includes searching a shift frequency with which a result of the scan test

indicates a pass or a shift frequency with which the result of the scan test indicates a fail, by increasing or decreasing a shift frequency of the target scan section differently from that of at least one scan section among other scan sections shifted to the scan path before or after the target scan section or by setting the shift frequency of the target scan section differently from that of the at least one scan section among the other scan sections.

11. The method according to claim 10, wherein when searching the usable shift frequency for the target scan section, the searching includes searching a shift frequency in a frequency range where the result of the scan test changes from the pass to the fail or a shift frequency in a frequency range where the result of the scan test changes from the fail to the pass, by increasing or decreasing the shift frequency of the target scan section.

12. The method according to claim 10 or 11, when searching the usable shift frequency for the target scan section, the searching includes determining, when both a result of a scan test for a scan pattern constituting the target scan section and a result of a scan test for a scan pattern inputted right before the scan pattern constituting the target scan section indicate the pass, the shift frequency used for the target scan section as the usable shift frequency for the target scan section.

13. The method according to any one of claims 10 to 12, wherein when searching the usable shift frequency for the target scan section, the searching includes increasing or decreasing the shift frequency of the target scan section

based on a binary search scheme.

14. A method to be used in an apparatus for performing a scan test of IC chip including a test target circuit by inputting a scan pattern to a scan path via a scan input port of the IC chip, comparing an output pattern outputted via a scan output port with a predetermined expected pattern, and determining whether or not the IC chip is defective based on a result of comparing the output pattern with the predetermined expected pattern, the method comprising:

performing a first scan test by shifting a first scan pattern of which a whole or a part constituting a first scan section to the scan path and a second scan test by shifting a second scan pattern of which a whole or a part constituting a second scan section; and

searching a usable shift frequency for the second scan section, wherein,

the first scan pattern is inputted to the scan path right before the second scan pattern, and

the searching includes

shifting the first scan section with a first shift frequency in the first scan test and shifting the second scan section with a second shift frequency different from the first shift frequency to the scan path in the second scan test, and

when searching the usable shift frequency for the second scan section, the searching includes determining, when both a result of the first scan test and a result of the second scan test indicate the pass, the second shift frequency as the usable shift frequency for the second scan section.

15. The method according to claim 14, wherein when searching the usable shift frequency for the second scan section, the searching includes increasing or decreasing the second shift frequency differently from that of at least one scan section among other scan sections shifted to the scan path before or after the second scan section or setting the second shift frequency differently from that of the at least one scan section among the other scan sections.

16. The method according to claim 15, wherein when searching the usable shift frequency for the target scan section, the searching includes increasing or decreasing the second shift frequency based on a binary search algorithm.

17. The method according to any one of claims 10 to 16, wherein the IC chip includes a chip on a wafer or a packaged chip.

18. The method according to any one of claims 10 to 14, further comprising allocating an optimum shift frequency from among usable shift frequencies searched at the searching to each of scan sections.

19. A system for testing an IC chip, the system comprising:

a computer including the apparatus according to any one of claims 1 to 9;

a tester main unit; and

a tester head, wherein

in a state in which the computer and the tester main unit are connected to each other via a wired or wireless communication, the computer is configured to control a scan test process performed by the tester main unit,

the test main unit is configured to generate an electrical signal for a test performed in the scan test process, and

the tester head is configured to transfer the electrical signal between the tester main unit and the IC chip.

20. A program for executing the method according to any one of claims 10 to 18 in the apparatus according to any one of claims 1 to 9.

21. A computer-readable recording medium that stores therein the program according to claim 20.