disposed on the respective surfaces of the impurity diffusion regions 23c and 23d. Similarly to the metal logic gate electrode LG2, each sidewall structure 27 has a top surface planarized through planarizing treatment such as CMP performed in a manufacturing process.

[0070] In the barrier region ER2, a remaining part 29 is disposed on the element separation layer IL1. The remaining part 29 remains through a process of manufacturing the memory gate structure 2, the first select gate structure 3, the second select gate structure 4, and the logic gate structures 21a and 21b. In this case, the remaining part 29 remains when the first select gate insulating film 15a and the second select gate insulating film 15b are formed. The remaining part 29 includes a remaining insulating film 31 made of an insulating material (in this case, a high-k material) the same as those of the first select gate insulating film 15a and the second select gate insulating film 15b and having an L-shaped section. The remaining insulating film 31 includes a bottom part 31a disposed on the element separation layer IL1, and a wall part 31b erected on the element separation layer IL1 at an end side surface of the bottom part 31a. A remaining metal layer MS2 is disposed on the bottom part 31a and along a surface of the wall part 31b. In the remaining part 29, a sidewall structure 34a made of, for example, SiN is disposed along the bottom part 31a of the remaining insulating film 31 and a sidewall of the remaining metal layer MS2 on the bottom part 31a.

[0071] In the remaining part 29, a wall-shaped remaining sidewall insulating film 30 is provided along the other surface of the wall part 31b of the remaining insulating film 31. The remaining sidewall insulating film 30 remains when the sidewall insulating films 13a and 13b of the memory cell 1 are formed. The remaining sidewall

the second insulating film 15 remains below the dummy first select gate electrode DDG, forming the first select gate insulating film 15a. In this manner, a dummy first select gate structure D3 including the sidewall-shaped dummy first select gate electrode DDG on the first select gate insulating film 15a is formed.

[0087] Simultaneously, in the memory circuit region ER1, the memory dummy electrode layer 38 remains in a sidewall shape along the sidewall spacer 8b on the second sidewall of the dummy memory gate structure D2, forming a dummy second select gate electrode DSG, and in addition, the second insulating film 15 remains below the dummy second select gate electrode DSG, forming the second select gate insulating film 15b. In this manner, a dummy second select gate structure D4 including the sidewall-shaped dummy second select gate electrode DSG on the second select gate insulating film 15b is formed.

[0088] Additionally, simultaneously, in the peripheral circuit region ER3, the logic dummy electrode layer 37 remains on the logic gate electrode formation target region through the hard mask layers HM1d and HM1e, forming dummy logic gate electrodes DGL1 and DGL2, and the first insulating film 11a remains below the dummy logic gate electrodes DLG1 and DLG2, forming the logic gate insulating films 25a and 25b, respectively. In this manner, dummy logic gate structures DL1 and DL2 in which the dummy logic gate electrodes DLG1 and DLG2 are stacked through the logic gate insulating films 25a and 25b, respectively, on the semiconductor substrate W in the peripheral circuit region ER3 are formed when the dummy first select gate structure D3 and the dummy second select gate structure D4 are formed in the memory circuit region ER1 (a dummy gate electrode forming process).

[0089] The dummy first select gate electrode DDG and the dummy second select gate electrode DSG, which are formed

through the dummy gate electrode forming process, can be formed to have a desired width by adjusting the thickness of the memory dummy electrode layer 38, which is formed through the second dummy electrode layer forming process described above.

[0090] When the hard mask layers HM1d and HM1e are formed, a hard mask layer HM1c remains in a region covered by the memory dummy electrode layer 38 and the second insulating film 15 in the barrier region ER2 (FIG. 5A). In addition to the hard mask layer HM1c, the first insulating film 11a, the second insulating film 15, the logic dummy electrode layer 37, and the memory dummy electrode layer 38 remain around the remaining sidewall insulating film 30 in the barrier region ER2, forming a dummy remaining part D29. In the barrier region ER2, the second insulating film 15 remains in an L-shaped section along one surface of the wall-shaped remaining sidewall insulating film 30 and the element separation layer IL1, forming the remaining insulating film 31, and the memory dummy electrode layer 38 remains in a sidewall shape along the bottom part 31a of the remaining insulating film 31 and the wall part 31b, forming a memory dummy electrode remaining part 39b. In the barrier region ER2, the logic dummy electrode layer 37 remains in a region disposed adjacent to the other surface of the remaining sidewall insulating film 30 and covered by the hard mask layer HM1c, forming a logic dummy electrode remaining part 39a, and the first insulating film 11a remains in a region covered by the logic dummy electrode remaining part 39a, forming the remaining insulating film 33 on the element separation layer IL1.

[0091] Subsequently, as illustrated in FIG. 6A, in which any corresponding part to that in FIG. 5B is denoted by an identical reference sign, low concentration of N-type impurities or P-type impurities are injected into the

memory circuit region ER1 and the peripheral circuit region ER3 by the ion implantation method or the like using a resist (not illustrated) patterned for the N type or the P type. Accordingly, the drain region 6a and the source region 6b are formed in the surface of the semiconductor substrate W in the memory circuit region ER1, and the impurity diffusion regions 23a, 23b, 23c, and 23d are formed in the surface of the semiconductor substrate W in the peripheral circuit region ER3. Subsequently, a layered insulating layer (not illustrated) made of, for example, SiN is formed across the memory circuit region ER1, the barrier region ER2, and the peripheral circuit region ER3, and then etched back. Accordingly, the insulating layer remains on sidewalls of the dummy first select gate structure D3 and the dummy second select gate structure D4, forming the sidewall structures 17a and 17b, and the insulating layer also remains on facing sidewalls of the dummy logic gate structures DL1 and DL2, forming the sidewall structures 26 and 27. The insulating layer also remains around the logic dummy electrode remaining part 39a and the memory dummy electrode remaining part 39b in the dummy remaining part D29 in the barrier region ER2, forming the sidewall structures 34a and 34b.

[0092] Thereafter, in addition to the above-described process, the following processes are sequentially performed: a process of forming high-concentration impurity regions in the drain region 6a and the source region 6b in the memory circuit region ER1 and the impurity diffusion regions 23a, 23b, 23c, and 23d in the peripheral circuit region ER3 by injecting high concentration of N-type impurities or P-type impurities into necessary places of the semiconductor substrate W by the ion implantation method or the like; a process of forming the silicide layer SC on the drain region 6a, the

the semiconductor substrate W through the logic gate insulating films 25a and 25b is formed in the peripheral circuit region ER3.

[0123] Simultaneously, in the memory circuit region ER1, the logic dummy electrode layer 49 remains in a sidewall shape along the sidewall spacer 8a on the first sidewall of the dummy memory gate structure D2, forming the dummy first select gate electrode DDG, and in addition, the insulating film 48 remains below the dummy first select gate electrode DDG, forming the first select gate insulating film 15a. In this manner, the dummy first select gate structure D3 including the sidewall-shaped dummy first select gate electrode DDG on the first select gate insulating film 15a is formed along the sidewall spacer 8a on the first sidewall of the dummy memory gate structure D2 in the memory circuit region ER1.

[0124] Simultaneously, in the memory circuit region ER1, the logic dummy electrode layer 49 remains in a sidewall shape along the sidewall spacer 8b on the second sidewall of the dummy memory gate structure D2, forming the dummy second select gate electrode DSG, and in addition, the insulating film 48 remains below the dummy second select gate electrode DSG, forming the second select gate insulating film 15b. In this manner, the dummy second select gate structure D4 including the sidewall-shaped dummy second select gate electrode DSG on the second select gate insulating film 15b is formed along the sidewall spacer 8b on the second sidewall of the dummy memory gate structure D2 in the memory circuit region ER1 (the dummy gate electrode forming process).

[0125] As described above, in the present embodiment, the logic dummy electrode layer 49 provided for forming the dummy logic gate electrodes DLG1 and DLG2 is used to form the dummy first select gate electrode DDG and the dummy

second select gate electrode DSG in the memory circuit region ER1.

[0126] To reduce the widths of the dummy first select gate electrode DDG and the dummy second select gate electrode DSG formed in the memory circuit region ER1, as illustrated in FIG. 8B, the peripheral circuit region ER3 and a partial region of the barrier region ER2 are covered by a resist M7, and the dummy first select gate electrode DDG and the dummy second select gate electrode DSG exposed in the memory circuit region ER1 are removed by dry etching. In this manner, the dummy first select gate electrode DDG and the dummy second select gate electrode DSG having desired widths are formed. Accordingly, in the manufacturing method, the dummy first select gate electrode DDG and the dummy second select gate electrode DSG in the memory circuit region ER1 can be formed to have desired widths independently whereas the dummy logic gate electrodes DLG1 and DLG2 having desired widths are formed in the peripheral circuit region ER3. Thus, the dummy first select gate electrode DDG and the dummy second select gate electrode DSG having small widths can be formed by the manufacturing method.

[0127] In the method for manufacturing the semiconductor integrated circuit device 46 according to the second embodiment, when the dummy first select gate electrode DDG, the dummy second select gate electrode DSG, and the dummy logic gate electrode DLG1, DLG2 are formed, the sidewall insulating film 30, the first insulating film 11a, the second insulating film 15, the logic dummy electrode layer 49, and the memory dummy electrode layer do not remain in the barrier region ER2, and thus the entire surface of the element separation layer IL1 can be exposed.

[0128] Thereafter, low concentration of N-type impurities or P-type impurities are injected into the memory circuit

region ER1 and the peripheral circuit region ER3 by the ion implantation method or the like using a resist (not illustrated) patterned for the N type or the P type. Accordingly, as illustrated in FIG. 7, the drain region 6a and the source region 6b are formed in the surface of the semiconductor substrate W in the memory circuit region ER1, and the impurity diffusion regions 23a, 23b, 23c, and 23d are formed in the surface of the semiconductor substrate W in the peripheral circuit region ER3. Subsequently, a layered insulating layer (not illustrated) made of, for example, SiN is formed across the memory circuit region ER1, the barrier region ER2, and the peripheral circuit region ER3 and then etched back. Accordingly, the insulating layer remains on the sidewalls of the dummy first select gate structure D3 and the dummy second select gate structure D4, forming the sidewall structures 17a and 17b, and the insulating layer also remains on the facing sidewalls of the dummy logic gate structures DL1 and DL2, forming the sidewall structures 26 and 27.

[0129] Thereafter, in addition, the following processes are sequentially performed: the process of forming high-concentration impurity regions on the drain region 6a and the source region 6b in the memory circuit region ER1 and the impurity diffusion regions 23a, 23b, 23c, and 23d in the peripheral circuit region ER3 by injecting high concentration of N-type impurities or P-type impurities into necessary places of the semiconductor substrate W by the ion implantation method or the like; the process of forming the silicide layer SC on the drain region 6a, the source region 6b, and the impurity diffusion regions 23a, 23b, 23c, and 23d; and the process of forming the interlayer insulating layer ILD to cover, for example, the dummy memory gate structure D2, the dummy first select gate structure D3, the dummy second select gate

structure D4, the dummy logic gate structures DL1 and DL2, and the dummy remaining part D29.

[0130] Subsequently, the surface of the interlayer insulating layer ILD is planarized by polished through planarizing treatment such as CMP to expose, on the surface of the interlayer insulating layer ILD, the planarized top surfaces of the dummy memory gate electrode DMG, the dummy first select gate electrode DDG, the dummy second select gate electrode DSG, and the dummy logic gate electrodes DLG1 and DLG2 (an electrode exposing process). Subsequently, the PMOS peripheral circuit region ER5 is covered by a resist, whereas the memory circuit region ER1, the barrier region ER2, and the NMOS peripheral circuit region ER4 are exposed. In this state, dry etching using, for example, carbon tetrafluoride (CF_4) is performed to remove the dummy memory gate electrode DMG, the dummy first select gate electrode DDG, the dummy second select gate electrode DSG, and the dummy logic gate electrode DLG1 exposed on the surface of the interlayer insulating layer ILD. Thereafter, the resist on the PMOS peripheral circuit region ER5 is removed.

[0131] Subsequently, a metal electrode layer made of an N-type MOS metallic material such as aluminum (Al), titanium aluminide (TiAl), tantalum carbide (TaC), or tantalum silicon nitride (TaSiN) is formed on the surface of the interlayer insulating layer ILD and embedded in the electrode formation spaces from which the dummy memory gate electrode DMG, the dummy first select gate electrode DDG, the dummy second select gate electrode DSG, and the dummy logic gate electrode DLG1 have been removed. Thereafter, a surface of the metal electrode layer is polished through planarizing treatment such as CMP and planarized in accordance with the surface of the interlayer insulating layer ILD. In the PMOS peripheral

barrier region ER2 and the peripheral circuit region ER3. Accordingly, as illustrated in FIG. 12C, in which any corresponding part to that in FIG. 12B is denoted by an identical reference sign, in the memory circuit region ER1, the memory dummy electrode layer 78 remains in a sidewall shape along the sidewall spacer 8a on a first sidewall of the dummy memory gate structure D22, forming the dummy first select gate electrode DDG on the semiconductor substrate W, and the memory dummy electrode layer 78 remains in a sidewall shape along the sidewall spacer 8b on a second sidewall of the dummy memory gate structure D22, forming the dummy second select gate electrode DSG on the semiconductor substrate W. Additionally, simultaneously, in the peripheral circuit region ER3, the logic dummy electrode layer 77 remains in the logic gate electrode formation target region through the hard mask layers HM1d and HM1e, forming the dummy logic gate electrodes DGL1 and DGL2 (the dummy gate electrode forming process).

[0161] The dummy first select gate electrode DDG and the dummy second select gate electrode DSG formed through the dummy gate electrode forming process can be formed to have a desired width by adjusting the thickness of the memory dummy electrode layer 78 formed through the second dummy electrode layer forming process described above.

[0162] When the hard mask layers HM1d and HM1e are formed in the barrier region ER2, the hard mask layer HM1c remains in a region covered by the memory dummy electrode layer 78 (FIG. 12B). In the barrier region ER2, in addition to the hard mask layer HM1c, the logic dummy electrode layer 77 and the memory dummy electrode layer 78 remain around the remaining sidewall insulating film 30, forming a dummy remaining part D61. In the barrier region ER2, the memory dummy electrode layer 78 remains in a sidewall shape along one surface of the wall-shaped

39b in the dummy remaining part D61 in the barrier region ER2, forming a sidewall structure 34.

[0164] Thereafter, in addition to the above-described process, the following processes are sequentially performed: the process of forming high-concentration impurity regions in the drain region 6a and the source region 6b in the memory circuit region ER1 and the impurity diffusion regions 23a, 23b, 23c, and 23d in the peripheral circuit region ER3 by injecting high concentration of N-type impurities or P-type impurities into necessary places of the semiconductor substrate W by the ion implantation method or the like; the process of forming the silicide layer SC on the drain region 6a, the source region 6b, and the impurity diffusion regions 23a, 23b, 23c, and 23d; and the process of forming the interlayer insulating layer ILD to cover, for example, the dummy memory gate structure D22, the dummy first select gate electrode DDG, the dummy second select gate electrode DSG, the dummy logic gate electrodes DLG1 and DLG2, and the dummy remaining part D61.

[0165] Subsequently, planarizing treatment such as CMP is performed to polish and planarize the surface of the interlayer insulating layer ILD, and further polish and planarize surfaces of the hard mask layers HM1a, HM1c, HM1d, and HM1e, the dummy memory gate structure D22, the dummy first select gate electrode DDG, the dummy second select gate electrode DSG, the dummy logic gate electrodes DLG1 and DLG2, and the dummy remaining part D61 that are exposed from the top surface of the interlayer insulating layer ILD. In this manner, as illustrated in FIG. 13B, in which any corresponding part to that in FIG. 13A is denoted by an identical reference sign, planarized top surfaces of the dummy memory gate electrode DMG, the dummy first select gate electrode DDG, the dummy second select gate electrode DSG, the dummy

[0192] Simultaneously, in the memory circuit region ER1, the logic dummy electrode layer 49 remains in a sidewall shape along the sidewall insulating film 13a on the first sidewall of the dummy memory gate structure D22, forming the dummy first select gate electrode DDG, and the logic dummy electrode layer 49 remains in a sidewall shape along the sidewall insulating film 13b on the second sidewall of the dummy memory gate structure D22, forming the dummy second select gate electrode DSG (the dummy gate electrode forming process). As described above, in the present embodiment, the logic dummy electrode layer 49 provided for forming the dummy logic gate electrodes DLG1 and DLG2 is used to form the dummy first select gate electrode DDG and the dummy second select gate electrode DSG in the memory circuit region ER1.

[0193] To reduce the widths of the dummy first select gate electrode DDG and the dummy second select gate electrode DSG formed in the memory circuit region ER1, as illustrated in FIG. 15B, the peripheral circuit region ER3 and a partial region of the barrier region ER2 are covered by the resist M7, and the dummy first select gate electrode DDG and the dummy second select gate electrode DSG exposed in the memory circuit region ER1 are removed by dry etching. In this manner, the dummy first select gate electrode DDG and the dummy second select gate electrode DSG having desired widths are formed. Accordingly, in the manufacturing method, the dummy first select gate electrode DDG and the dummy second select gate electrode DSG in the memory circuit region ER1 can be formed to have desired widths independently whereas the dummy logic gate electrodes DLG1 and DLG2 having desired widths are formed in the peripheral circuit region ER3. Thus, the dummy first select gate electrode DDG and the dummy second select gate electrode DSG having small widths can be formed by the manufacturing method.

[0194] In the method for manufacturing the semiconductor integrated circuit device 80 according to the fourth embodiment, when the dummy first select gate electrode DDG, the dummy second select gate electrode DSG, and the dummy logic gate electrode DLG1, DLG2 are formed, the sidewall insulating film 30, the memory dummy electrode layer, and the logic dummy electrode layer 49 do not remain in the barrier region ER2, and thus the entire surface of the element separation layer IL1 can be exposed.
[0195] Thereafter, low concentration of N-type impurities or P-type impurities are injected into the memory circuit region ER1 and the peripheral circuit region ER3 by the ion implantation method or the like using a resist (not illustrated) patterned for the N type or the P type. Accordingly, as illustrated in FIG. 14, the drain region 6a and the source region 6b are formed in the surface of the semiconductor substrate W in the memory circuit region ER1, and the impurity diffusion regions 23a, 23b, 23c, and 23d are formed in the surface of the semiconductor substrate W in the peripheral circuit region ER3. Subsequently, a layered insulating layer (not illustrated) made of, for example, SiN is formed across the memory circuit region ER1, the barrier region ER2, and the peripheral circuit region ER3 and then etched back. Accordingly, the insulating layer remains on the sidewalls of the dummy first select gate electrode DDG and the dummy second select gate electrode DSG, forming the sidewall structures 17a and 17b, and the insulating layer also remains on the facing sidewalls of the dummy logic gate electrodes DLG1 and DLG2, forming the sidewall structures 26 and 27.
[0196] Thereafter, in addition, the following processes are sequentially performed: the process of forming high-concentration impurity regions in the drain region 6a and the source region 6b in the memory circuit region ER1 and

the impurity diffusion regions 23a, 23b, 23c, and 23d in the peripheral circuit region ER3 by injecting high concentration of N-type impurities or P-type impurities into necessary places of the semiconductor substrate W by the ion implantation method or the like; the process of forming the silicide layer SC on the drain region 6a, the source region 6b, and the impurity diffusion regions 23a, 23b, 23c, and 23d; and the process of forming the interlayer insulating layer ILD to cover the dummy memory gate structure D22, the dummy first select gate electrode DDG, the dummy second select gate electrode DSG and the dummy logic gate electrodes DLG1 and DLG2.

[0197] Subsequently, the surface of the interlayer insulating layer ILD is planarized by polished through planarizing treatment such as CMP to expose, on the surface of the interlayer insulating layer ILD, the planarized top surfaces of the dummy memory gate electrode DMG, the dummy first select gate electrode DDG, the dummy second select gate electrode DSG, and the dummy logic gate electrodes DLG1 and DLG2 (the electrode exposing process). Subsequently, the PMOS peripheral circuit region ER5 is covered by a resist, whereas the memory circuit region ER1, the barrier region ER2, and the NMOS peripheral circuit region ER4 are exposed. In this state, dry etching using, for example, carbon tetrafluoride (CF_4) is performed to remove the dummy memory gate electrode DMG, the dummy first select gate electrode DDG, the dummy second select gate electrode DSG, and the dummy logic gate electrode DLG1 exposed on the surface of the interlayer insulating layer ILD. Thereafter, the resist on the PMOS peripheral circuit region ER5 is removed.

[0198] Subsequently, a layered insulating film made of an insulating material (for example, a high-k material) different from that of the lower memory gate insulating

Claims

1. A memory cell disposed on a semiconductor substrate on which a peripheral circuit including a metal logic gate electrode containing a metallic material is provided, the memory cell comprising:

a drain region disposed on a surface of the semiconductor substrate and connected with a bit line;

a source region disposed on the surface of the semiconductor substrate and connected with a source line;

a memory gate structure that is disposed between the drain region and the source region and in which a lower memory gate insulating film, a charge storage layer, an upper memory gate insulating film, and a metal memory gate electrode containing the metallic material are stacked in this order on the semiconductor substrate;

a first select gate structure in which a metal first select gate electrode containing the metallic material is disposed on the semiconductor substrate between the drain region and the memory gate structure through a first select gate insulating film and that is disposed adjacent to a first sidewall of the memory gate structure through a first sidewall spacer; and

a second select gate structure in which a metal second select gate electrode containing the metallic material is disposed on the semiconductor substrate between the source region and the memory gate structure through a second select gate insulating film and that is disposed adjacent to a second sidewall of the memory gate structure through a second sidewall spacer, wherein

a first memory gate sidewall insulating film disposed along the first sidewall spacer and integrated with the upper memory gate insulating film is provided between the metal memory gate electrode and the first sidewall spacer, and

a second memory gate sidewall insulating film disposed along the second sidewall spacer and integrated with the upper memory gate insulating film is provided between the metal memory gate electrode and the second sidewall spacer.

2. A memory cell disposed on a semiconductor substrate on which a peripheral circuit including a metal logic gate electrode containing a metallic material is provided, the memory cell comprising:

a drain region disposed on a surface of the semiconductor substrate and connected with a bit line;

a source region disposed on the surface of the semiconductor substrate and connected with a source line;

a memory gate structure that is disposed between the drain region and the source region and in which a lower memory gate insulating film, a charge storage layer, an upper memory gate insulating film, and a metal memory gate electrode containing the metallic material are stacked in this order on the semiconductor substrate;

a first select gate structure in which a metal first select gate electrode containing the metallic material is disposed on the semiconductor substrate between the drain region and the memory gate structure through a first select gate insulating film and that is disposed adjacent to a first sidewall of the memory gate structure through a first sidewall spacer; and

a second select gate structure in which a metal second select gate electrode containing the metallic material is disposed on the semiconductor substrate between the source region and the memory gate structure through a second select gate insulating film and that is disposed adjacent to a second sidewall of the memory gate structure through a second sidewall spacer, wherein

the first sidewall spacer is composed of a first sidewall insulating film disposed along the first sidewall of the memory gate structure and a first select gate sidewall insulating film disposed along a sidewall of the first select gate structure and integrated with the first select gate insulating film,

the second sidewall spacer is composed of a second sidewall insulating film disposed along the second sidewall of the memory gate structure and a second select gate sidewall insulating film disposed along a sidewall of the second select gate structure and integrated with the second select gate insulating film,

the first select gate sidewall insulating film and the second select gate sidewall insulating film are made of an insulating material different from an insulating material of the first sidewall insulating film and the second sidewall insulating film,

the first sidewall insulating film and the second sidewall insulating film are made of the insulating material having a relative dielectric constant smaller than a relative dielectric constant of the insulating material of the first select gate sidewall insulating film and the second select gate sidewall insulating film, and

the first select gate sidewall insulating film and the second select gate sidewall insulating film are each made of a high-k material.

3. The memory cell according to claim 1, wherein the metal memory gate electrode, the metal first select gate electrode, and the metal second select gate electrode have planarized top surfaces, and a planarized top surface of the metal memory gate electrode, a planarized top surface of the metal first select gate electrode, and

a planarized top surface of the metal second select gate electrode have identical heights.

4. A semiconductor integrated circuit device including memory cells arranged in a matrix of rows and columns and each connected with a bit line and a source line, wherein

each memory cell is the memory cell according to claim 1, and

a peripheral circuit region in which the peripheral circuit is provided is provided around a memory circuit region in which each memory cell is disposed.

5. The semiconductor integrated circuit device according to claim 4, wherein

the peripheral circuit has a configuration in which the metal logic gate electrode containing the metallic material is disposed on the surface of the semiconductor substrate through a logic gate insulating film, and

the metal memory gate electrode, the metal first select gate electrode, the metal second select gate electrode, and the metal logic gate electrode are made of the same metallic material.

6. A method for manufacturing a semiconductor integrated circuit device including:

a memory circuit region in which a memory cell including a memory gate structure between a first select gate structure and a second select gate structure is disposed; and

a peripheral circuit region in which a peripheral circuit including a logic gate structure is disposed,

the method comprising:

a first dummy electrode layer forming process of forming a layered lower memory gate insulating film and a layered charge storage layer in this order on a

semiconductor substrate in the memory circuit region, and then forming a layered logic dummy electrode layer on the charge storage layer in the memory circuit region and the semiconductor substrate in the peripheral circuit region;

a dummy memory gate structure forming process of patterning the logic dummy electrode layer, the charge storage layer, and the lower memory gate insulating film in the memory circuit region by using a patterned resist so that a dummy memory gate structure in which the lower memory gate insulating film, the charge storage layer, and a dummy memory gate electrode provided by patterning are stacked in this order is formed in the memory circuit region whereas the logic dummy electrode layer remains intact in the peripheral circuit region using the resist;

a sidewall insulating film forming process of forming a layered sidewall insulating film across the memory circuit region and the peripheral circuit region, and then etching back the layered sidewall insulating film to expose the semiconductor substrate, thereby forming sidewall insulating films along facing sidewalls of the dummy memory gate structure in the memory circuit region;

a second dummy electrode layer forming process of forming a layered memory dummy electrode layer across the memory circuit region and the peripheral circuit region, and then removing the memory dummy electrode layer in the peripheral circuit region by using a patterned resist whereas the memory dummy electrode layer remains in the memory circuit region;

a dummy gate electrode forming process of patterning the logic dummy electrode layer in the peripheral circuit region by using another patterned resist to form a dummy logic gate electrode on the semiconductor substrate, and etching back the memory dummy electrode layer in the memory circuit region so that a sidewall-shaped dummy

first select gate electrode is formed along one of the sidewall insulating films of the dummy memory gate structure and a sidewall-shaped dummy second select gate electrode is formed along the other sidewall insulating film of the dummy memory gate structure;

an electrode exposing process of forming an interlayer insulating layer in the memory circuit region and the peripheral circuit region, and then processing the interlayer insulating layer to expose, on the interlayer insulating layer, top surfaces of the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode; and

a metal gate electrode forming process of removing the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode, forming a layered insulating film in spaces in which the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode have been formed, and then forming a metal memory gate electrode, a metal first select gate electrode, a metal second select gate electrode, and a metal logic gate electrode each containing a metallic material, in electrode formation spaces enclosed by the insulating film in the spaces.

7. A method for manufacturing a semiconductor integrated circuit device including:

a memory circuit region in which a memory cell including a memory gate structure between a first select gate structure and a second select gate structure is disposed; and

a peripheral circuit region in which a peripheral circuit including a logic gate structure is disposed,

the method comprising:

a sidewall insulating film forming process of providing, in the memory circuit region, a dummy memory gate structure in which a lower memory gate insulating film, a charge storage layer, and a dummy memory gate electrode provided by patterning are stacked in this order on a semiconductor substrate, and then forming a layered sidewall insulating film across the memory circuit region and the peripheral circuit region, and then etching back the layered sidewall insulating film to expose the semiconductor substrate, thereby forming sidewall insulating films along facing sidewalls of the dummy memory gate structure;

a dummy electrode layer forming process of forming a layered logic dummy electrode layer in the memory circuit region and the peripheral circuit region;

a dummy gate electrode forming process of patterning the logic dummy electrode layer in the peripheral circuit region by using a patterned resist to form a dummy logic gate electrode on the semiconductor substrate, and etching back the logic dummy electrode layer in the memory circuit region so that a sidewall-shaped dummy first select gate electrode is formed along one of the sidewall insulating films of the dummy memory gate structure and a sidewall-shaped dummy second select gate electrode is formed along the other sidewall insulating film of the dummy memory gate structure;

an electrode exposing process of forming an interlayer insulating layer in the memory circuit region and the peripheral circuit region, and then processing the interlayer insulating layer to expose, on the interlayer insulating layer, top surfaces of the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode; and

a metal gate electrode forming process of removing the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode, forming a layered insulating film in spaces in which the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode have been formed, and then forming a metal memory gate electrode, a metal first select gate electrode, a metal second select gate electrode, and a metal logic gate electrode each containing a metallic material, in electrode formation spaces enclosed by the insulating film in the spaces.

8. A method for manufacturing a semiconductor integrated circuit device including:

a memory circuit region in which a memory cell including a memory gate structure between a first select gate structure and a second select gate structure is disposed; and

a peripheral circuit region in which a peripheral circuit including a logic gate structure is disposed,

the method comprising:

a first dummy electrode layer forming process of forming a layered lower memory gate insulating film and a layered charge storage layer in this order on a semiconductor substrate in the memory circuit region, and then stacking a layered first insulating film and a layered logic dummy electrode layer in this order on the charge storage layer in the memory circuit region and the semiconductor substrate in the peripheral circuit region;

a dummy memory gate structure forming process of patterning the logic dummy electrode layer, the first insulating film, the charge storage layer, and the lower memory gate insulating film in the memory circuit region

by using a patterned resist so that a dummy memory gate structure in which the lower memory gate insulating film, the charge storage layer, an upper memory gate insulating film, and a dummy memory gate electrode provided by patterning are stacked in this order is formed in the memory circuit region and the first insulating film and the logic dummy electrode layer remain intact in the peripheral circuit region using the resist;

a sidewall insulating film forming process of forming a layered sidewall insulating film across the memory circuit region and the peripheral circuit region, and then etching back the layered sidewall insulating film to expose the semiconductor substrate, thereby forming sidewall insulating films along facing sidewalls of the dummy memory gate structure in the memory circuit region;

a second dummy electrode layer forming process of forming a layered second insulating film across the memory circuit region and the peripheral circuit region to form sidewall spacers composed of the sidewall insulating films and the second insulating film on the respective facing sidewalls of the dummy memory gate structure, stacking a layered memory dummy electrode layer on the second insulating film, and removing the memory dummy electrode layer and the second insulating film in this order in the peripheral circuit region by using a patterned resist so that the second insulating film and the memory dummy electrode layer remain in the memory circuit region;

a dummy gate electrode forming process of patterning the logic dummy electrode layer and the first insulating film in the peripheral circuit region by using another patterned resist to form a dummy logic gate structure in which a dummy logic gate electrode is stacked on the semiconductor substrate through a logic gate insulating

film, and etching back the memory dummy electrode layer and the second insulating film in the memory circuit region so that a sidewall-shaped dummy first select gate electrode is formed along one of the sidewall spacers of the dummy memory gate structure whereas the second insulating film remains below the dummy first select gate electrode to form a first select gate insulating film, and a sidewall-shaped dummy second select gate electrode is formed along the other sidewall spacer of the dummy memory gate structure whereas the second insulating film remains below the dummy second select gate electrode to form a second select gate insulating film;

an electrode exposing process of forming an interlayer insulating layer in the memory circuit region and the peripheral circuit region, and then processing the interlayer insulating layer to expose, on the interlayer insulating layer, top surfaces of the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode; and

a metal gate electrode forming process of removing the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode, and then forming, in electrode formation spaces in which the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode have been formed, a metal memory gate electrode, a metal first select gate electrode, a metal second select gate electrode, and a metal logic gate electrode each containing a metallic material.

9. A method for manufacturing a semiconductor integrated circuit device including:

a memory circuit region in which a memory cell including a memory gate structure between a first select gate structure and a second select gate structure is disposed; and

a peripheral circuit region in which a peripheral circuit including a logic gate structure is disposed,

the method comprising:

a sidewall insulating film forming process of providing, in the memory circuit region, a dummy memory gate structure in which a lower memory gate insulating film, a charge storage layer, an upper memory gate insulating film, and a dummy memory gate electrode provided by patterning are stacked in this order on a semiconductor substrate, and then forming a layered sidewall insulating film across the memory circuit region and the peripheral circuit region, and then etching back the layered sidewall insulating film to expose the semiconductor substrate, thereby forming sidewall insulating films along facing sidewalls of the dummy memory gate structure;

a dummy electrode layer forming process of forming a layered insulating film in the memory circuit region and the peripheral circuit region to form sidewall spacers composed of the sidewall insulating films and the insulating film on the respective facing sidewalls of the dummy memory gate structure, and then stacking a layered logic dummy electrode layer on the insulating film;

a dummy gate electrode forming process of patterning the logic dummy electrode layer and the insulating film in the peripheral circuit region by using a patterned resist to form a dummy logic gate structure in which a dummy logic gate electrode is stacked on the semiconductor substrate through a logic gate insulating film, and etching back the logic dummy electrode layer and the insulating film in the memory circuit region so

that a sidewall-shaped dummy first select gate electrode is formed along one of the sidewall spacers of the dummy memory gate structure whereas the insulating film remains below the dummy first select gate electrode to form a first select gate insulating film and a sidewall-shaped dummy second select gate electrode is formed along the other sidewall spacer of the dummy memory gate structure whereas the insulating film remains below the dummy second select gate electrode to form a second select gate insulating film;

an electrode exposing process of forming an interlayer insulating layer in the memory circuit region and the peripheral circuit region, and then processing the interlayer insulating layer to expose, on the interlayer insulating layer, top surfaces of the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode; and

a metal gate electrode forming process of removing the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode, and then forming, in electrode formation spaces in which the dummy memory gate electrode, the dummy first select gate electrode, the dummy second select gate electrode, and the dummy logic gate electrode have been formed, a metal memory gate electrode, a metal first select gate electrode, a metal second select gate electrode, and a metal logic gate electrode each containing a metallic material.

10. The method for manufacturing a semiconductor integrated circuit device according to claim 6, wherein the dummy first select gate electrode and the dummy second select gate electrode formed through the dummy gate electrode forming process are formed to have desired

widths by adjusting a thickness of the memory dummy electrode layer formed through the second dummy electrode layer forming process.

11. The method for manufacturing a semiconductor integrated circuit device according to claim 7, further comprising, after the dummy gate electrode forming process, a dummy electrode adjusting process of covering the peripheral circuit region with a resist and removing predetermined amounts of the dummy first select gate electrode and the dummy second select gate electrode in the memory circuit region to adjust widths of the dummy first select gate electrode and the dummy second select gate electrode.