1. A method of forming an array of memory cells, comprising:

forming shallow trenches into conductively doped silicon-comprising semiconductor material of a first conductivity type, second conductivity type semiconductor material being elevationally inward of the conductively doped first type semiconductor material;

reacting metal with silicon of bases of the shallow trenches to form conductive metal silicide over the bases;

forming deep trenches through the conductive metal silicide, through the conductively doped first type semiconductor material, and into the second conductivity type semiconductor material to form buried access lines running along and between the deep trenches; the forming of the deep trenches forming pillars comprising conductively doped first type semiconductor material extending elevationally outward of and spaced along the buried access lines;

forming outer access lines elevationally outward of the pillars;

providing a plurality of conductive vias spaced along and electrically coupling pairs of individual of the buried and outer access lines, a plurality of the pillars being spaced between immediately adjacent of the vias along the pairs; and

providing a memory cell within individual of the pillars.

2. The method of claim **1** comprising:

lining sidewalls and the bases of the shallow trenches with dielectric;

removing the dielectric from the bases; and

after removing the dielectric, conducting said reacting.

3. The method of claim **2** wherein the reacting forms conductive metal silicide elevationally under the dielectric sidewall lining.

4. The method of claim **3** wherein the reacting forms conductive metal silicide laterally into and elevationally under the pillars.

5. The method of claim **1** wherein the reacting extends conductive metal silicide elevationally under the pillars.

6. The method of claim **5** wherein the reacting interconnects the conductive metal silicide elevationally under the pillars.

7. The method of claim 5 wherein the reacting does not interconnect the conductive metal silicide elevationally under the pillars.

8. A method of forming an array of memory cells, comprising:

forming intersecting shallow trenches and deep trenches into semiconductor material about individual pillar regions of the semiconductor material, those portions of the semiconductor material beneath and between the pillar regions and between the deep trenches comprising individual buried access line regions;

forming a dielectric liner against sidewalls of the pillars;

forming conductive metal material against bottoms of the shallow trenches to extend between the pillar regions atop the buried access line regions and forming the conductive metal material directly under the dielectric liner, the conductive metal material being formed to extend to elevationally directly under individual of the pillar regions;

forming outer access lines elevationally outward of the pillar regions;

providing a plurality of conductive vias spaced along and electrically coupling pairs of individual of the buried access line regions and the outer access lines, a plurality of the pillar regions being spaced between immediately adjacent of the vias along the pairs;

providing a memory cell within individual of the pillar regions; and

providing the semiconductor material of the buried access line regions to be conductively doped, the outer access lines being more electrically conductive than the conductively doped buried access line regions in a finished circuitry construction.

9. A method of forming an array of memory cells, comprising:

forming intersecting shallow trenches and deep trenches into semiconductor material about individual pillar regions of the semiconductor material, those portions of the semiconductor material beneath and between the pillar regions and between the deep trenches comprising individual buried access line regions;

forming conductive metal material against bottoms of the shallow trenches to extend between the pillar regions atop the buried access line regions and forming the conductive metal material to have a concave arcuate elevationally outer surface, the conductive metal material being formed to extend to elevationally directly under individual of the pillar regions;

forming outer access lines elevationally outward of the pillar regions;

providing a plurality of conductive vias spaced along and electrically coupling pairs of individual of the buried access line regions and the outer access lines, a plurality of the pillar regions being spaced between immediately adjacent of the vias along the pairs;

providing a memory cell within individual of the pillar regions; and

providing the semiconductor material of the buried access line regions to be conductively doped, the outer access lines being more electrically conductive than the conductively doped buried access line regions in a finished circuitry construction.

10. The method of claim **9** comprising forming a dielectric liner against sidewalls of the pillars, and forming the conductive metal material directly under the dielectric liner, the concave arcuate elevationally outer surface not being directly beneath the dielectric liner.

11. A method of forming an array of memory cells, comprising:

forming intersecting shallow trenches and deep trenches into semiconductor material about individual pillar regions of the semiconductor material, those portions of the semiconductor material beneath and between the pillar regions and between the deep trenches comprising individual buried access line regions;

forming conductive metal material against bottoms of the shallow trenches to extend between the pillar regions atop the buried access line regions and forming the conductive metal material to have a convex arcuate elevationally inner surface, the conductive metal material being formed to extend to elevationally directly under individual of the pillar regions;

forming outer access lines elevationally outward of the pillar regions;

providing a plurality of conductive vias spaced along and electrically coupling pairs of individual of the buried access line regions and the outer access lines, a plurality of the pillar regions being spaced between immediately adjacent of the vias along the pairs;

providing a memory cell within individual of the pillar regions; and

providing the semiconductor material of the buried access line regions to be conductively doped, the outer access lines being more electrically conductive than the conductively doped buried access line regions in a finished circuitry construction.

12. The method of claim **8** comprising forming the conductive metal material to be physically contacting a bottom surface of the dielectric liner.