

WHAT IS CLAIMED IS:

1. A three-dimensional semiconductor memory device, comprising:
a substrate including a peripheral circuit region and a cell array region;
peripheral gate stacks provided on the peripheral circuit region of the substrate;
and
an electrode structure provided on the cell array region of the substrate, the electrode structure including a lower electrode, a lower insulating layer covering the lower electrode, and upper electrodes and upper insulating layers, which are vertically and alternately stacked on the lower insulating layer,
wherein the lower insulating layer is extended from a region between the lower electrode and a lowermost one of the upper electrodes on the cell array region to the peripheral circuit region to cover the peripheral gate stacks, and
a top surface of the lower insulating layer is higher on the peripheral circuit region than on the cell array region.
2. The device as claimed in claim 1, wherein an uppermost level of the top surface of the lower insulating layer on the peripheral circuit region is positioned above a top surface of a lowermost one of the upper electrodes.
3. The device as claimed in claim 1, wherein a lowermost level of the top surface of the lower insulating layer on the peripheral circuit region is positioned between the peripheral gate stacks.

4. The device as claimed in claim 1, wherein a difference in distance between lowermost and uppermost levels of the top surface of the lower insulating layer on the peripheral circuit region is larger than a thickness of each of the upper electrodes.

5. The device as claimed in claim 1, wherein the peripheral gate stacks have a first thickness,

the lower electrode has a second thickness smaller than the first thickness, and

the lower insulating layer on the cell array region has a third thickness larger than the first thickness.

6. The device as claimed in claim 1, wherein the lower insulating layer has a lower insulating layer thickness that is substantially uniform on the cell array region, and

each of the upper insulating layers has a thickness smaller than the lower insulating layer thickness.

7. The device as claimed in claim 1, wherein each of the upper electrodes has substantially a same thickness as that of the lower electrode.

8. The device as claimed in claim 1, wherein top surfaces of the peripheral gate stacks are positioned between a top surface of the lower electrode and a bottom surface of the lowermost one of the upper electrodes.

9. The device as claimed in claim 1, wherein the top surface of the lower insulating layer is even on the cell array region and is uneven on the peripheral circuit region.

10. The device as claimed in claim 1, wherein the lower insulating layer includes upwardly convex portions provided on the peripheral circuit region.

11. The device as claimed in claim 1, further comprising an upper insulating gapfill layer that covers the electrode structure and the lower insulating layer of the peripheral circuit region,

wherein the upper insulating gapfill layer is in direct contact with the top surface of the lower insulating layer, on the peripheral circuit region.

12. The device as claimed in claim 11, wherein the lower insulating layer includes a first insulating material, and

the upper insulating gapfill layer includes a second insulating material that is different from the first insulating material.

13. The device as claimed in claim 12, wherein the first and second insulating materials have etch rates that are different from each other.

14. The device as claimed in claim 11, further comprising a dummy sacrificial pattern that is on the peripheral circuit region and conformally covers the peripheral gate stacks,

wherein the dummy sacrificial pattern includes an insulating material that is different from the lower insulating layer and the upper insulating gapfill layer.

15. The device as claimed in claim 14, wherein the lower insulating layer includes a portion that is disposed between a bottom surface of the upper insulating gapfill layer and a top surface of the dummy sacrificial pattern.

16. The device as claimed in claim 1, further comprising a plurality of vertical structures that are on the cell array region, the plurality of vertical structures penetrating the electrode structure and being connected to the substrate.

17. A three-dimensional semiconductor memory device, comprising:
a substrate including a peripheral circuit region and a cell array region;
peripheral gate stacks provided on the peripheral circuit region of the substrate;
a lower electrode provided on the cell array region of the substrate;
a lower insulating layer covering the lower electrode and the peripheral gate stacks; and

an electrode structure on the cell array region, the electrode structure including upper electrodes and upper insulating layers which are vertically and alternately stacked on the lower insulating layer,

wherein the lower insulating layer includes a flat portion, which is between the lower electrode and a lowermost one of the upper electrodes on the cell array region and has a uniform first thickness, and upwardly convex portions, which are on the peripheral circuit region and cover the peripheral gate stacks.

18. The device as claimed in claim 17, wherein a top surface of the flat portion is positioned at a first level, when measured from the substrate, and

top surfaces of the convex portions are positioned at a second level higher than the first level, when measured from the substrate.

19. The device as claimed in claim 17, further comprising an upper insulating gapfill layer that is on the lower insulating layer and covers the electrode structure,

wherein the upper insulating gapfill layer is in direct contact with the convex portions of the lower insulating layer.

20. The device as claimed in claim 19, further comprising a dummy sacrificial pattern that is on the peripheral circuit region of the substrate, the dummy sacrificial pattern having a uniform thickness and covering the peripheral gate stacks, wherein the dummy sacrificial pattern is spaced apart from the upper insulating gapfill layer.