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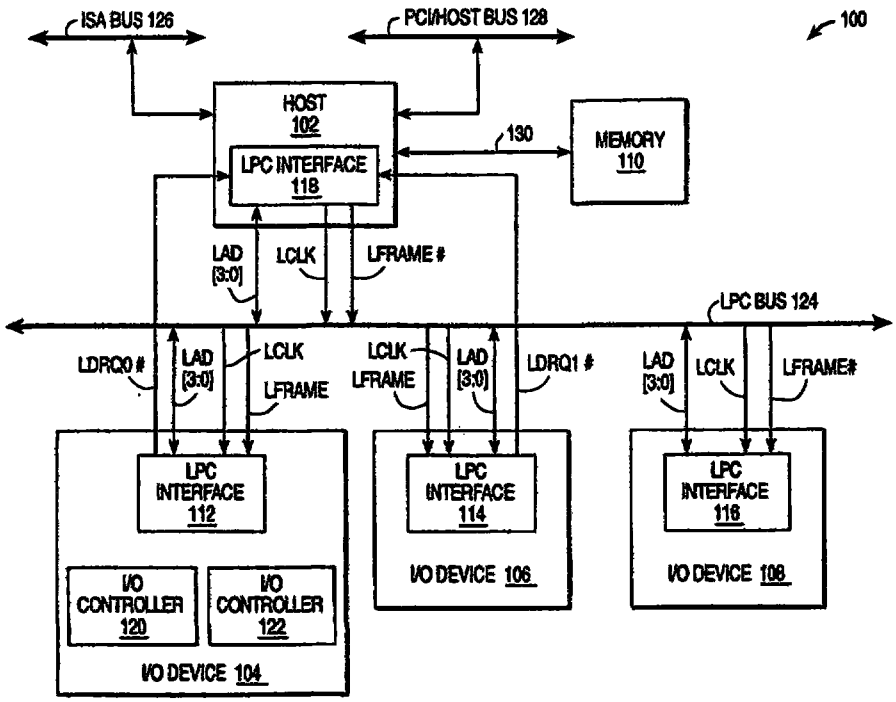
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(54) Title: MEMORY TRANSACTIONS ON A LOW PIN COUNT BUS



(57) Abstract

A system having a bus (124) coupled to a host (102) and a memory device (108). The bus (124) may include a plurality of general purpose signal lines to carry time-multiplexed address, data, and control information. The memory device (108) may store system start-up information and communicate this information with the host (102) over the bus (124).