ABSTRACT

SHALLOW TRENCH ISOLATION OF MOSFETS WITH REDUCED CORNER PARASITIC CURRENTS

A method is described for forming MOSFETs with shallow trench isolation wherein the abrupt corners introduced by anisotropically etching the silicon trenches are modified by an oxidation step which rounds off the corners and also reduces the effect of tensile stresses caused by the densified trench filler material. The method selectively exposes the corner regions to an oxidation whereby the formation of an oxide birdsbeak modulates the corners and introduces a compressive stress component in the corner region. Several variations of the procedure are disclosed, including embodiments wherein birdsbeaks extending in both a vertical and horizontal directions from the corners are employed. The channel and gate oxide edges of MOSFETs extend to these corners. By attenuating the abrupt corners and reducing the mechanical stresses, gate oxide integrity is improved and anomalous sub-threshold currents of MOSFETs formed are abated.

(FIGURE 3 IS SUGGESTED FOR PUBLICATION)