

System and Method for Phase Shift Calibration

FIELD OF INVENTION

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The present invention relates broadly to a system and method for phase shift calibration as well as to a computer readable data storage medium having stored thereon computer code means for instructing a computer to execute a method for phase shift calibration.

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BACKGROUND

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Serial data transfer is popular in connections between electronic cards or systems. Serialized data makes greater use of the resources such as connector pins and cable wires available to the system. In serial data transfers, one or more data signals, which can either be single-ended or differential, and a clock signal, are transmitted to a receiver.

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In the receiver, a sampling clock is generated from the received clock signal by clock multiplication (if necessary) to match the data rate. Also, phase-shifting of the sampling clock is performed to align the sampling clock edge to the center of the valid data window. In general, there are two forms of clock edges the rising edge and the falling edge.

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Depending on the defined data rate, the data signals are then sampled and deserialized using the sampling clock. If the sampling is single data rate (SDR), only the rising sampling clock edges are used to sample the data and hence the sampling clock rate is the same as data rate. If the sampling is double data rate (DDR), both rising and falling sampling clock edges are used to sample data and hence the data rate is double the sampling clock rate.

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In an ideal data transfer, the received clock and data signals are phase-aligned in the receiver. The sampling clock is typically a phase shifted version of the received

clock, with a phase shift of $\frac{1}{2}$ sampling clock period in SDR, or $\frac{1}{4}$ sampling clock period in DDR, such that the sampling edges of the sampling clock are in the center of the data valid window.

5 The received clock and data signals may have different delays along the connecting cable between the transmitter and the receiver. This introduces timing skews between the received clock and data signal, such that the received clock and data signals are not phase-aligned. The timing skew between clock and data can cause data sampling clock edge to be off the center of the valid data window and therefore reduce
10 the noise margin. In worst-case scenarios, the skew can result in the data sampling clock edge to be outside the valid data window and result in the incorrect data being sampled.

 The timing skew can increase with cable length and may vary with cable quality.
15 Timing skew between clock and data may also be due to different PCB (Printed Circuit Board) track lengths and circuitry in the transmitter and receiver. In addition, the clock recovery and multiplication circuits in the receiver may further introduce some delay.

 To overcome the timing skew between the received clock and data signals,
20 different phase shift and skew correction techniques may be found in the state of the art. For example, in a typical LVDS (Low Voltage Differential Signal) channel link receiver, a predetermined phase shift is imposed on the received clock to align the clocking edge with the valid data window.

25 In "Skew Cancellation for Source Synchronous Clock and Data Signals" (US Patent 7,301,996 B1), Chi *et al* discloses a system where the timing skew is manually measured through e.g. an oscilloscope, and the measured timing skew is programmed into a data storage device. Sampling clock signals of varying phase differences from the received clock signal are generated for selection. Based on the measured timing skew
30 value stored in the data storage device, one sampling clock signal is then selected for use.

 Other techniques of measuring the timing skew between signals include the use of a timer as disclosed in "Using Multiple High Speed Serial Lines to Transmit High Data

Rates While Compensating for Overall Skew", (US Patent 6,167,077), Ducaroir *et al.* The timer times the receiving of the data sets and measures the data skew across the plurality of serial lines. The measured skew data is then forwarded to a control circuit for skew correction.

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Also disclosed in "Skew Cancellation for Source Synchronous Clock and Data Signals" by Chi *et al.*, is the use of a clock recovery PLL (Phase Locked Loop) to adjust the phase of the sampling clock to be in-phase with the serial input data signal during an initial training period.

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Open-loop skew detection may also be used to determine the amount of skew by using a preamble pulse or any combination of successive rising and falling edges in a data signal, as referenced in "Adaptive Clock Skew and Duty Cycle Compensation for a Serial Data Bus", (US Patent 5,467,464, Oprescu *et al.*). However, the method described by Oprescu *et al.* requires a large number of clocks, including clock multiplexers and complicated circuitry for the data sampling, decoder and detector units.

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In "Skew-Insensitive Low Voltage Differential Receiver", (International Application Number WO 99/55000), LEE *et al.* further discloses a method of determining the amount of skew through transition and over-sampling circuits.

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However, the disclosed techniques above require the use of convoluted sampling circuits or clock generation circuits which are susceptible to process shifts and variations, and may result in stability and resilience issues particularly with respect to thermal and voltage variations.

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Therefore, there exists a need to provide a system and method for phase shift calibration to address one or more of the problems mentioned above.

30 SUMMARY

In accordance with a first aspect of the present invention, there is provided a method of calibrating a phase shift to an input clock signal for the detection of data in an input data signal comprising the steps of: receiving the input clock signal; receiving the input data signal including a predefined data pattern; consecutively

generating a plurality of output clock signals of different phase shifts with respect to the input clock signal using a programmable clock circuit; and determining for each of the output clock signals, whether the predefined data pattern is detected.

5 The different phase shifts may be increasing phase shifts.

 The method may further comprise determining a widest working range of output clock signals wherein each output clock signal in the widest working range provides for the detection of the predefined data pattern; and selecting one output
10 signal from the widest working range of output clock signal.

 The step of determining the widest working range may further comprise: predefined data detecting a first consecutive sequence of output clock signals which provide for the detection of the predefined data pattern; storing the first consecutive
15 sequence as the widest working range; comparing, if available, subsequently detected consecutive sequences with the stored widest working range; and replacing the stored widest working range each of available subsequently detected consecutive sequences when the one or more subsequently detected consecutive sequences is wider than the stored widest working range.
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 The step of selecting said one output clock signal may comprises selecting the center output clock signal of the widest working range as said one output clock signal.

25 The step of selecting said one output clock signal may comprise selecting either one of the center output clock signals of the widest working range as the said one output clock signal.

 The step of generating a plurality of output clock signals of increasing phase
30 shifts with respect to the input clock signal may comprise delaying the input clock signal with a series of delays, each delay output generating a respective output clock signal.

The input clock signal may be in differential form and the step of receiving the input clock signal may further comprise converting the input clock signal into a full-swing form.

5 The input data signal may be in differential form and the step of receiving the input data signal may further comprise converting the input data signal into a full-swing form.

10 The method may further comprise the step of multiplying the input clock signal to modify the frequency of the input clock signal to match that of the input data signal.

The input data signal may comprise a plurality parallel input data signals.

15 The clock signal may comprise one clock signal.

The clock signal may comprise a plurality of clock signals, each clock signal associated to a respective one of the parallel input signals.

20 In accordance with a second aspect of the present invention, there is provided a system for calibrating a phase shift to an input clock signal for the detection of data in an input data signal comprising: a clock receiver for receiving the input clock signal; a data receiver for receiving the input data signal including a predefined data pattern; a programmable clock circuit for consecutively generating a
25 plurality of output clock signals of different phase shifts with respect to the input clock signal; and a control logic for determining for each of the output clock signals, whether the predefined data pattern is detected.

The different phase shifts may be increasing phase shifts.

30 The system may further comprise means for determining a widest working range of output clock signals wherein each output clock signal in the widest working range provide for the detection of the predefined data pattern; and a selector for selecting one output signal from the widest working range of output clock signal.

The means for determining the widest working range may further comprise: a first detector detecting a first consecutive sequence of output clock signals which provides for the detection of the predefined data pattern; means for storing the first consecutive sequence as the widest working range; means for comparing, if available, subsequently detected consecutive sequences with the stored widest working range; and means for replacing the stored widest working range each of available subsequently detected consecutive sequences when the one or more subsequently detected consecutive sequences is wider than the stored widest working range.

The selector may select the center output clock signal of the widest working range as said one output clock signal.

The selector may select either one of the center output clock signals of the widest working range as the said one output clock signal

The programmable clock circuit may comprise: a series of delays for delaying the input clock signal, each delay output generating a respective output clock signal.

The input clock signal may be in differential form and the clock receiver further comprises means for converting the input clock signal into a full-swing form.

The input data signal may be in differential form and the data receiver further comprises means for converting the input data signal into a full-swing form.

The programmable clock circuit may further comprise a clock multiplier for multiplying the input clock signal to modify the frequency of the input clock signal to match that of the input data signal.

The input data signal may comprise a plurality parallel input data signals.

The clock signal may comprise one clock signal.

The clock signal may comprise a plurality of clock signals, each clock signal associated to a respective one of the parallel input signals.

In accordance with a third aspect of the present invention, there is provided a computer readable data storage medium having stored thereon computer code means for instructing a computer to execute a method of calibrating a phase shift to an input clock signal for the detection of data in an input data signal comprising the steps of: receiving the input clock signal; receiving the input data signal including a predefined data pattern; consecutively generating a plurality of output clock signals of different phase shifts with respect to the input clock signal using a programmable clock circuit; and determining for each of the output clock signals, whether the predefined data pattern is detected.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1 illustrates an example embodiment of a data output circuit.

Figure 2 illustrates a Phase Shift Search Range indicating the working ranges.

Figure 3 illustrates the calibration process for determining and performing the phase shift calibration in the example embodiment.

Figure 4 shows the example embodiment of the data output circuit illustrating the individual units in detail.

Figure 5 shows a flow chart illustrating a method for Phase Shift Calibration.

Figure 6 illustrates the method and system of the example embodiment implemented on a computer system.

DETAILED DESCRIPTION

Embodiments of the present invention seek to exploit use of a predefined data
5 pattern in the data stream to determine the timing skew through an open loop detection
scheme. A control logic varies the sampling clock across a phase shift range through a
programmable clock circuit to identify working ranges where the predefined data pattern
is recognised. The control logic then selects an optimal phase shift for the sampling
clock based on the identified working ranges.

10 Some portions of the description which follows are explicitly or implicitly
presented in terms of algorithms and functional or symbolic representations of
operations on data within a computer memory. These algorithmic descriptions and
functional or symbolic representations are the means used by those skilled in the data
15 processing arts to convey most effectively the substance of their work to others skilled in
the art. An algorithm is here, and generally, conceived to be a self-consistent sequence
of steps leading to a desired result. The steps are those requiring physical manipulations
of physical quantities, such as electrical, magnetic or optical signals capable of being
stored, transferred, combined, compared, and otherwise manipulated.

20 Unless specifically stated otherwise, and as apparent from the following, it will be
appreciated that throughout the present specification, discussions utilizing terms such as
“scanning”, “determining”, “replacing”, “generating”, “initializing”, “comparing”, or the like,
refer to the action and processes of a computer system, or similar electronic device, that
25 manipulates and transforms data represented as physical quantities within the the
computer system into other data similarly represented as physical quantities within the
computer system or other information storage, transmission or display devices.

30 The present specification also discloses apparatus for performing the operations
of the methods. Such apparatus may be specially constructed for the required purposes,
or may comprise a general purpose computer or other device selectively activated or
reconfigured by a computer program stored in the computer. The algorithms and
displays presented herein are not inherently related to any particular computer or other
apparatus. Various general purpose machines may be used with programs in

accordance with the teachings herein. Alternatively, the construction of more specialized apparatus to perform the required method steps may be appropriate. The structure of a conventional general purpose computer will appear from the description below.

5 In addition, the present specification also implicitly discloses a computer program, in that it would be apparent to the person skilled in the art that the individual steps of the method described herein may be put into effect by computer code. The computer program is not intended to be limited to any particular programming language and implementation thereof. It will be appreciated that a variety of programming
10 languages and coding thereof may be used to implement the teachings of the disclosure contained herein. Moreover, the computer program is not intended to be limited to any particular control flow. There are many other variants of the computer program, which can use different control flows without departing from the spirit or scope of the invention.

15 Furthermore, one or more of the steps of the computer program may be performed in parallel rather than sequentially. Such a computer program may be stored on any computer readable medium. The computer readable medium may include storage devices such as magnetic or optical disks, memory chips, or other storage devices suitable for interfacing with a general purpose computer. The computer readable
20 medium may also include a hard-wired medium such as exemplified in the Internet system, or wireless medium such as exemplified in the GSM mobile telephone system. The computer program when loaded and executed on such a general-purpose computer effectively results in an apparatus that implements the steps of the preferred method.

25 Figure 1 illustrates an example embodiment of a data output circuit 100. The data output circuit 100 comprises of a pair of differential/single-ended receivers 102 and 104 for receiving an input data signal DataIn 106 and an input clock signal ClockIn 108 respectively. The data output circuit 100 further comprises a data sampling circuit 110, a clock circuit 112, a control logic 114 and a de-serialization circuit 116. The data output
30 circuit 100 generates output data and clock signals DataOut 118 and ClockOut 120, which respectively represent the de-serialized data and the clock for the de-serialized data.

The functions of the differential/single-ended receivers 102 and 104 are known to a person skilled in the art and are not described in detail here. In general, differential/single-ended receivers 102 and 104 convert the DataIn and ClockIn signals into appropriately formatted signals DataInB 103 and ClockInB 105 for further processing by the respective Data Sampling and Clock Circuits 110 and 112. For example, the differential/single-ended receivers 102 and 104 may comprise buffers or differential-to-CMOS convertors to convert the input signals DataIn 106 and ClockIn 108 into full swing signals DataInB 103 and ClockInB 105.

In the example embodiment, based on the full swing signal ClockInB 105, the clock circuit 112 implements clock multiplication (if necessary) and clock phase-shifting to generate a sampling clock signal SCLK 107 and an output clock signal ClockOut 120. Clock multiplication may be used to match the frequency of SCLK 107 with DataInB 103. For example, assuming DataInB 103 and ClockInB 105 were of 280Mhz and 40Mhz respectively. For DDR data sampling, ClockInB 105 would have to be multiplied by a factor of 3.5 such that the output SCLK 107 is at 140Mhz to match the DataInB 103 frequency. The clock circuit 112 also provides further phase shifting to SCLK 107 over a range of e.g. -5ns to 5ns in incremental steps of e.g. 0.1ns.

The sampled data bits DataS 111 is then received by the de-serialization circuit 116. It will be appreciated by a person skilled in the art that various forms of de-serialization may be performed. For example, the de-serialization circuit may provide storage to store bursts of seven individual data bits on DataS 111 which forms a data frame according to specific signal protocol. Each stored burst of seven bits within a data frame are then organized according to specific data protocol and output simultaneously as a single 7 bit parallel stream as DataOut 118. The frequency of the output data stream DataOut 118 may also be of a different frequency than the original serial data DataIn 106 frequency. For continuous data flow, since 7 bits of data are received before output, the output frequency is lowered to one-seventh the original frequency. In other words, a 280Mhz DataIn 108 has a corresponding DataOut 118 and ClockOut 120 of 40Mhz. This ClockOut 120 frequency of 40Mhz can be generated by the Clock Circuit 112 through phase shifting and clock division (if necessary).

The control logic 114 controls the operation of clock circuit 112, providing instructions to perform the clock phase shifting as described earlier. The control logic interacts with a host (not illustrated here) to override the phase shift setting and reports the status of the phase shift calibration, e.g. calibration in progress, calibration
5 succeeded or calibration failed. It also receives instructions from the host to perform the searches for the optimized phase shift setting.

The data output circuit 100 can be implemented totally or partially in a FPGA (Field Programmable Grid Array), e.g. Xilinx Virtex-II or later FPGA family. In Xilinx
10 Virtex-II or later FPGA family, differential/single-ended receivers and data sampling can be implemented in Input/Output Blocks, clock circuit in Digital Clock Manager, and the others in Configurable Logic Blocks.

The detailed operation in the control logic 114 for phase shift calibration is
15 elaborated below. As described earlier, if the data stream contains a predefined data pattern, which may be periodic, the predefined data pattern is used as indication whether the sampling clock edge is within the valid data window. If the data stream does not contain a predefined data pattern, an initial training period can be incorporated to send a known calibration data pattern for calibration purpose.

The embodiment described below illustrates the calibration process for the
20 scenario where known calibration data is sent during an initial training period. For clarity and simplicity, the data and clock input rates are the same and hence no clock multiplication is used for sampling in the described example embodiment, but may be
25 employed in other embodiments.

With further reference to figure 1, the control logic 114 is initially in the "Idle" state. Upon receipt of a calibration trigger from the host (not illustrated), the control logic begins the calibration process and the control logic 114 status is changed to a
30 "calibration in progress" state. The clock circuit 112 is designed to provide a range of phase shifts or time delays, known hereinafter as the Phase Shift Search Range.

In the example embodiment, the Clock Circuit 112 can be controlled by the Control Logic 114 to impose a plurality of phase shifts to the ClockInB signal 105 to

produce phase shifted versions of ClockInB 105. Phase shifted versions of the ClockInB signal 105, SCLK 107 are generated one at a time in incremental phase-shift fashion until the range of phase shifts in the entire Phase Shift Search Range has been exhausted. With each generated sampling clock SCLK 107, the Data Sampling Circuit

5 110 samples the data on the DataInB signal 103, the control logic 114 checks for the predefined data pattern in data out 118. For each SCLK 107 which successfully detects the predefined data pattern, the associated phase shift value is considered as a working value. Working phase shift ranges comprising one or more consecutive working values are stored in the Control Logic 114.

10 As the phase-shifted versions of the ClockInB signal, SCLK 107, are generated one at a time, and not in parallel, the predefined data pattern is transmitted repeatedly, for subsequent receipt by the receiver 102, until data sampling with all possible SCLK 107 is achieved and calibration is complete.

15 It will be appreciated that any number of delays of any magnitude may be used to provide for the phase shift to ClockInB 105. For example, for -50 to 50 time delays of 0.1ns may be used to provide a Phase Shift Search Range of -5ns to 5ns. The Search Range required depends on the specific application. In another example, the search

20 range covers the duration of one complete data frame which may consist of several sampling clock cycles according to a specific signal protocol, e.g. 25ns.

It will also be appreciated that the Clock Circuit 112 may be a programmable clock circuit capable of being controlled by the Control Logic 114 to impose the plurality

25 of phase shifts to ClockInB 105.

Figure 2 illustrates a Phase Shift Search Range 200 indicating the working ranges 202a, 202b. As illustrated, more than one working ranges 202a, 202b can be detected. As the control logic 114 scans phase shifts across the entire Phase Shift

30 Search Range 200 (from the lowest phase shift 204a to the highest (or maximum) phase shift 204j) for working values of SCLK 107, the working ranges 202a, 202b are detected one at a time, with the widest working range being recorded. Upon reaching the highest phase shift 204j, the widest working range 202b is retrieved, as the spurious ranges 202a have been removed. The centre 206 of the widest working range 202a is defined

as the optimized phase shift and this completes the calibration process. After the calibration, the defined optimized phase shift is incorporated into the ClockInB 105 (Figure 1) to generate the optimised sampling clock SCLK 107 (Figure 1). In instances where the widest working range comprises of an even number of working phase shifted clock signals, there can be two centres, and either one of the two centres can be selected as the optimised phase shifted clock signal.

Figure 3 illustrates the calibration process 300 for determining and performing the phase shift calibration in the example embodiment. At step 302, the control circuit 114 (Figure 1) is initially in an idle state, the working range parameters and phase shift setting are at initial values, e.g. start and end point of working range and phase shift setting are at same value equivalent to $\frac{1}{2}$ sampling clock period in SDR or $\frac{1}{4}$ sampling clock period in DDR. Upon receipt of a calibrate phase shift instruction, at step 304, the control circuit 114 (Figure 1) sets the phase shift to SCLK 107 (Figure 1) to the lowest phase shift 204a (Figure 2) in the entire Phase Shift Search Range 200 (Figure 2). At step 306, the newly phase shifted SCLK 107 is used to sample for the predefined data pattern. If the predefined data pattern is correctly detected, it is also checked for stability for multiple consecutive repetitions, e.g. 100, of the predefined data pattern at step 308 to ensure stable detection of the predefined data pattern. If the predefined data pattern is not detected or is unstable, the phase shift to SCLK is incremented until the predefined data pattern is stably detected or the highest phase shift in the Phase Shift Search Range 200 is reached (steps 310 and 312).

When the predefined data pattern is stably detected by an SCLK 107 of particular phase shift, a working phase range "start" point has been determined. The process then moves to search for the corresponding working phase range "end" point. The working phase range "ends" when a) a further incremental phase shift to SCLK 107 does not allow the correct and stable detection of the predefined data pattern or b) when the highest phase shift in the Phase Shift Search Range 200 (figure 2) has been reached, as illustrated in steps 314, 316, 318 and 320. Once the "end" point of the working phase range is determined, a working phase shift range is deemed detected at step 320 and the process returns to step 310 to search for a new working phase range "start" point, and the cycle repeats itself until the highest phase shift in the Phase Shift Search Range 200 (figure 2) is reached. The parameters (start and end points) of the widest of the

earlier working phase shift ranges (measured in terms of e.g. delay elements) are stored as the widest working phase shift range. With each detection of working phase shift ranges at step 320, the newly detected working phase shift range is compared with the stored range. If the newly detected range exceeds that of the stored range, the stored parameters are replaced with the new parameters.

Upon return to step 310, if the highest phase shift is reached, step 302 is returned to. The set phase shift command would then set the phase shift to an optimized phase shift which is determined as the mid point of the stored working phase shift range (step 322).

In the example embodiments, a single data signal is described. However, it will be appreciated by a person skilled in the art a plurality of data signals can be received. In such a circuit, the data signals can be taken as a single set and the same skew is assumed and hence only one clock circuit can be used for all the data signals. Alternatively, if the skew among the plurality of data signals is different, the calibration be done for individual data signals, each data signal having its own corresponding clock circuit.

Further, the calibration process can be triggered either manually after the connection is ready or automatically when the forwarded input clock is detected.

Figure 4 shows the example embodiment of the data output circuit illustrating the individual units in detail. As shown in Figure 4, only one data sampling circuit 110 is used. Each serial data input signal (A0_In, A1_In, A2_In or A3_In) 106a-d is first received by respective differential receivers 102a-d and converted into the appropriately formatted signals A0_InB, A1_InB, A2_InB and A3_InB 103a-d. In the case of SDR data, A0_InB, A1_InB, A2_InB and A3_InB 103a-d are then clocked in by a respective one of D-type Flip-flops 410a-d as illustrated. It will be appreciated that in the case of DDR data, two D-type Flip-flops may be required for each data input stream instead.

The sampling clock signal SCLK 107 is generated by the Clock Circuit 112. In the example embodiment, the Clock Circuit 112 uses only one variable phase shift unit 412 and one clock multiplier 414. The Clock Circuit 112 can be implemented in different

ways, including , but not limited to, by using Digital Clock Manager (DCM) in Xilinx Virtex-II FPGA devices, enhanced phase-locked loop (PLL) in Altera Cyclone™ FPGA devices or stand alone PLL-Based clock synthesizer, e.g. CDC5801A from Texas Instruments Incorporate or ICS1523 from Integrated Device Technology, Inc. As
 5 described earlier, the Clock Multiplier 414 may not be necessary. The Clock Circuit 112 also generates the reference output clock signal Clock Out 120 for the de-serialized or parallel data. Clock Out 120 for the parallel data is generally in the same phase with the data sampling clock SCLK 107.

10 The variable phase shift implemented by the Variable Phase Shift unit 412 in the Clock Circuit 412 is controlled by the Control Logic 114. The Control Logic 114 varies the phase shift via the Phase Shift Set unit 416 and subsequently ascertains if the known pattern is received correctly via the Pattern Check unit 418 to finally determine the optimized phase shift setting. The process of searching for the optimized phase shift
 15 setting is operated by the State Machine 420, as illustrated in Figure 3. The Control Logic 114 also provides access to the host processor (not illustrated) to override the current phase shift setting and to check the status of the search.

As will be appreciated by a person skilled in the art, the de-serialization unit 116
 20 determines a data frame according to specific signal protocol and organizes the serial data into a parallel data according to specific data protocol. For example, in OpenLDI signals, the de-serialized parallel data are R7-R0, G7-G0, B7-B0, VSYNC, HSYNC and DE in each cycle of Clock Out 120. In such an example, HSYNC would be ideal to be used as a known data pattern.

25 Figure 5 shows a flow chart illustrating a method for Phase Shift Calibration to an input clock signal for the detection of data in an input data signal 500. At step 502, the input clock signal is received. At step 504, the input data signal including a predefined data pattern is received. At step 506, a plurality of output clock signals of
 30 using a programmable clock circuit of different phase shifts with respect to the input clock signal is consecutively generated. At step 508, for each of the output clock signals, it is determined whether the predefined data pattern is detected.

The embodiments of the invention can provide a variety of benefits, some of which are described as follows:

- 5 1) Minimized data error. The embodiments enable automatic calibration of phase shift to compensate for the timing skew between clock and data signals, and can ensure the data sampling is performed in the center of valid data window, minimizing the data error.
- 2) Optimise noise margin. By sampling data in the center of the valid data window, the noise margin can also be optimized.
- 10 3) Adaptation to different cable length and quality. Different cable length and quality can cause different timing skew between clock and data if the signal rates are different. The embodiments automatically calibrate the phase shift to compensate for the timing skew between clock and data signals introduced by the cable in the implementations.
- 15 4) Adaptation to skew between clock and data introduced by factors including the transmitter and receiver circuitry, the clock recovery and multiplication circuits in the receiver, different PCB track lengths.
- 5) Elimination of design changes for different phase shift setting to compensate different timing skew due to different cable length or other factors. The embodiments enable automatic calibration in design where the phase shift can be automatically determined, recorded and set.
- 20 6) Automatic calibration instead manual measurements. In the embodiments, the optimized phase shift can be determined automatically.
- 7) No extra sampling circuit, clock circuit, measurement circuit or detector circuits. For example, embodiments of the present invention can use only one data sampling circuit for the serial data inputs. Even in the scenario where n different clocks are used for n serial inputs, e.g. because of different skew on different input lines, n is usually small.
- 25 8) Easy implementation in a programmable logic device, e.g. FPGA
- 30

The method and system of the example embodiment can be implemented on a computer system 600, schematically shown in Figure 6. It may be implemented as software, such as a computer program being executed within the computer system

600, and instructing the computer system 600 to conduct the method of the example embodiment.

5 The computer system 600 comprises a computer module 602, input modules such as a keyboard 604 and mouse 606 and a plurality of output devices such as a display 608, and printer 610.

10 The computer module 602 is connected to a computer network 612 via a suitable transceiver device 614, to enable access to e.g. the Internet or other network systems such as Local Area Network (LAN) or Wide Area Network (WAN).

15 The computer module 602 in the example includes a processor 618, a Random Access Memory (RAM) 620 and a Read Only Memory (ROM) 622. The computer module 602 also includes a number of Input/Output (I/O) interfaces, for example I/O interface 624 to the display 608, and I/O interface 626 to the keyboard 604.

20 The components of the computer module 602 typically communicate via an interconnected bus 628 and in a manner known to the person skilled in the relevant art.

25 The application program is typically supplied to the user of the computer system 600 encoded on a data storage medium such as a CD-ROM or flash memory carrier and read utilising a corresponding data storage medium drive of a data storage device 630. The application program is read and controlled in its execution by the processor 618. Intermediate storage of program data maybe accomplished using RAM 620.

30 It will be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

CLAIMS

1. A method of calibrating a phase shift to an input clock signal for the detection of data in an input data signal comprising the steps of:

- 5 receiving the input clock signal;
receiving the input data signal including a predefined data pattern;
consecutively generating a plurality of output clock signals of different phase shifts with respect to the input clock signal using a programmable clock circuit; and
determining for each of the output clock signals, whether the predefined data
10 pattern is detected.

2. The method as claimed in claim 1, wherein the different phase shifts are increasing phase shifts.

- 15 3. The method as claimed in claim 2, further comprises
determining a widest working range of output clock signals wherein each output clock signal in the widest working range provides for the detection of the predefined data pattern; and
selecting one output signal from the widest working range of output clock
20 signal.

4. The method as claimed in claim 3 wherein, the step of determining the widest working range further comprises:
predefined data detecting a first consecutive sequence of output clock
25 signals which provide for the detection of the predefined data pattern;
storing the first consecutive sequence as the widest working range;
comparing , if available, subsequently detected consecutive sequences with the stored widest working range; and
replacing the stored widest working range each of available subsequently
30 detected consecutive sequences when the one or more subsequently detected consecutive sequences is wider than the stored widest working range.

5. The method as claimed in claim 4, wherein the step of selecting said one output clock signal comprises:

selecting the center output clock signal of the widest working range as said one output clock signal.

5 6. The method as claimed in claim 4, wherein the step of selecting said one output clock signal comprises:

 selecting either one of the center output clock signals of the widest working range as the said one output clock signal

10 7. The method as claimed in any one of claims 2 to 6, wherein the step of generating a plurality of output clock signals of increasing phase shifts with respect to the input clock signal comprises:

 delaying the input clock signal with a series of delays, each delay output generating a respective output clock signal.

15 8. The method as claimed in any one of the preceding claims, wherein the input clock signal is in differential form and the step of receiving the input clock signal further comprises converting the input clock signal into a full-swing form.

20 9. The method as claimed in any one of the preceding claims, wherein the input data signal is in differential form and the step of receiving the input data signal further comprises converting the input data signal into a full-swing form.

25 10. The method as claimed in any one of the preceding claims, further comprising the step of multiplying the input clock signal to modify the frequency of the input clock signal to match that of the input data signal.

 11. The method as claimed in any one of the preceding claims, the input data signal comprises a plurality parallel input data signals.

30 12. The method as claimed in claim 11, wherein the clock signal comprises one clock signal.

13. The method as claimed in claim 11, wherein the clock signal comprises a plurality of clock signals, each clock signal associated to a respective one of the parallel input signals.

5 14. A system for calibrating a phase shift to an input clock signal for the detection of data in an input data signal comprising:

a clock receiver for receiving the input clock signal;

a data receiver for receiving the input data signal including a predefined data pattern;

10 a programmable clock circuit for consecutively generating a plurality of output clock signals of different phase shifts with respect to the input clock signal; and

a control logic for determining for each of the output clock signals, whether the predefined data pattern is detected.

15 15. The system as claimed in claim 14, wherein the different phase shifts are increasing phase shifts.

16. The system as claimed in claim 15, further comprises

20 means for determining a widest working range of output clock signals wherein each output clock signal in the widest working range provide for the detection of the predefined data pattern; and

a selector for selecting one output signal from the widest working range of output clock signal.

25 17. The system as claimed in claim 16 wherein, the means for determining the widest working range further comprises:

a first detector detecting a first consecutive sequence of output clock signals which provides for the detection of the predefined data pattern;

30 means for storing the first consecutive sequence as the widest working range;

means for comparing, if available, subsequently detected consecutive sequences with the stored widest working range; and

means for replacing the stored widest working range each of available subsequently detected consecutive sequences when the one or more subsequently detected consecutive sequences is wider than the stored widest working range.

5 18. The system as claimed in claim 17, wherein the selector selects the center output clock signal of the widest working range as said one output clock signal.

10 19. The system as claimed in claim 17, wherein the selector selects either one of the center output clock signals of the widest working range as the said one output clock signal

 20. The system as claimed in any one of claims 15 to 19, wherein the programmable clock circuit comprises:
15 a series of delays for delaying the input clock signal, each delay output generating a respective output clock signal.

 21. The system as claimed in any one of claims 14 to 20, wherein the input clock signal is in differential form and the clock receiver further comprises
20 means for converting the input clock signal into a full-swing form.

 22. The system as claimed in any one of claims 14 to 21, wherein the input data signal is in differential form and the data receiver further comprises
25 means for converting the input data signal into a full-swing form.

 23. The system as claimed in any one of claims 14 to 22, wherein the programmable clock circuit further comprises a clock multiplier for multiplying the input clock signal to modify the frequency of the input clock signal to match that of the input data signal.

30 24. The system as claimed in any one of claims 14 to 23, wherein the input data signal comprises a plurality parallel input data signals.

25. The system as claimed in claim 24, wherein the clock signal comprises one clock signal.

5 26. The system as claimed in claim 25, wherein the clock signal comprises a plurality of clock signals, each clock signal associated to a respective one of the parallel input signals.

10 27. A computer readable data storage medium having stored thereon computer code means for instructing a computer to execute a method of calibrating a phase shift to an input clock signal for the detection of data in an input data signal comprising the steps of:

receiving the input clock signal;
receiving the input data signal including a predefined data pattern;
consecutively generating a plurality of output clock signals of different phase
15 shifts with respect to the input clock signal using a programmable clock circuit; and
determining for each of the output clock signals, whether the predefined data pattern is detected.