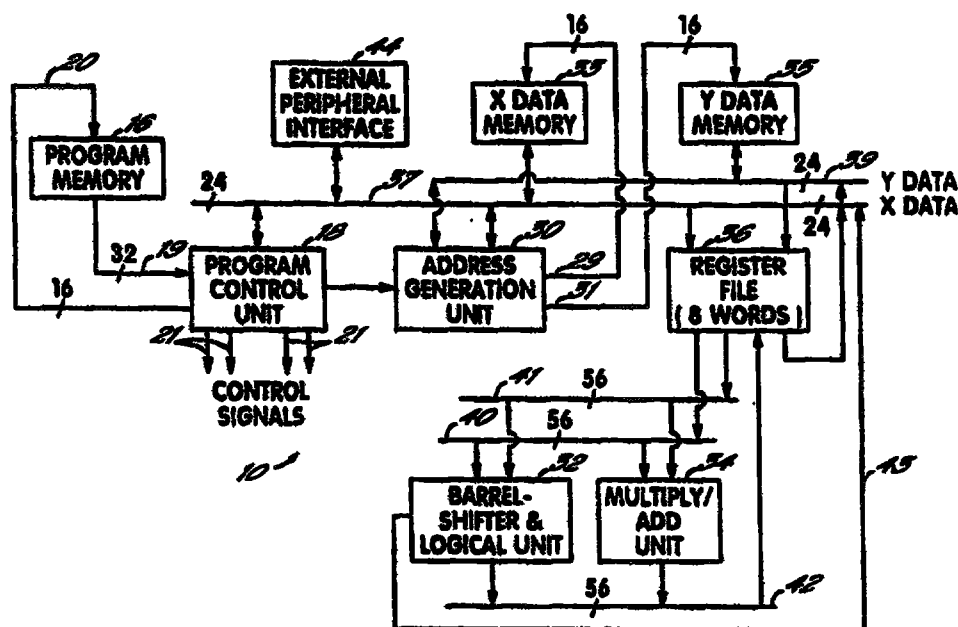




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 9/355		A2	(11) International Publication Number: WO 99/14665
			(43) International Publication Date: 25 March 1999 (25.03.99)
(21) International Application Number: PCT/US98/18699		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).	
(22) International Filing Date: 9 September 1998 (09.09.98)			
(30) Priority Data: 60/060,710 17 September 1997 (17.09.97) US 09/115,187 14 July 1998 (14.07.98) US			
(71) Applicant: SONY ELECTRONICS INC. [US/US]; 1 Sony Drive, Park Ridge, NJ 07656-8003 (US).			
(72) Inventors: TAN, Yew-Koon; 330 Elan Village Lane #106, San Jose, CA 95134 (US). OZEKI, Agee; 5-25-6-101, Hatano-Dai, Shinagawa-ku, Tokyo 142-0064 (JP). FUKUSHIMA, Tetsuya; 111-2-201, Zenb-Shou, Asahi-ku, Yokohama-shi, Kanagawa 241-0823 (JP).		Published Without international search report and to be republished upon receipt of that report.	
(74) Agents: HUMPHREY, Thomas, W. et al.; Wood, Herron & Evans, L.L.P., 2700 Carew Tower, Cincinnati, OH 45202 (US).			

(54) Title: DIGITAL SIGNAL PROCESSOR PARTICULARLY SUITED FOR DECODING DIGITAL AUDIO



(57) Abstract

A digital signal processor (10) particularly adapted for decoding digital audio. The barrel shifter (32) of the processor includes logical circuitry, so that operations involving a combination of a logical operation and a shift, can be performed in a single pass through the combined barrel shifter/logical unit, rather than requiring separate passes through the barrel shifter and ALU, which would require more instruction cycles. The address generator (30) of the processor, includes circuitry which concatenates the most significant bits of a base address of a table to the least significant bits of an index, to thereby rapidly generate addresses of indexed locations in a table.