CLAIMS:

1. A test circuit, comprising:

a signal processing module, which is configured to receive a pulse signal to be tested and output a processing signal under control of a control signal;

a sampling module, which is connected to the signal processing module and is configured to receive the processing signal and generate a sampling signal according to the processing signal;

wherein the signal processing module comprises a fourth inverter and a multiplexer, wherein a first input terminal of the multiplexer is connected to an output terminal of the fourth inverter, a second input terminal of the multiplexer and an input terminal of the fourth inverter are respectively configured to receive the pulse signal, and the multiplexer is used to receive the control signal and select to turn on the path between the first input terminal of the multiplexer and an output terminal of the multiplexer or the path between the second input terminal of the multiplexer and the output terminal of the multiplexer under control of the control signal, and the output terminal of the multiplexer is used to output the processing signal;

wherein the sampling module comprises a first D flip-flop, a first inverter and a second inverter, a clock driving terminal of the first D flip-flop is connected to the output terminal of the multiplexer, an input terminal of the first inverter is connected to an output terminal of the first D flip-flop, an output terminal of the first inverter is connected to an input terminal of the first D flip-flop, an input terminal of the second inverter is connected to the output terminal of the first inverter, and an output terminal of the second inverter is configured to output the sampling signal.

2. The test circuit of claim 1, wherein the pulse signal comprises four adjacent pulses in a time sequence, the sampling signal comprises a first sampling pulse and a second sampling pulse; and the signal processing module is configured to, in response to the control signal, invert a first pulse of the four adjacent pulses in the time sequence without inverting remaining pulses of the four adjacent pulses in the time sequence;

wherein the sampling module is configured to generate the first sampling pulse in response to first two pulses of the four adjacent pulses in the time sequence, and generate the second sampling pulse in response to last two pulses of the four adjacent pulses in the time sequence;

wherein the first sampling pulse and the second sampling pulse have a pulse width difference, and the pulse width difference is equal to a pulse width of the pulse signal.

3. The test circuit of claim 2, wherein the sampling module is configured to generate the first sampling pulse in response to different edges of the first two pulses, and generate the second sampling pulse in response to a same edge of the last two pulses.

4. The test circuit of claim 1, further comprising:

a control module, which is connected to the sampling module and the signal processing module respectively, and is configured to generate the control signal in response to the sampling signal, wherein an edge of the control signal corresponds to an edge of the sampling signal;

wherein the control module comprises a second D flip-flop, a clock driving terminal of the second D flip-flop is connected to the output terminal of the second inverter, an input terminal of the second D flip-flop is configured to receive a preset level signal, an output terminal of the second D flip-flop is connected to a control terminal of the multiplexer, and the second D flip-flop is used to, in response to the sampling signal, sample the preset level signal to generate the control signal.

5. A test apparatus, comprising:

a test circuit according to any one of claims 1 to 4;

an analysis module, which is connected to the sampling module and is configured to obtain a pulse width of the pulse signal according to the first sampling pulse and the second sampling pulse.

6. A test method, based on the test apparatus according to claim 5, wherein the

method comprising:

receiving a pulse signal to be tested;

outputting a processing signal under a control signal;

generating a sampling signal according to the processing signal, wherein the sampling signal comprises a first sampling pulse and a second sampling pulse;

obtaining a pulse width of the pulse signal according to the first sampling pulse and the second sampling pulse;

wherein the first sampling pulse and the second sampling pulse have a pulse width difference, and the pulse width difference is equal to the pulse width of the pulse signal.