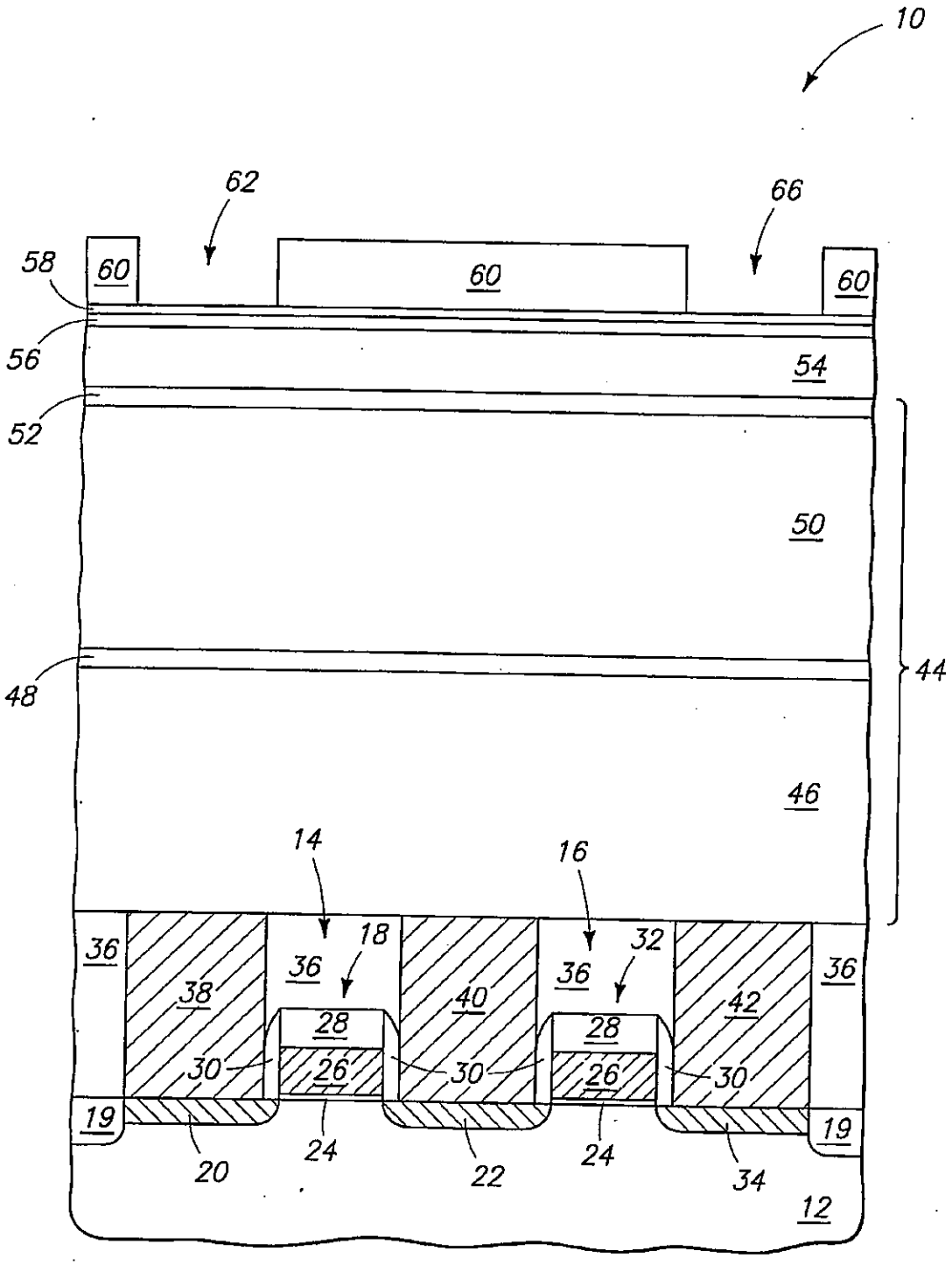


Fig 1
PRIOR ART

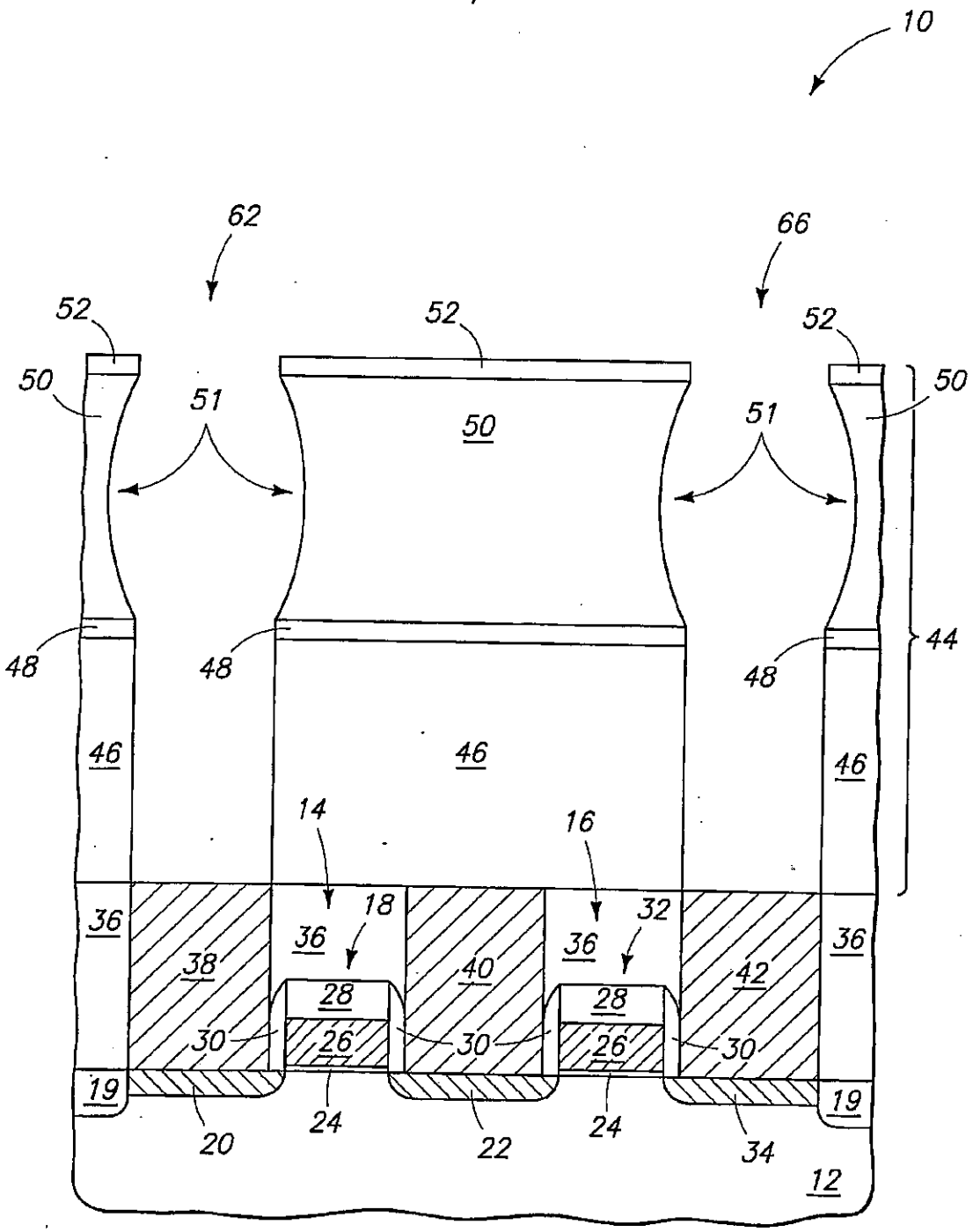


Fig 2
PRIOR ART

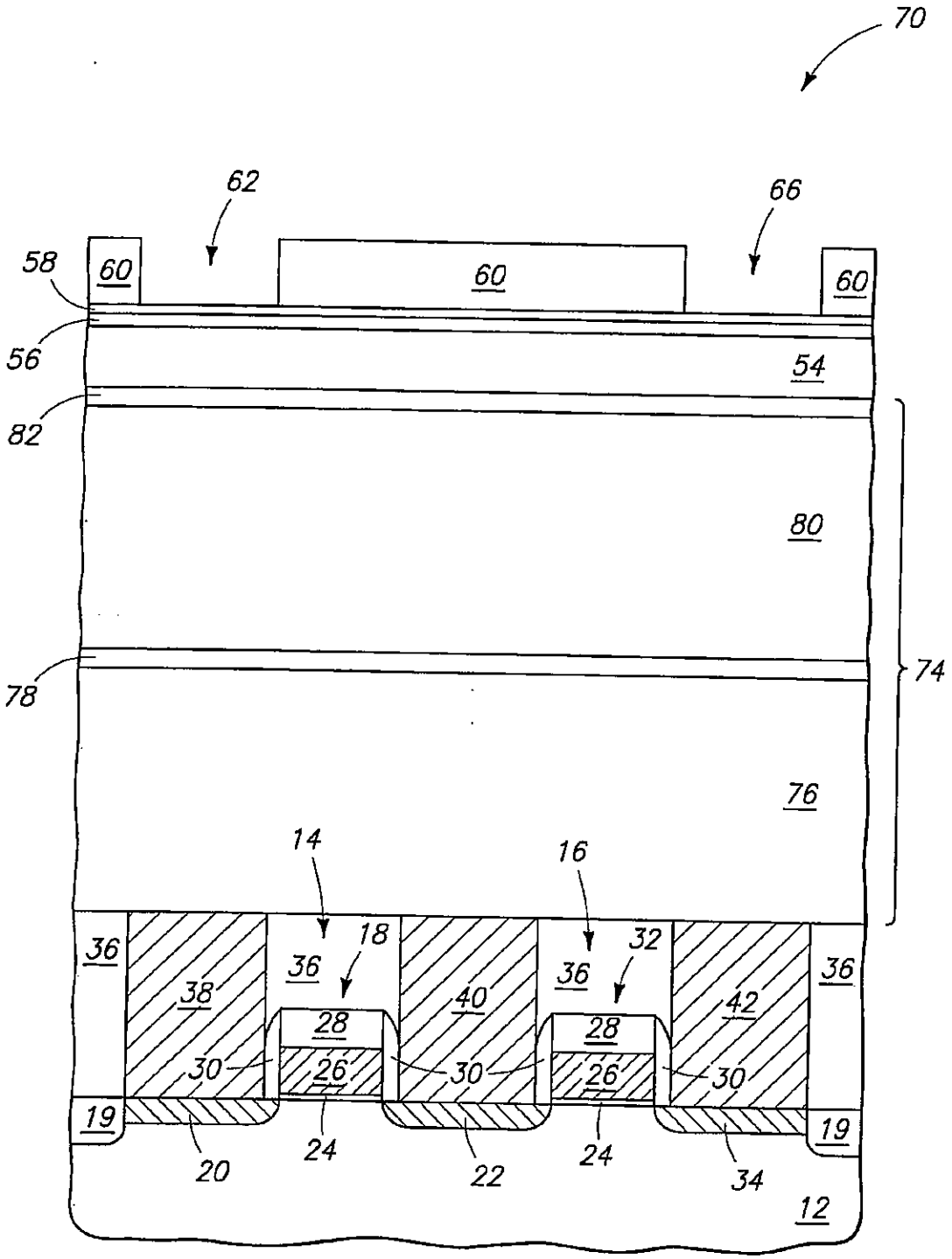

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Fig 3

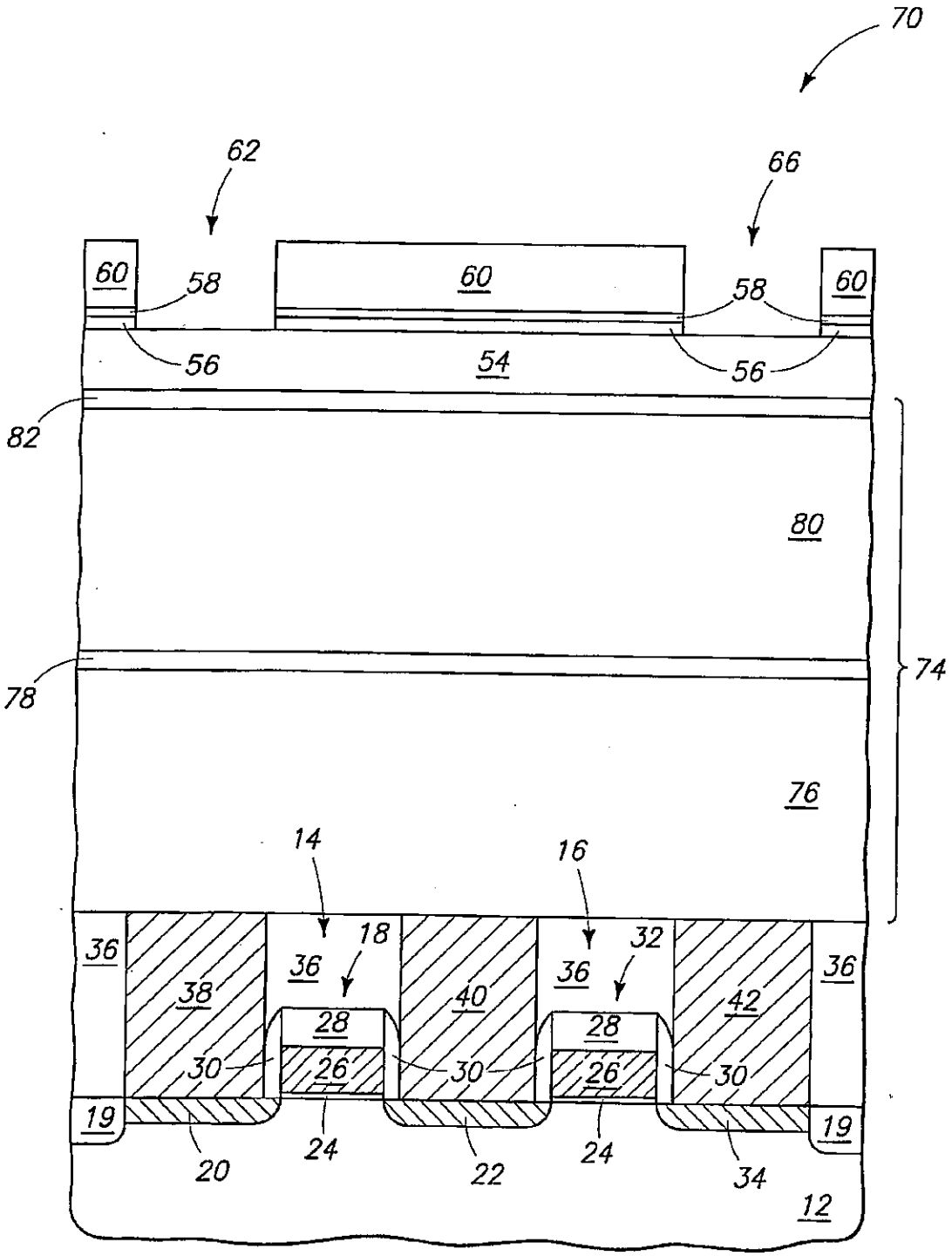

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Fig. 4

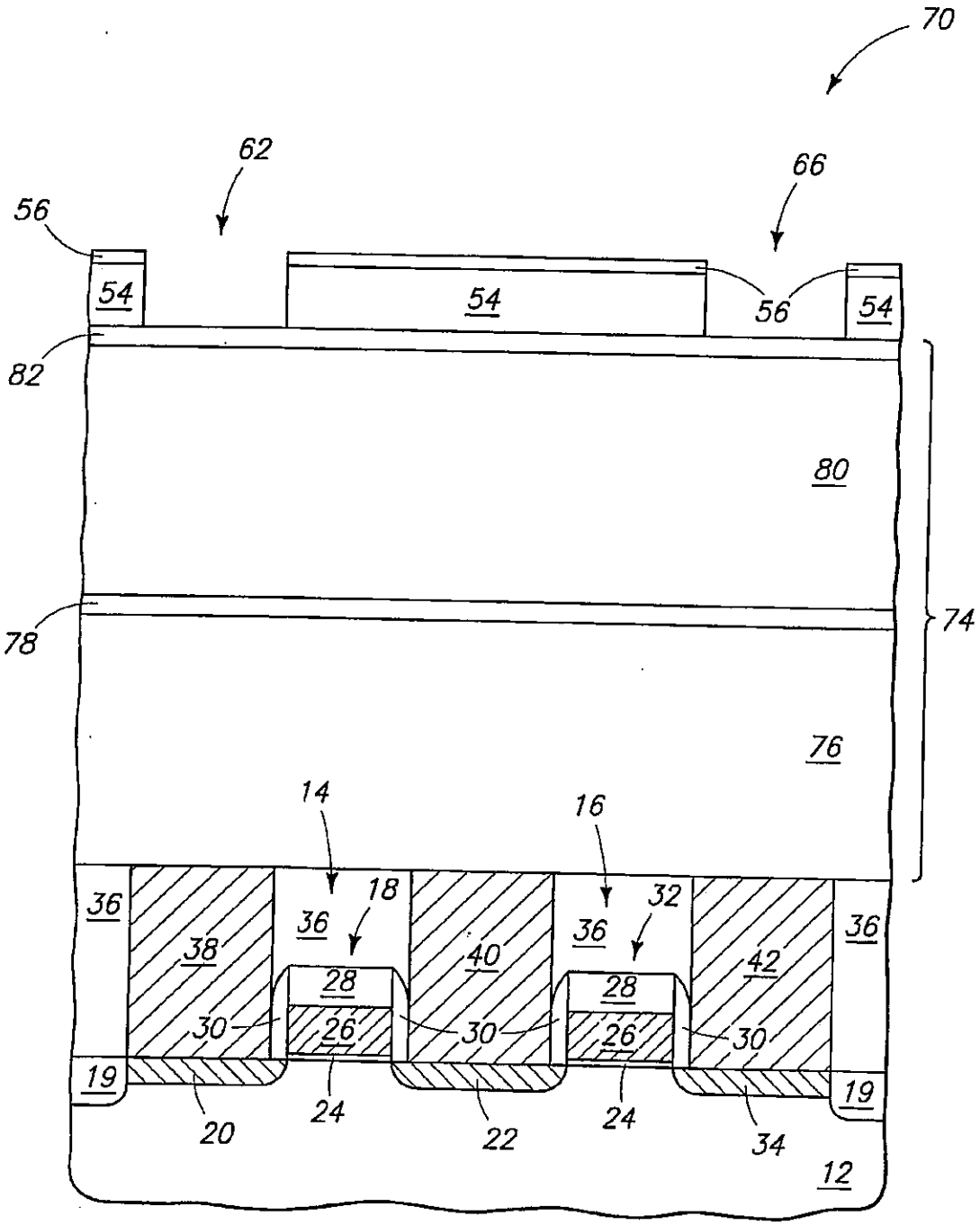

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Fig 5

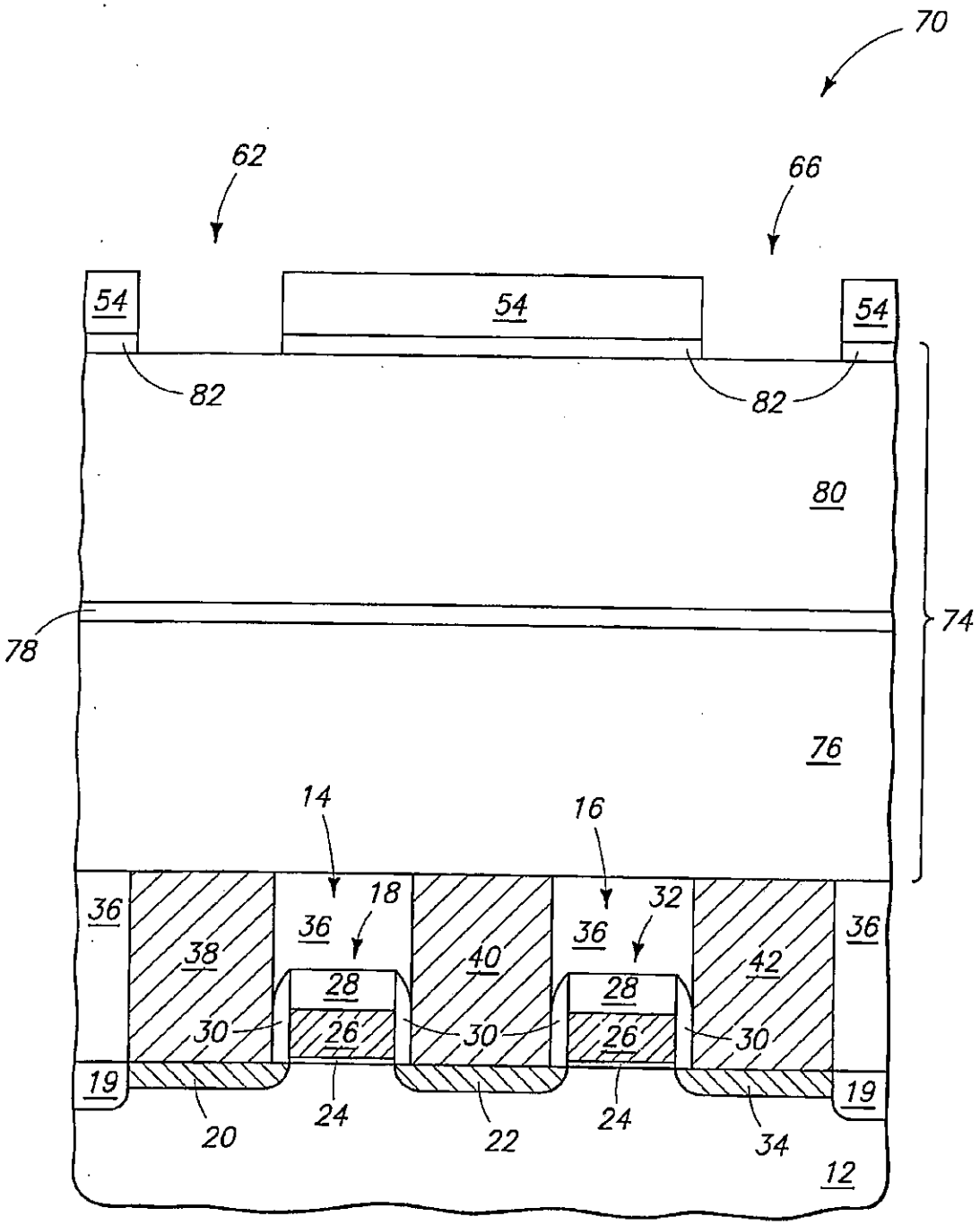

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Fig 6

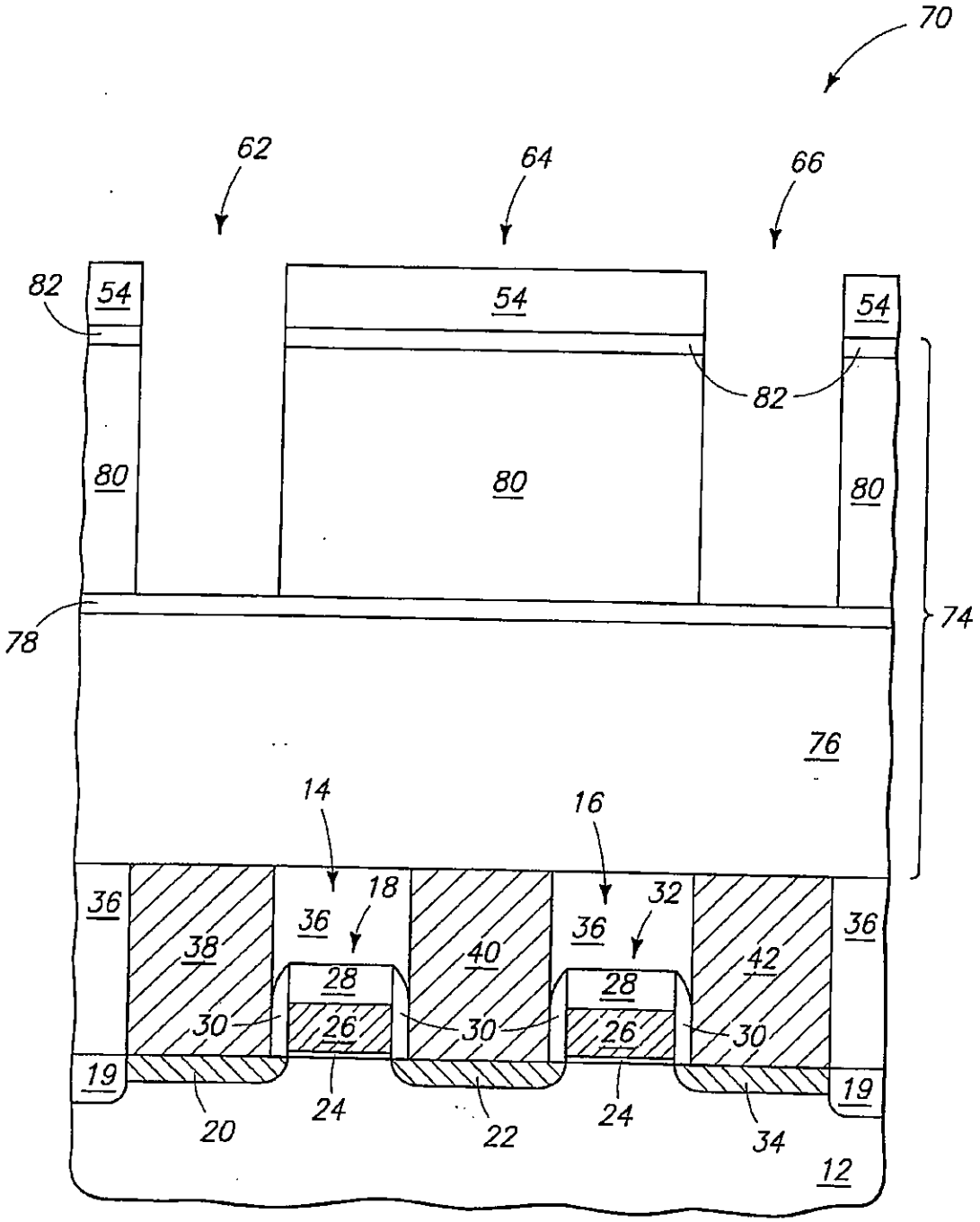

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Fig. 7

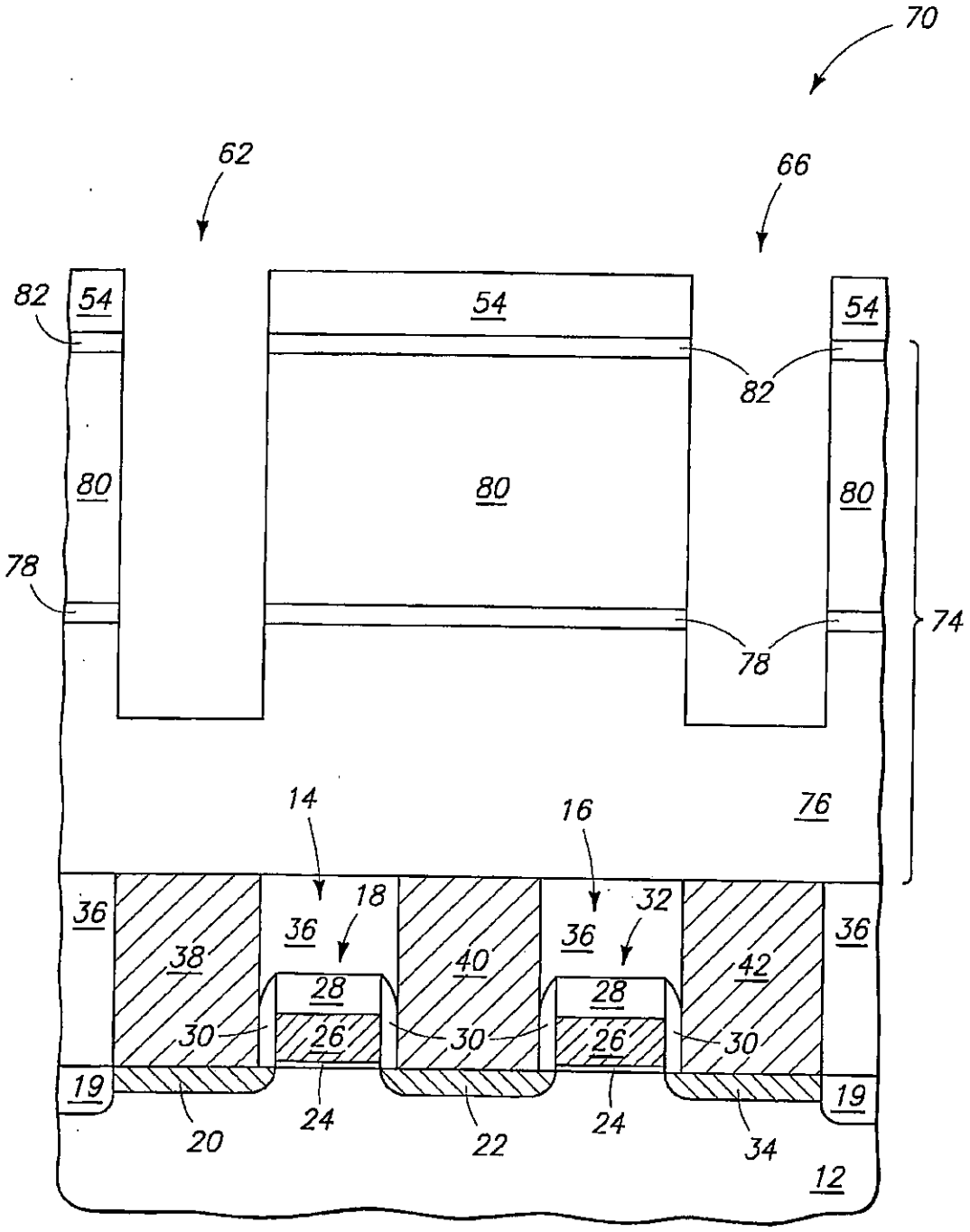

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Fig. 8

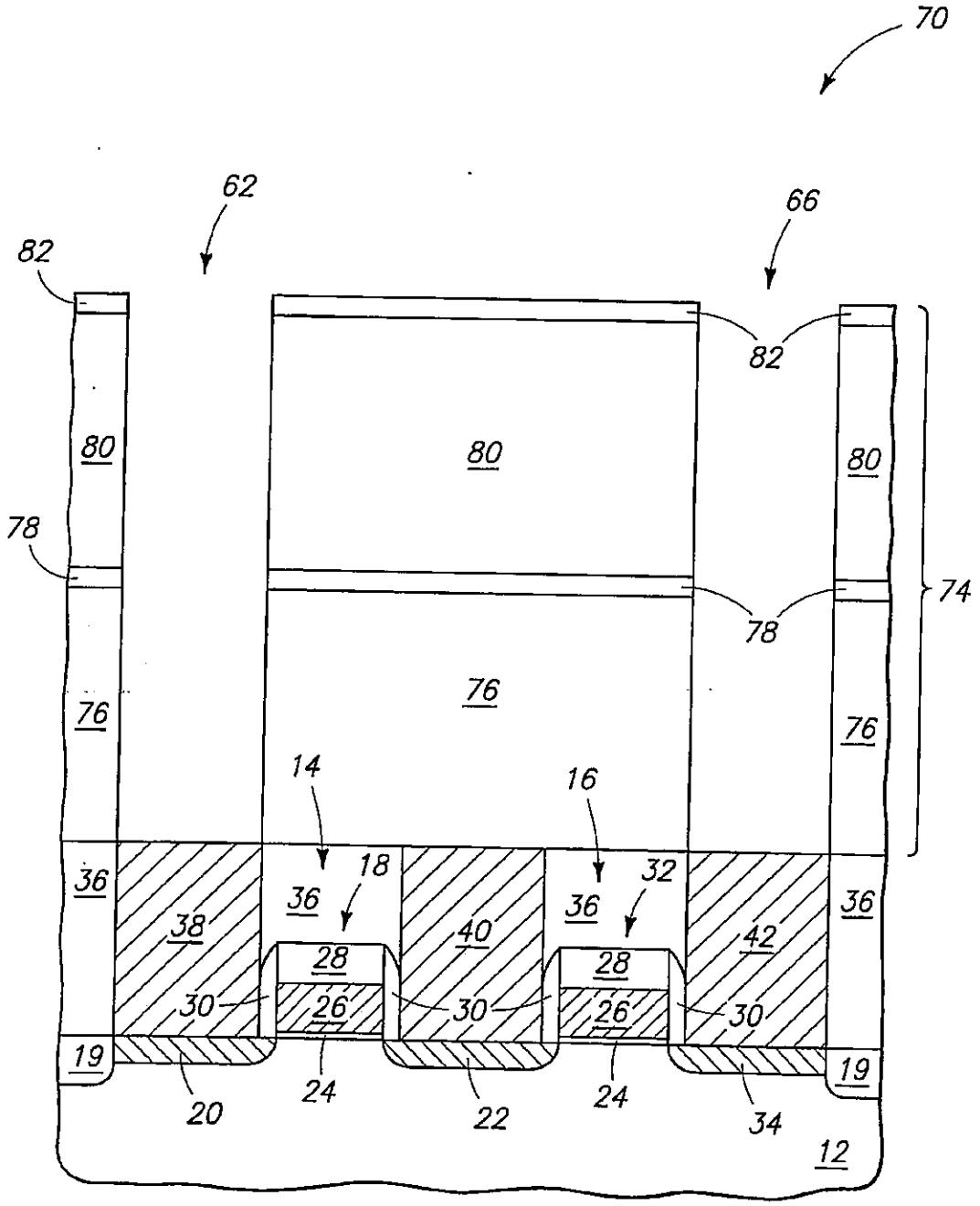

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Fig 9

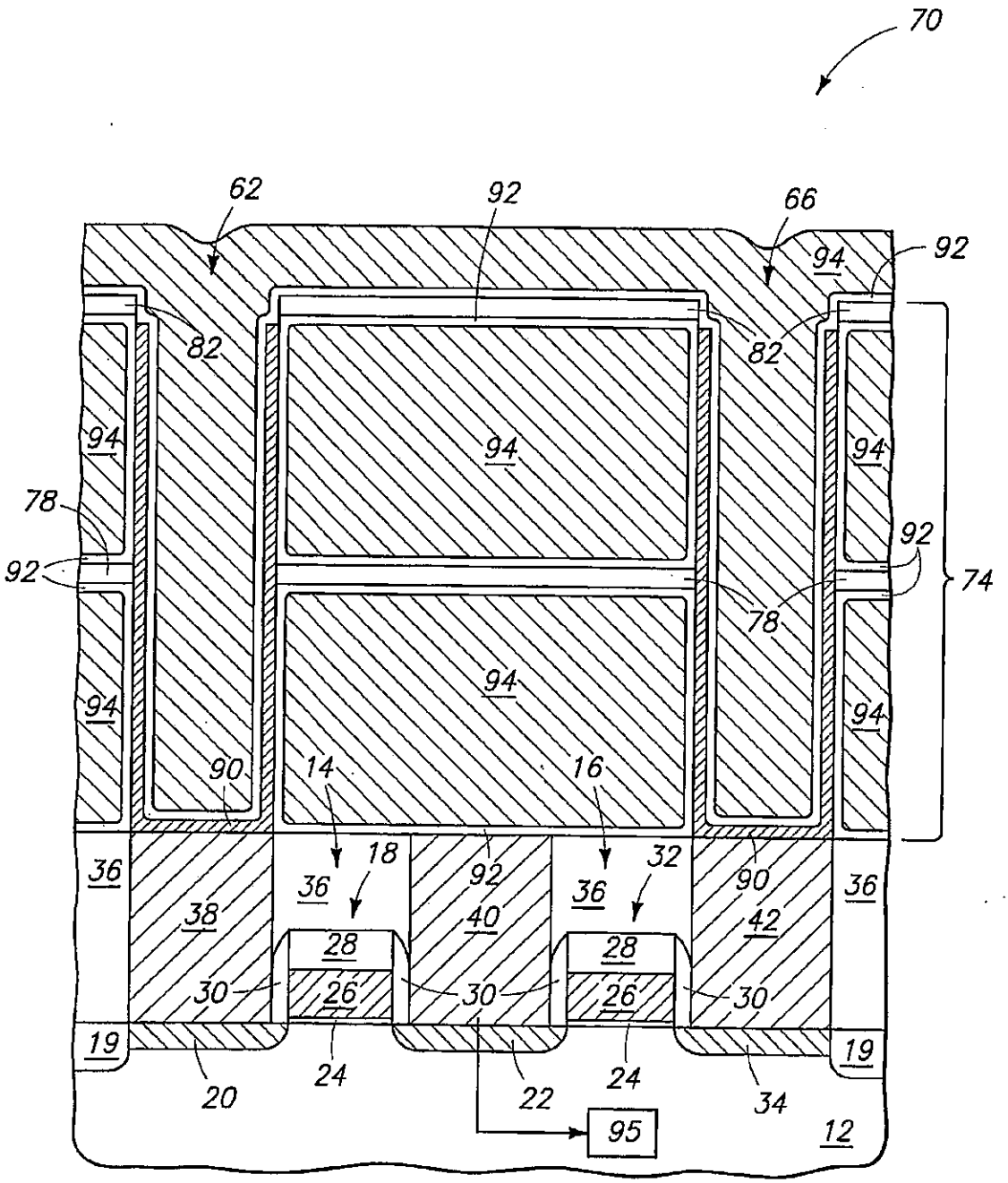

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Fig. 10

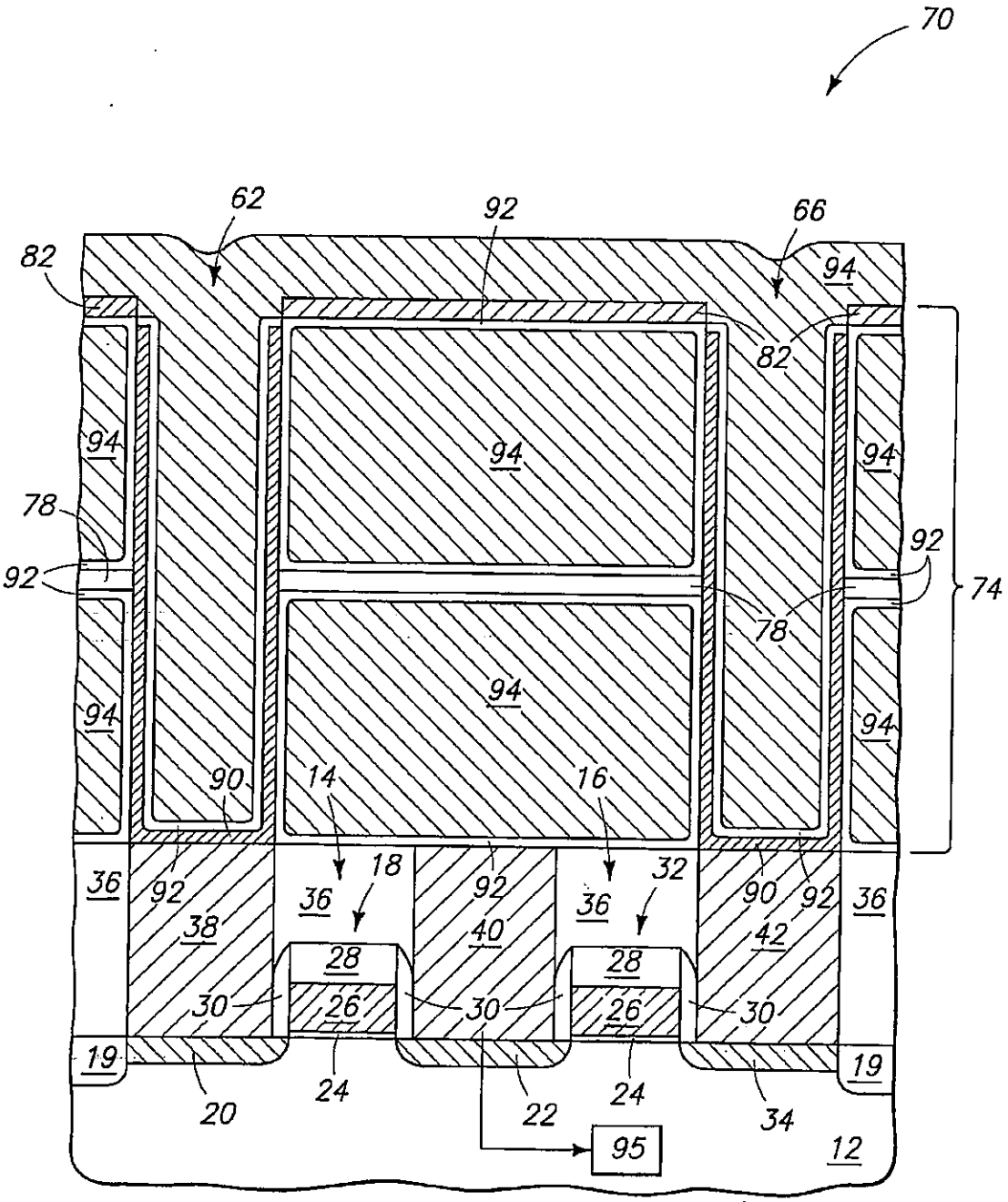

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Fig. 11

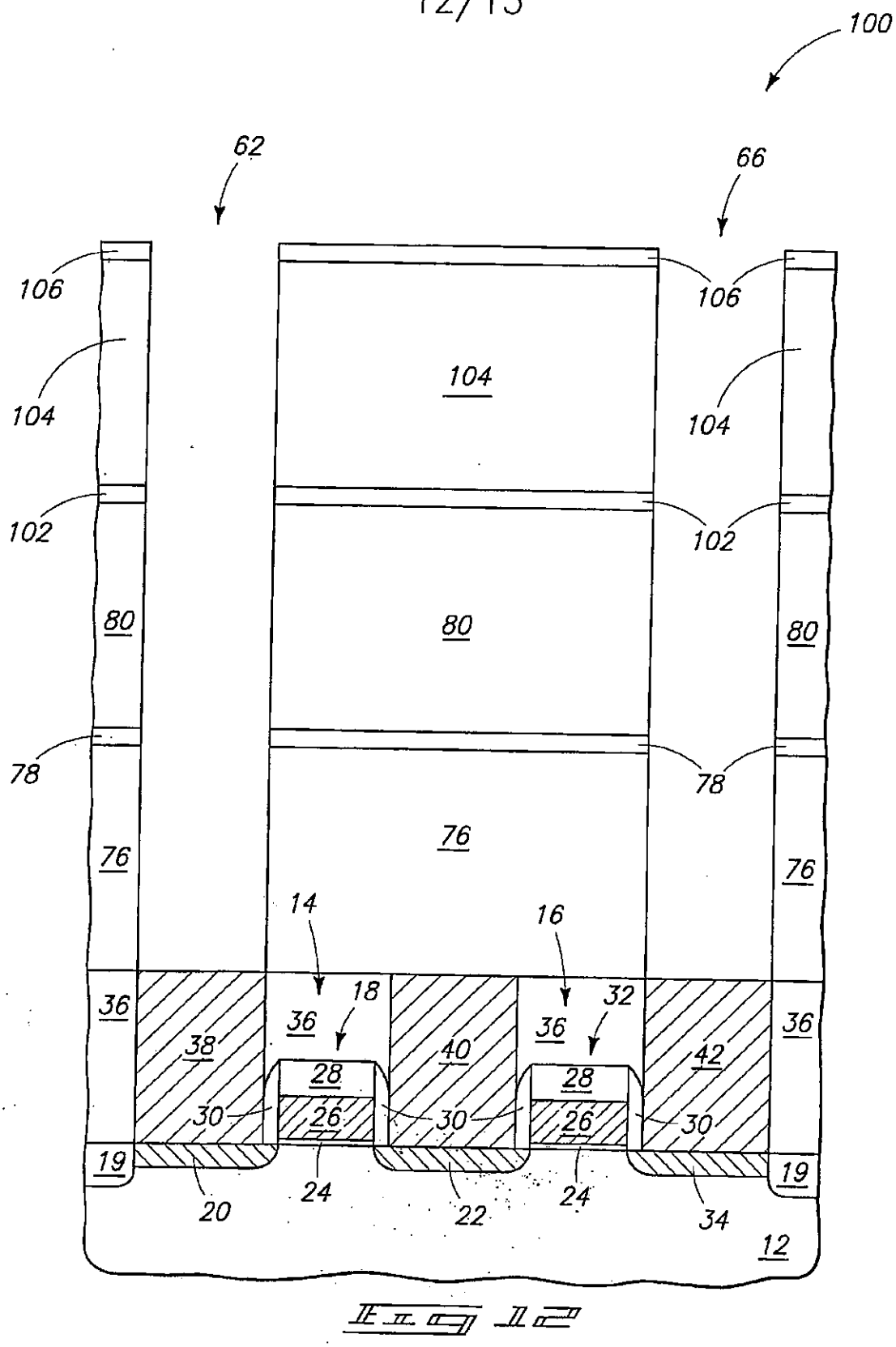

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Fig. 12

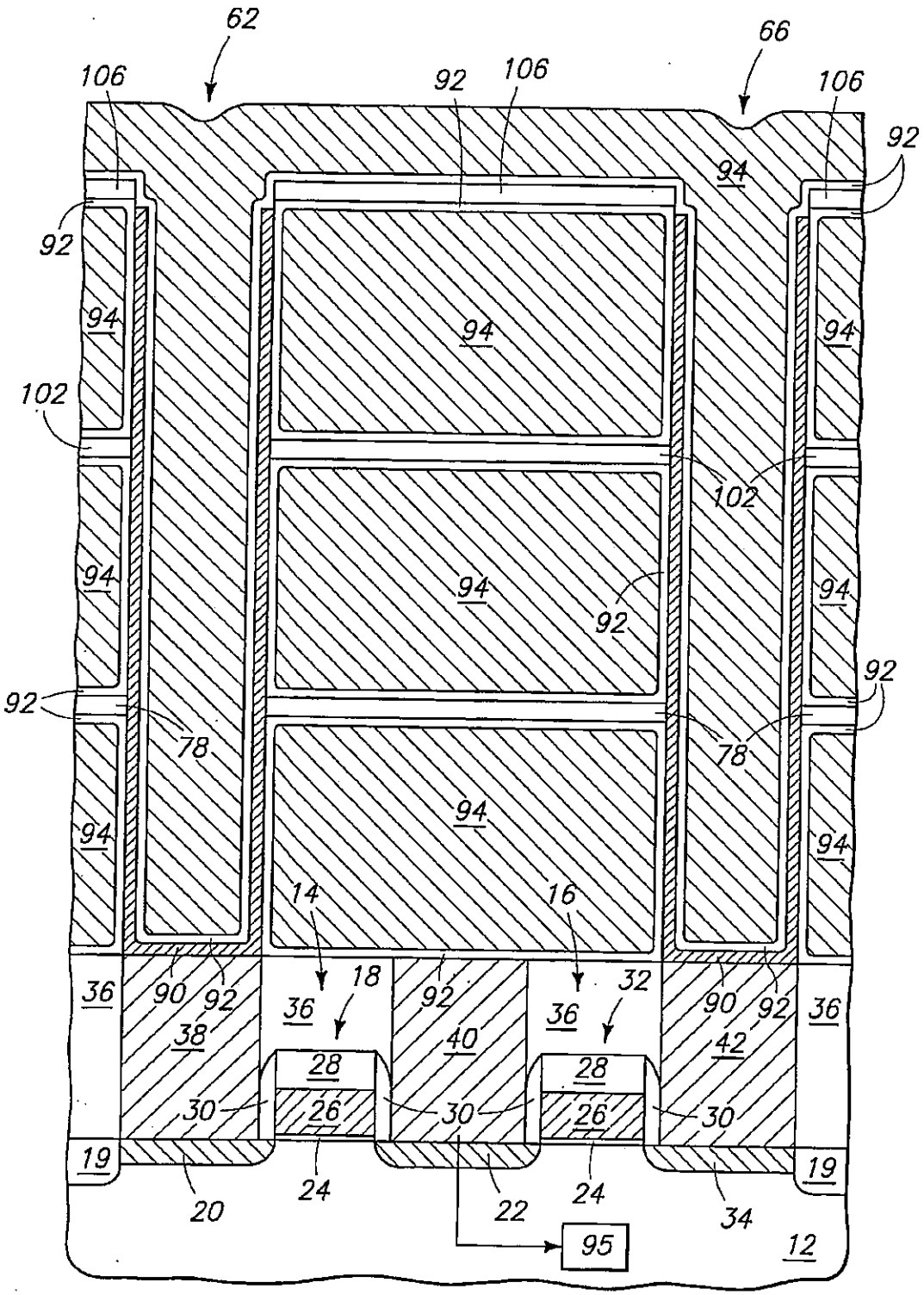

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Fig 13

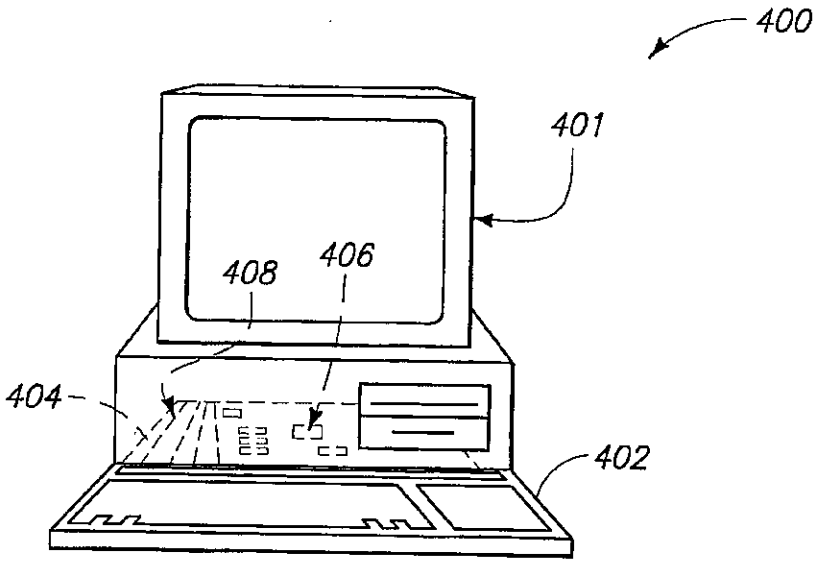


Fig 14

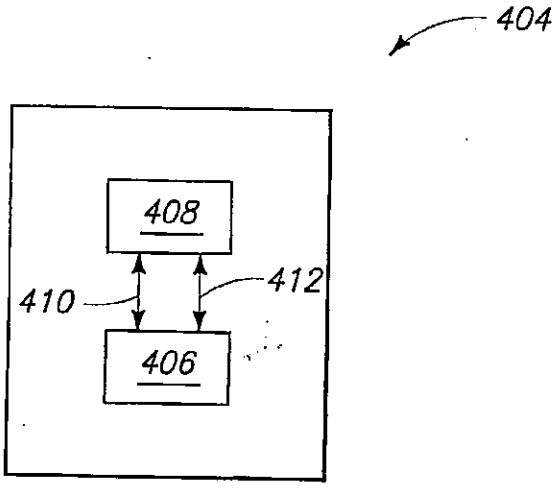


Fig 15

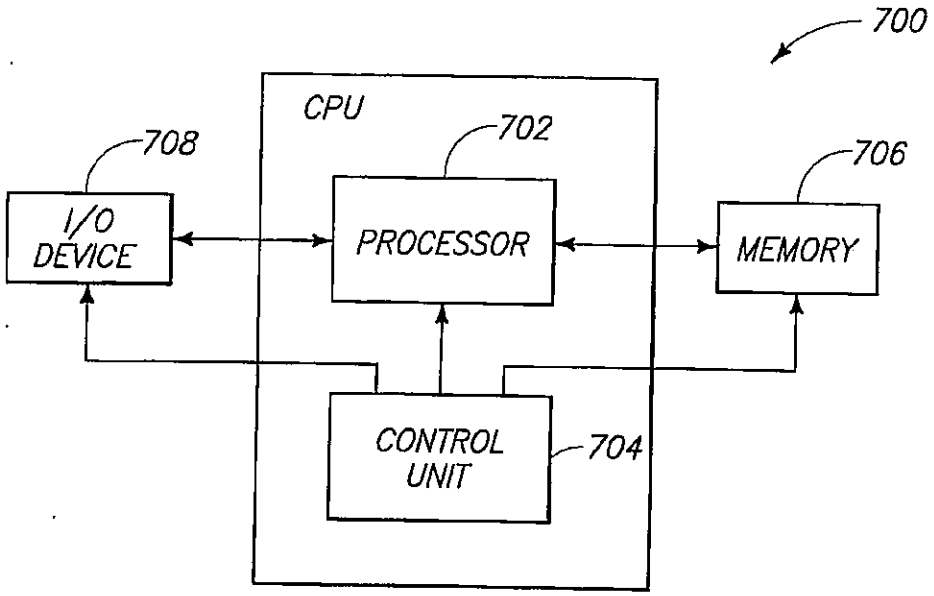

700
CPU
708
I/O DEVICE
702
PROCESSOR
706
MEMORY
CONTROL UNIT
704

Fig 16

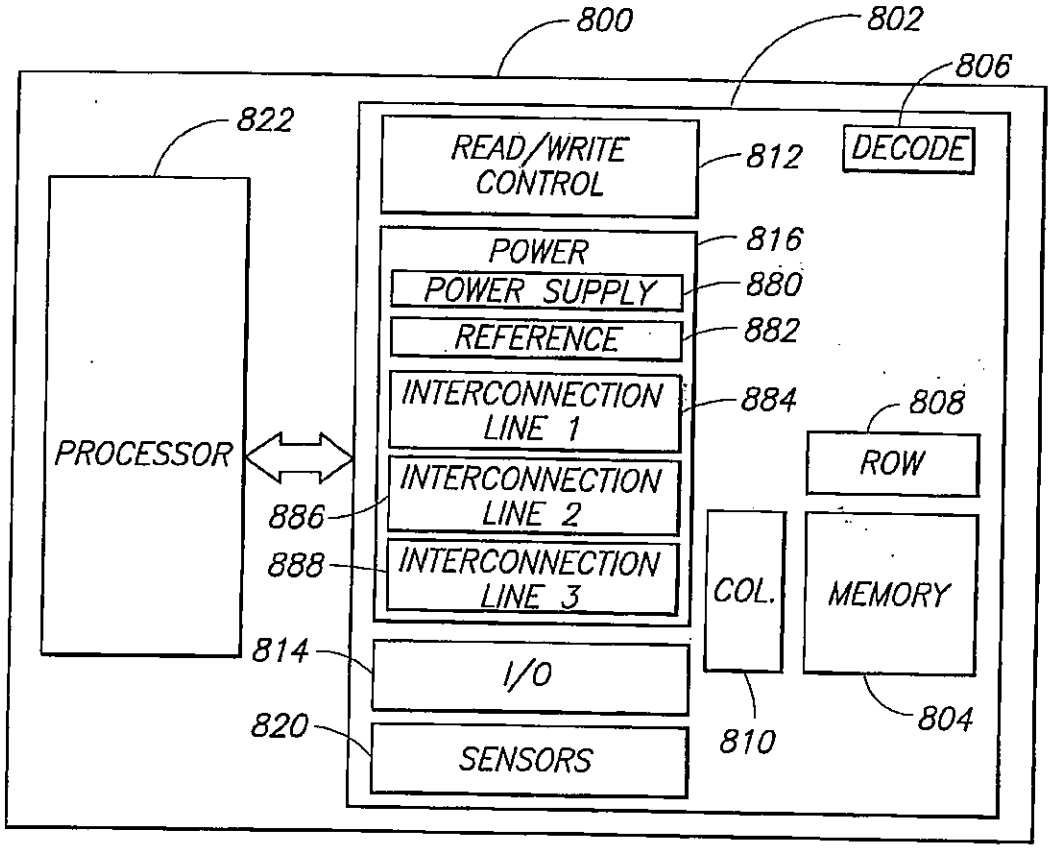

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READ/WRITE CONTROL
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DECODE
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POWER
POWER SUPPLY
880
REFERENCE
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INTERCONNECTION LINE 1
884
808
ROW
PROCESSOR
886
INTERCONNECTION LINE 2
888
INTERCONNECTION LINE 3
COL.
MEMORY
814
I/O
820
SENSORS
810
804

Fig 17