CHIP SIZE INTEGRATED CIRCUIT PACKAGE

ABSTRACT OF THE DISCLOSURE

An integrated circuit package (30) comprising a substrate (70) having an opening (86) and first and second surfaces(92, 94), a plurality of routing strips (82) being integral with the substrate (70) and extending to opening (86), a plurality of pads (100) disposed on the first surface (92) and electrically connected with at least one of the routing strips (82), a chip (50) having bonding pads (120) is adhered to the second surface (84) of the substrate (70) and is of substantially the same outline as substrate (70), wire bonding (80) electrically connecting at least one bonding pad (120) to at least one of the routing strips (82) and potting material (90) filling the opening (86) is disclosed.

Figure 1