CLAIMS

1. A method of forming a gate stack, the method comprising:

providing a plasma sputter chamber including a target comprising ruthenium and a pedestal for supporting a substrate to be sputter deposited in opposition to the target, the pedestal comprising a high current electrostatic chuck at a temperature greater than or equal to about 350° C.;

flowing krypton into the chamber and exciting the krypton into a plasma to deposit a ruthenium layer on the substrate; providing an anneal chamber; and annealing the ruthenium layer on the substrate at a temperature of about 900° C. for about 30 seconds in a N_2 environment.

2. The method of claim 1, wherein the electrostatic chuck is at a temperature in the range of about 450° C. to about 550° C.

3. The method of claim 1, wherein the electrostatic chuck comprises high resistivity ceramic.

4. The method of claim 1, wherein annealing the ruthenium layer comprises heating the ruthenium layer to about 500° C., increasing the temperature to about 900° C. at a rate greater than or equal to about 50° C./sec, holding the temperature for about 30 seconds and cooling the temperature at a rate equal to or greater than about 70° C./sec.

5. The method of claim 1, wherein the ruthenium layer has a thickness in the range of about 100 Å to about 300 Å.

6. The method of claim 1, wherein the ruthenium layer is deposited directly on a barrier layer without an interface layer.

7. The method of claim 6, wherein the barrier layer comprises one or more of TiN, TaN, WN or TiSiN.

8. The method of claim 7, wherein the barrier layer is formed on a silicide layer.

9. The method of claim 8, wherein the silicide layer comprises TiSi with a thickness of about 20 Å.

10. The method of claim 1, further comprising forming a spacer layer on sides of the ruthenium layer, the spacer layer comprising SiN.

11. The method of claim 10, wherein forming the spacer layer forms substantially no ruthenium nitride.

12. A method of forming a gate stack, the method comprising:

forming a polysilicon layer on a substrate;

forming a silicide layer on the polysilicon layer, the silicide layer comprising titanium silicide with a thickness of about 20 Å;

forming a barrier layer on the silicide layer, the barrier layer comprising one or more of TiN, TaN, WN or TiSiN;

optionally forming an interface layer on the barrier layer;

depositing a PVD Ru layer on the barrier layer or the optional interface layer, the PVD Ru layer deposited with the substrate on a high current electrostatic chuck comprising a high resistivity ceramic at a temperature greater than or equal to about 350° C. in a krypton environment, the PVD Ru layer having a thickness in the range of about 100 Å to about 300 Å;

annealing the PVD Ru layer at a temperature greater than or equal to about 500° C.; and

forming a spacer layer on sides of the annealed PVD Ru layer, the spacer layer comprising SiN and forming substantially no ruthenium nitride.

13. A method of forming a gate stack, the method comprising:

providing a plasma sputter chamber including a target comprising ruthenium and a pedestal for supporting a substrate with a barrier layer thereon to be sputter deposited in opposition to the target, the pedestal comprising a high current electrostatic chuck at a temperature greater than or equal to about 350° C., the barrier layer comprising one or more of TiN, TaN, WN or TiSiN, the barrier layer formed on a silicide layer, the silicide layer formed on a polysilicon layer, the polysilicon layer formed on a substrate;

flowing krypton into the chamber and exciting the krypton into a plasma to deposit a ruthenium layer on the barrier layer of the substrate without an interface layer;

providing an anneal chamber; and

annealing the ruthenium layer on the substrate at a temperature of about 900° C. for about 30 seconds in a N_2 environment.

14. The method of claim 13, wherein the electrostatic chuck is at a temperature in the range of about 450° C. to about 550° C.

15. The method of claim 13, wherein the electrostatic chuck comprises high

resistivity ceramic.

16. The method of claim 13, wherein annealing the ruthenium layer occurs at a temperature of about 900° C. for about 30 seconds in a N_2 environment.

17. The method of claim 13, wherein annealing the ruthenium layer comprises heating the ruthenium layer to about 500° C., increasing the temperature to about 900° C. at a rate greater than or equal to about 50° C./sec, holding the temperature for about 30 seconds and cooling the temperature at a rate equal to or greater than about 70° C./sec.

18. The method of claim 13, wherein the ruthenium layer has a thickness in the range of about 100 Å to about 300 Å.

19. The method of claim 13, wherein the silicide layer comprises TiSi with a thickness of about 20 Å.

20. The method of claim 13, further comprising forming a spacer layer on sides of the ruthenium layer, the spacer layer comprising SiN.