

1. A semiconductor device comprising:
 - a stacked transistor memory cell including:
 - a bottom tier including a plurality of bottom transistors including at least one non-floating transistor and at least one floating transistor, the at least one floating transistor having at least one terminal being electrically disconnected from other transistors of the stacked transistor memory cell;
 - a top tier including at least one top transistor; and
 - a cross-coupling including epitaxial region (epi) connections and gate to epi connections between the top tier and the bottom tier.
2. The device of claim 1, wherein:
 - the stacked transistor memory cell is a stacked vertical transistor memory cell;
 - the plurality of bottom transistors includes a plurality of bottom vertical transistors having a merged top source/drain epi, the plurality of bottom vertical transistors including first non-floating and floating transistors, and second non-floating and floating transistors; and
 - the plurality of top vertical transistors includes first, second, third and fourth top vertical transistors having a merged bottom source/drain epi.
3. The device of claim 2, wherein the cross-coupling includes:
 - epi connections by the merged top source/drain epi between the first non-floating and floating transistors, and the second non-floating and floating transistors;
 - epi connections by the merged bottom source/drain epi between the first and third top vertical transistors, and the second and fourth top vertical transistors;
 - gate to epi connections by metal between the first non-floating transistor and the second non-floating transistor, and the second non-floating transistor and the first floating transistor; and
 - gate to epi connections by metal between the first and second top vertical transistors, and the third and fourth top vertical transistors.
4. The device of claim 2, wherein the plurality of bottom vertical transistors include n-type field-effect transistors (nFETs) and the plurality of top vertical transistors include p-type field-effect transistors (pFETs).
5. The device of claim 2, wherein the plurality of bottom vertical transistors further includes respective bottom source/drain epis and the plurality of top vertical transistors further includes respective top source/drain epis.
6. The device of claim 5, further comprising dielectric layers separating the bottom source/drain epis and the top source/drain epis, and isolation layers separating the bottom tier and the top tier.

7. The device of claim 1, further comprising wordline, bitline, supply voltage and ground contacts.
8. The device of claim 1, wherein the cross-coupling further contacts gate structures of the bottom and top tiers.
9. A method for fabricating a semiconductor device, comprising:
forming a stacked transistor memory cell including a bottom tier having a plurality of bottom transistors including at least one non-floating transistor and at least one floating transistor and a top tier having at least one top transistor, the at least one floating transistor having at least one terminal being electrically disconnected from other transistors of the stacked vertical transistor memory cell, wherein forming the stacked transistor memory cell includes:
forming a cross-coupling including epitaxial region (epi) connections and gate to epi connections between the top tier and the bottom tier.
10. The method of claim 9, wherein:
the stacked transistor memory cell is a stacked vertical transistor memory cell;
the plurality of bottom transistors includes a plurality of bottom vertical transistors having a merged top source/drain epi, the plurality of bottom vertical transistors including first non-floating and floating transistors, and second non-floating and floating transistors; and
the plurality of top vertical transistors includes first, second, third and fourth top vertical transistors having a merged bottom source/drain epi.
11. The method of claim 10, wherein forming the cross-coupling further includes:
forming epi connections by the merged top source/drain epi between the first non-floating and floating transistors, and the second non-floating and floating transistors;
forming epi connections by the merged bottom source/drain epi between the first and third top vertical transistors, and the second and fourth top vertical transistors;
forming gate to epi connections by metal between the first non-floating and second floating transistors, and the second non-floating and first floating transistors; and
forming gate to epi connections by metal between the first and second top vertical transistors, and the third and fourth top vertical transistors.
12. The method of claim 10, wherein the plurality of bottom vertical transistors include n-type field-effect transistors (nFETs) and the plurality of top vertical transistors include p-type field-effect transistors (pFETs).
13. The method of claim 10, wherein the plurality of bottom vertical transistors further includes respective bottom source/drain epis and the plurality of top vertical transistors further includes respective top source/drain epis.

14. The method of claim 13, wherein the bottom source/drain epis and the top source/drain epis are separated by dielectric layer, and wherein the bottom tier and the top tier are separated by isolation layers.
15. The method of claim 9, wherein the stacked vertical transistor device further includes wordline, bitline, supply voltage and ground contacts.
16. The method of claim 9, wherein forming the cross-coupling further includes contacting gate structures of the bottom and top tiers.