CLAIMS

We claim:

1. A probe card assembly comprising:

a first substrate;

a plurality of resilient probes disposed on said substrate and arranged to contact corresponding pads of a device under test;

a tester interface;

a test circuit electrically coupled to said tester interface and electrically coupled to ones of said plurality of resilient probes;

a controller coupled to said test circuit, said controller comprising an interface;

a wireless transceiver coupled to said interface of said controller wherein said wireless transceiver can establish a wireless communications link with an external computer.

2. The probe card assembly of claim 1, wherein said interface of said controller is a boundary scan interface.

3. The probe card assembly of claim 2, wherein said boundary scan interface is a joint test access group (JTAG) compliant interface.

4. The probe card assembly of claim 3, wherein said wireless transceiver communicates JTAG commands and status across said wireless communications link.

5. The probe card assembly of claim 3, wherein said wireless transceiver translates commands received on said wireless communications link into a plurality of JTAG commands on said boundary scan interface.

6. The probe card assembly of claim 1, further comprising a second substrate coupled to said first substrate, wherein said test circuit and said controller are disposed on said second substrate.

7. The probe card assembly of claim 6, further comprising a daughter card coupled to said second substrate, wherein said wireless transceiver is disposed on said daughter card.

8. The probe card assembly of claim 1, wherein said test circuit comprises a means for providing test resource enhancement.

9. The probe card assembly of claim 1, wherein said test circuit comprises a means for providing power supply expansion.

10. The probe card assembly of claim 1, wherein said controller controls operation of said probe card assembly based on commands received via said wireless communications link.

11. The probe card assembly of claim 1, wherein said external computer is a verifier.

12. A wireless verification attachment for a probe card assembly comprising:

a substrate sized to fit within a space between a test head and a probe card assembly when said probe card assembly is installed into a prober;

an electrical connector disposed on said substrate and positioned to mechanically and electrically connect to an electrical interface disposed on said probe card assembly; and

a wireless transceiver coupled to said electrical interface and capable of establishing a wireless communications link with an external computer.

13. The wireless verification attachment of claim 12, wherein said electrical interface is a boundary scan interface.

14. The wireless verification attachment of claim 13, wherein said boundary scan interface comprises a joint test access group (JTAG) compliant interface.

15. The wireless verification attachment of claim 14, wherein said wireless transceiver replicates JTAG signals of said external computer at said electrical connector using information transferred across said wireless communications link.

16. The wireless verification attachment of claim 14, further comprising a controller electrically coupled to said wireless transceiver and said electrical connector, wherein said controller generates JTAG signals at said electrical connector using information transferred across said wireless communications link.

CLAIMS

1. A probe card assembly comprising:

a first substrate;

a plurality of resilient probes disposed on said first substrate and arranged to contact corresponding pads of a device under test (DUT);

a tester interface configured to provide a communications link with a tester for controlling testing of said DUT;

a controller coupled to said tester interface and comprising a debugger interface to a debugger for debugging said probe card assembly, wherein said debugger is a distinct and different piece of equipment than said tester and said debugger interface is a distinct and different interface than said tester interface; and

a wireless transceiver configured to establish a wireless communications link between said debugger interface and said debugger, wherein said wireless communications link is a distinct and different communications link than said communications link to said tester.

2. The probe card assembly of claim 1, wherein said debugger interface is a boundary scan interface.

3. The probe card assembly of claim 2, wherein said boundary scan interface is a joint test access group (JTAG) compliant interface.

4. The probe card assembly of claim 3, wherein said wireless transceiver communicates JTAG commands and status across said wireless communications link.

5. The probe card assembly of claim 3, wherein said wireless transceiver translates commands received on said wireless communications link into a plurality of JTAG commands on said boundary scan interface.

6. The probe card assembly of claim 1, further comprising a second substrate coupled to said first substrate, wherein said tester interface is disposed on said second substrate.

7. The probe card assembly of claim 6, further comprising a daughter card coupled to said second substrate, wherein said wireless transceiver is disposed on said daughter card.

8. The probe card assembly of claim 1 further comprising a test circuit electrically coupled to

said tester interface and electrically coupled to ones of said probes, wherein said test circuit comprises a means for providing test resource enhancement.

9. The probe card assembly of claim 1 further comprising a test circuit electrically coupled to said tester interface and electrically coupled to ones of said probes, wherein said test circuit comprises a means for providing power supply expansion.

10. The probe card assembly of claim 1, wherein said controller controls operation of said probe card assembly based on commands received via said wireless communications link.

11. The probe card assembly of claim 1, wherein said debugger is a verifier.

12. A wireless verification attachment for a probe card assembly comprising:

a substrate sized to fit within a space between a test head and a probe card assembly when said probe card assembly is installed into a prober;

an electrical connector disposed on said substrate and positioned to mechanically and electrically connect to a tester interface disposed on said probe card assembly and configured to provide a communications link with a tester for controlling testing of a device under test (DUT); and

a wireless transceiver comprising a debugger interface and capable of establishing a wireless communications link with a debugger for debugging said probe card assembly,

wherein:

said debugger is a distinct and different piece of equipment than said tester,

said debugger interface is a distinct and different interface than said tester interface, and

said wireless communications link is a distinct and different communications link than said communications link to said tester.

13. The wireless verification attachment of claim 12, wherein said debugger interface is a boundary scan interface.

14. The wireless verification attachment of claim 13, wherein said boundary scan interface comprises a joint test access group (JTAG) compliant interface.

15. The wireless verification attachment of claim 14, wherein said wireless transceiver replicates JTAG signals of said debugger at said electrical connector using information transferred across said wireless communications link.

16. The wireless verification attachment of claim 14, further comprising a controller electrically coupled to said wireless transceiver and said electrical connector, wherein said controller generates JTAG signals at said electrical connector using information transferred across said wireless communications link.

17. The wireless verification attachment of claim 16, wherein said controller translates commands received across said wireless communications link into a plurality of JTAG commands at said electrical connector.

18. The wireless verification attachment of claim 12, wherein said debugger is a verifier.

19. A method of probe card verification comprising:

obtaining a probe card assembly, wherein said probe card assembly comprises:

a tester interface for providing a communications link with a tester for controlling testing of a device under test (DUT),

a controller electrically coupled to said tester interface wherein said controller controls operation of said probe card assembly, said controller comprising a debugger interface to a debugger configured to debug said probe card assembly, said debugger interface is a distinct and different interface than said tester interface,

a wireless transceiver electrically coupled to said debugger interface, and

a plurality of resilient probes arranged to contact corresponding pads on said DUT and coupled to said controller;

installing said probe card assembly in a prober with said tester interface connected to a test head of said prober;

establishing with said wireless transceiver a wireless communications link between said debugger interface and said debugger, wherein said debugger is positioned outside of said prober, said debugger is a distinct and different piece of equipment than said tester, and said wireless communications link is a distinct and different link than any communications link from said tester interface to said tester; and

using said wireless communications link to communicate commands from said debugger to said controller while said probe card assembly is installed in said prober and connected to said test head; and

using said wireless communications link to communicate status from said controller to said debugger while said probe card assembly is installed in said prober and connected to said test head.

20. The method of claim 19, wherein said debugger interface is a boundary scan interface.

21. The method of claim 20, wherein said commands and said status correspond to joint test access group (JTAG) compliant signals replicated at said boundary scan interface.

22. The method of claim 21, wherein said wireless transceiver converts JTAG compliant signals at said boundary scan interface and the commands and status communicated across said wireless communications link.

23. The method of claim 19, wherein said status comprises a state of at least one signal at said tester interface.

24. The method of claim 19, wherein said status comprises a state of at least one signal at said resilient probes.

25. The method of claim 19, wherein said commands comprise setting a state of at least one signal at said tester interface.

26. The method of claim 19, wherein said commands comprise setting a state of at least one signal at said resilient probes.

27. The method of claim 19, wherein said debugger provides a display corresponding to at least one signal within said probe card assembly.

28. The method of claim 19, wherein said obtaining comprises installing a daughter card comprising said wireless transceiver onto a probe card base comprising said controller.

29. The method of claim 19, wherein said debugger is a verifier.