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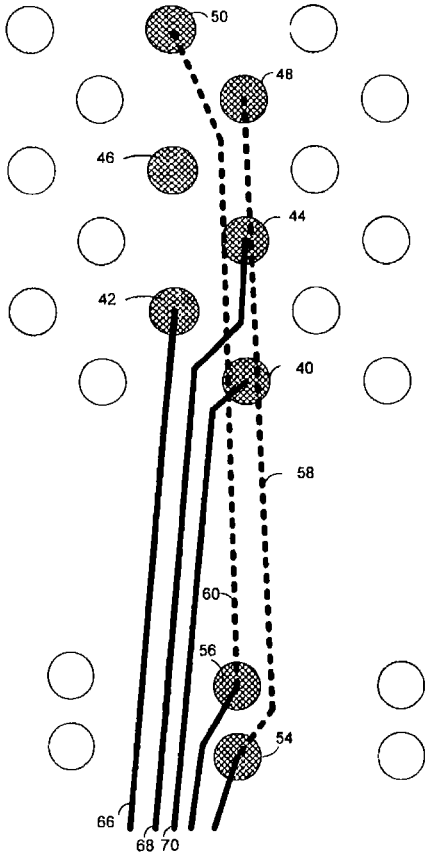
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(54) Title: HIGH-DENSITY FLIP-CHIP INTERCONNECT



(57) Abstract: An interconnect routing for a card or interposer or the like, including splines of traces on a first layer (66, 69, 70) and traces on a second layer (58, 60), with vias connecting between the layers. Outer rows of signals (40, 42, 44) are routed out from a chip on the first layer, while inner rows of signals (48, 50) are viad down to the second layer where they are routed out, then viad back up to the first layer. These outer vias are arranged in an arc, enabling the second layer trace segments to be of a more uniform length. The second layer may also include ground or power plane fingers extending between the splines and viad up to ground or power signals of the chip.

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