FORMATION AND TREATMENT OF A SiGe STRUCTURE

Embodiments of the present invention relate to a method of forming a structure comprising a removed layer of semiconductor material taken from a donor wafer, the donor wafer comprising, prior to removal, a first layer formed of $Si_{1-x}Ge_x$ and a second layer of $Si_{1-y}Ge_y$ on the first layer (x, y respectively being in the range 0 to 1, and x being different from y), the method comprising the following steps in succession:

a) implanting atomic species to form a zone of weakness beneath the second layer;

b) bonding the donor wafer to a receiver wafer;

c) supplying thermal and/or mechanical energy to detach the removed layer from the donor wafer at the zone of weakness;

d) treating the removed layer.

That type of layer removal uses the Smart-Cut® technique which is well known to the skilled person. One example of employing such a removal method is described in United States document US2004/0053477 in which the crystallographic structure of the second layer is elastically strained by the structure of the first layer.

Step d) for treating the removed layers often has to be carried out to lift off defective zones and to reduce surface roughness principally resulting from carrying out steps a) and c). The thickness of the defective zone is typically about 150 nanometers (nm) for hydrogen atomic implantation.

As an example, it is possible to perform mechanical polishing or chemical-mechanical planarization (CMP, chemical mechanical polishing) in order to eliminate surface roughness, and/or steps of sacrificially oxidizing defective zones.

Since bonding in accordance with step b) is conventionally carried out via a layer of electrically insulating material, a semiconductor-on-insulator

structure can thus be produced, such as a $Si_{1-x}Ge_x/Si_{1-y}Ge_y$ on insulator structure.

As disclosed in US2004/0053477, a step subsequent to step d) can be carried out to lift off the remaining portion of the first layer, hence retaining only the second layer on the receiver wafer. Thus, a $Si_{1-y}Ge_y$ on insulator structure can be produced.

The operation for lifting off the remaining portion of the first layer can be carried out effectively by selective chemical etching using suitable etching agents. Selective chemical etching can in the end produce the desired layer with a good surface quality without too great a risk of damaging it (which could be the case if only a single polish were to be carried out).

However, selective chemical etching necessitates prior preparation of the etching surface, typically carried out using mechanical polishing means. That preparation for etching remains necessary to reduce the severe roughness which could subsequently cause locally over-inhomogenous etching, which could create through defects or holes in the second layer.

However, the successive actions of polishing and chemical etching render the post-detachment finishing step (as well as the whole of the removal procedure) long, complex, and economically expensive.

Furthermore, chemical etching can in some cases result in problems with at least partial unbonding of the bonding interface. In particular, it may delaminate the side of the bonding layer, i.e. attack the layer where it crops out from the side of the resulting structure. An example that can be mentioned is HF treatment of a sSOI (strained silicon on insulator) structure comprising SiO_2 buried under strained Si, or H_2O_2:HF:HAc treatment (HAc being the abbreviation for acetic acid) on a sSi/SiGeOI (strained silicon on SiGe on insulator) structure, where the layers of SiGe and buried SiO_2 are liable to be etched beneath the layer of strained Si.

Thus as regards the quality of the final product, the results obtained are less than satisfactory.

One alternative which could be envisaged to overcome that problem would be to dilute the etching agents further to enable their action to be better controlled. However, that solution is not satisfactory since by substantially increasing the duration of the procedure, it does not completely solve the problem of delamination.

A further solution which could be envisaged would be to reinforce the bonding interface prior to etching to render that interface more resistant to chemical agents. To this end, a post-detachment stabilizing heat treatment carried out at about 1000°C or more for several hours could be envisaged.

However, that solution, which is well known when producing a SOI (silicon on insulator) structure, is not suitable when transferring heterogeneous layers of $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$. In fact, such a heat treatment causes Ge to diffuse from the layer having the highest Ge content towards the layer having the lowest Ge content, thus tending to homogenize the Ge content over the two layers and thus the physical and electrical properties of those two layers can no longer be differentiated.

If the two layers become essentially identical, then subsequent etching can no longer be selective.

Further, it is frequently desirable to avoid any diffusion from one layer to another. This is particularly the case when the second layer is formed of strained Si (i.e. $y=0$) and if a final sSOI structure is to be obtained to fully benefit from the electrical properties of said structure (i.e. increased charge mobility).

Thus, the treatment temperature is limited by the diffusion of Ge from one layer to the other (said diffusion typically commencing at about 800°C), and low temperature reinforcement can thus only be partial. Thus, the delamination problem subsists.

Embodiments of the invention seek to avoid delamination at the side of the bonding layer when carrying out finishing chemical etching.

Embodiments of the invention further seek to reduce the duration, economic cost, and number of treatments after step c) carried out on the removed layers, and in particular to dispense with the use of mechanical polishing.

Embodiments of the invention further seek to produce a structure such as a semiconductor-on-insulator structure comprising a removed layer including a material which is less stable than Si, such as strained Si or SiGe.

Embodiments of the invention further seek to reduce the quantity of material sacrificed during treating the removed layer.

Embodiments of the invention further seek to propose a simple method of treating the removed layer which readily integrates into the whole removal method employing the Smart-Cut® technique.

A first aspect of the present invention provides a method for forming a semiconductor structure, which comprises: providing a donor wafer that includes a first layer of $Si_{1-x}Ge_x$ and a second layer of $Si_{1-y}Ge_y$ located on the first layer, with x and y respectively, being in the range of 0 to 1, and x being different than y; implanting atomic species into the donor wafer to form a zone of weakness in the first layer; bonding the donor wafer to a receiver wafer; detaching the second layer and a portion of the first layer from the donor wafer by supplying energy to bonded wafers sufficient to cause cleavage at the zone of weakness to form an intermediate structure thereof; conducting a rapid thermal anneal of the intermediate structure at a temperature of about 1000°C or

more for a period of time not exceeding 5 minutes; and removing any remaining portions of the first layer of the intermediate structure to provide a semiconductor structure comprising the second layer on the receiving wafer.

Other possible characteristics of some example embodiments of the invention are as follows:

- Thermal anneal may be carried out at a temperature in the range from about 1000°C to about 1200°C for about 10 seconds to about 30 seconds;
- Thermal anneal may be carried out at a temperature of about 1100°C for about 10 seconds;
- Thermal anneal may be carried out in a reducing atmosphere;
- Thermal anneal may be carried out in a reducing atmosphere of argon and hydrogen or in a reducing atmosphere of argon;
- sacrificial oxidation of a portion of the first layer may be carried out between detaching the second layer and conducting the rapid thermal anneal;
- plasma activation of at least one bonding surface may be carried out prior to the bonding step;
- a heat treatment of more than about 30 minutes to reinforce the bonding may also be carried out after the bonding step;
- the atomic species implanted during the implanting step may be constituted by a single atomic element;
- the atomic species implanted during the implanting step may comprise two distinct atomic elements, the implanting step thereby constituting co-implantation;
- after the detaching step, the method may not include carrying out mechanical polishing;

- after the final step, the method may further comprise crystal growth of $Si_{1-y}Ge_y$ on the second layer to thicken said second layer;
- the second layer may be formed of elastically strained $Si_{1-y}Ge_y$;
- the donor wafer may further comprise a third layer of $Si_{1-x}Ge_x$ on the second layer;

- the donor wafer may comprise a support substrate formed of bulk Si, a SiGe buffer structure and a multilayer structure comprising first layers of $Si_{1-x}Ge_x$ alternating with the second layers of strained $Si_{1-y}Ge_y$ layers to enable a plurality of removals to be made from the same donor wafer;
- each layer of strained $Si_{1-y}Ge_y$ may be thicker than the critical equilibrium thickness;
- prior to the bonding step, the method may further comprise a step of forming a bonding layer on the donor wafer and/or on the receiver wafer, the bonding layer comprising an electrically insulating material such as SiO_2, Si_3N_4, or $Si_xO_yN_z$, for example.

Further characteristics, aims, and advantages of the invention become apparent from the following detailed description of preferred implementations of the method, given by way of non limiting example, and made with reference to the accompanying drawings in which:

Figures 1a to 1f are diagrams of the different steps of a method in accordance with the invention to form a structure comprising a layer removed by Smart-Cut®.

Figures 2a and 2b are diagrams of a first variation of the invention.

Figures 3a and 3b are diagrams of a second variation of the invention.

Figure 4 shows the results of measurements carried out by secondary ion mass spectrometry to determine the concentration of germanium in a layer of strained silicon taken off in accordance with the invention, compared with concentrations of germanium in Si (unstrained) calculated from diffusion constants taken from the literature.

Figure 5 shows a comparative study of the germanium diffusion coefficients in a layer of unstrained silicon and in a layer of strained silicon.

There follow examples of methods of the invention and uses of the invention, based on layers removed by Smart-Cut® formed of a type IV material or alloy, in particular Si and SiGe.

Figures 1a to 1e show a first method of removing a first layer 1 formed of $Si_{1-x}Ge_x$ (in which $x \in [0;1]$) and a second layer 2 formed of $Si_{1-y}Ge_y$ (in which $y \in [0;1]$ and $y \neq x$), from a donor wafer 10, to transfer them to a receiver wafer 20, in accordance with the invention.

Figure 1a shows a donor wafer 10 comprising the first layer 1 formed of $Si_{1-x}Ge_x$ and the second layer 2 formed of $Si_{1-y}Ge_y$ to be removed.

As is conventional, the donor wafer 10 including $Si_{1-x}Ge_x$ comprises a bulk substrate 5 formed of Si on which there has been formed, for example by crystal growth, a buffer structure formed of SiGe (not shown) composed of different layers. In particular, this buffer structure may have a gradual change in its Ge content from 0% at the bulk Si substrate to about 100 x % at the interface with the first layer 1 formed of $Si_{1-x}Ge_x$ (it too is preferably formed by crystal growth). The selected thickness of the $Si_{1-x}Ge_x$ layer can be about 1 micrometer, for example.

A second layer of $Si_{1-y}Ge_y$ is formed on the first layer 1 formed of $Si_{1-x}Ge_x$. In a first case, the second layer is grown in situ, continuing on directly from the formation of the first layer 1. In a second case, the second layer 2 is grown after a brief step of preparing the surface of the first layer 1, for example by CMP polishing.

The second layer 2 is advantageously formed by epitaxial growth using known techniques such as CVD and MBE (chemical vapor deposition and molecular beam epitaxy). Thus, for a first layer 1 formed of $Si_{0.8}Ge_{0.2}$

and a second layer 2 formed of strained Si (i.e. y = 0), a second layer having a thickness in the range from about 100 Angströms (Å) to about 800 Å can be formed.

Given that the concentration of silicon in the two layers 1 and 2 is different, the second layer 2 is thus strained by the first layer 1 to render its lattice parameter substantially identical to that of its growth substrate, thus giving it internal elastic strains. Said internal strains are tensile if the amount of silicon in the alloy of the second layer 2 is greater than that of the first layer 1 and compressive in the opposite case. A fairly thin second layer 2 has to be formed: too thick a layer, above a critical equilibrium thickness, could cause relaxation of the strain in the thickness of that film towards the nominal lattice parameter of $Si_{1-y}Ge_y$ and/or could cause defects to be generated. Reference should be made to the document entitled "High mobility Si and Ge structures" by Friedrich Schäffler (Semiconductor Science Technology, 12 (1997) 1515-1549) for more details regarding this subject.

However, in the particular case of depositing a strained material at a sufficiently low temperature, it may become possible to form said second strained layer 2 with a thickness that is greater than the critical equilibrium thickness (discussed below).

Referring now to Figure 1b, a zone of weakness 4 is then formed in the donor wafer 10 beneath the second layer 2. In particular, said implantation can be made in the first layer 1 of $Si_{1-x}Ge_x$ (as shown in Figure 1b).

This zone of weakness 4 is formed by implanting atomic species the dose, nature, and energy of which are selected to determine an implantation depth and a degree of weakness. In particular, the implantation energy is determined so that the zone of weakness is formed beneath the second layer 2. For a first layer 1 with a thickness of about 0.5 micrometers or more and a second layer 2 with a thickness in the range from about 100 Å to about

800 Å, for example about 200 Å, said zone of weakness 4 can be formed between about 1500 Å and about 3000 Å, more particularly at about 2000 Å.

As an example, it is possible to implant hydrogen species at an energy in the range 20 kiloelectron volts (keV) to 80 kV and at a dose in the range 3×10^{16} atoms per square centimeter (atoms/cm^2) to 10×10^{16} atoms/cm^2, more particularly at an energy of about 30 keV and at a dose of about 6×10^{16} atoms/cm^2). An implantation depth of the order of 1000 Å to 5000 Å is thus obtained.

Optionally, the parameters determining the implanting atomic species are adjusted to minimize the roughness appearing at the zone of weakness 4 after detachment. In fact, the degree of post-detachment roughness is partially linked to these parameters. Thus, it is possible to select co-implanting atomic species, such as co-implantation of hydrogen and helium or argon or another inert gas. In the case of co-implantation, it has been noticed that the zone of weakness 4 is often thinner than in the case of simple implantation (see in particular FR 04/09980 for more details).

In the case of co-implantation with helium at about $1 \times 10^{16}/cm^2$ and at an energy in the range 20 keV to 80 keV and hydrogen at $1 \times 10^{16}/cm^2$ and at an energy in the range 20 keV to 80 keV, it is possible to obtain an implantation depth of the order of 1000 Å to 5000 Å.

Referring to Figure 1c, a step of bonding a receiver wafer 20 with the face of the donor wafer 10 that has undergone implantation is carried out.

The receiver wafer 20 may be produced from bulk Si or from other materials.

Prior to the bonding step, a bonding layer may be formed, such as a layer comprising SiO_2, Si_3N_4, $Si_xO_yN_z$, on one and/or the other of the respective surfaces to be bonded. The technique used to form said bonding layer may be deposition, in order to avoid any deterioration of the

strains in the second layer 2 or any consequent diffusion in the first layer 1.

Prior to bringing the receiver wafer 20 into contact with the donor wafer 10, at least one of the surfaces to be bonded can optionally be prepared using known techniques for surface cleaning and preparing, such as SC1 and SC2 solutions, ozone-containing solutions, or others.

Bonding per se may be carried out in the first place by molecular bonding, taking into account the hydrophilic nature of each of the two surfaces to be bonded.

It is also possible to carry out plasma activation of one or both bonding surfaces just prior to carrying out bonding, which principally allows the future bonding interface to be reinforced without carrying out high temperature heat treatment. In particular, plasma activation can be carried out so that in the end, after bonding and after removal, the bonding energy is about 0.8 joules per square meter (J/m^2) or more. The plasma can, for example, be obtained from an inert gas such as Ar or N_2 or from an oxidizing gas such as O_2.

Optionally, a low temperature annealing heat treatment (800°C or less) may be carried out prior to bonding, to further reinforce the bonding interface.

Figure 1d shows detachment of the removed layers at the zone of weakness 4 by supplying thermal and/or mechanical energy sufficient to break the weak bonds at the zone of weakness 4 and thereby to detach the donor wafer 10 into a first portion 10′ comprising a remainder of the first layer 1″ and into a second portion 30 comprising the other portion of the first layer 1′ and the second layer 2. Said thermal energy may then be sufficient to cause, at the zone of weakness 4, thermal effects on the gaseous species which are enclosed therein, causing rupture of weak bonds.

Detachment may be carried out at temperatures in the range from about 300°C to about 600°C for a longer or

shorter time period, depending respectively on whether the temperature is low or high.

As an example, for a layer to be removed formed of $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$, it is possible to carry out heat treatment at a temperature of about 500°C to about 600°C for a period of 15 minutes to 30 minutes up to 2 hours, more particularly at about 600°C.

When detachment is carried out solely by heat treatment, detachment may occur without necessarily withdrawing contact with the remaining portion of the donor wafer 10'.

In this case, and optionally, a new heat treatment may be carried out following detachment, without removing the wafers from the furnace (in which the detachment heat treatment has been carried out) and without carrying out additional operations which would take more time and would necessitate using appropriate equipment. Further, the remaining portion of the donor wafer 10' protects the removed first and second layers 1' and 2 against possible contaminants, oxidants, or other species, which offers the possibility of carrying out the new heat treatment in different atmospheres.

Heat treatment can also clearly be carried out after the wafers have been physically separated (and removed from the detachment furnace). Said heat treatment can be carried out in addition to, or instead of, any plasma activation carried out prior to bonding. In all cases, the heat treatment for reinforcing the bonding interface 6 is carried out at a temperature in the range from about 350°C to about 800°C, in particular in the range from about 350°C to about 700°C, more particularly at about 600°C, maintained for about 30 minutes to about 4 hours, and is carried out so as to reinforce bonding sufficiently (and thus avoid the risk of delaminating the side during the selective etching to be carried out following removal).

In accordance with the invention, following detachment, with or without the preceding step of reinforcing the bonding interface, rapid thermal annealing (RTA) is then carried out at a temperature of 1000°C or more, for a period that does not exceed about 5 minutes.

Said RTA is preferably carried out in a reducing atmosphere, such as an atmosphere of argon and hydrogen or argon alone.

As an example, said RTA may be carried out between about 1000°C and about 1200°C for about 10 seconds to about 30 seconds, in particular at about 1100°C for about 10 seconds.

Said temperature of 1000°C or more is a temperature which is not conventionally used when in the presence of two layers 1 and 2 having different Ge concentrations. In fact, it has been recognized (see, for example, the document by M Griglione et al entitled "Diffusion of Ge in $Si_{1-x}Ge_x/Si$ single quantum wells in inert and oxidizing ambients" (Journal of Applied Physics, vol 88, n° 3, August 1st, 2000) that heat treatments carried out at temperatures which would cause diffusion of Ge from the layer with the highest Ge concentration to the layer with the lowest concentration would tend to homogenize the Ge content over the two layers and thus the physical and electrical properties of the two layers would no longer be distinguished. Said diffusion is undesirable in the context of the invention, as well as in the majority of conventional methods, in particular because differentiation of the layers 1' and 2 will allow subsequent selective etching of the first layer 1' as opposed to the second layer 2 to be carried out. For this reason, known methods, as described above, have been carried out using techniques that remain below 1000°C, and more particularly below 800°C (see in particular FR 04/09980).

However, the Applicant has carried out a series of studies on $Si_{1-x}Ge_x$/ strained $Si_{1-y}Ge_y/SiO_2$/bulk Si wafer structures obtained just after detachment, showing that the diffusion of Ge during treatment at 800°C or more is not as marked as was proposed earlier. In particular, the Applicant has demonstrated that RTA as described above can thus be carried out without substantial diffusion between the first layer 1' and the second layer 2.

Figure 4 shows a series of results obtained by the Applicant.

The measurements were carried out on structures 30 each similar to the structure 30 shown in Figure 1e, obtained after detaching removed layers 1' and 2. In the context of this study, the first layer 1' was formed of 20% germanium (i.e. $x = 0.2$) and was about 200 Å thick, and the second layer 2 was formed of strained silicon (i.e. $y = 0$) and was about 200 Å thick.

The abscissa of the graph of Figure 4 shows the probed depth in the test samples from the free surface of the first layer 1'.

Figure 4 is divided into a left hand portion 1' representing the first layer 1' and a right hand portion 2 representing the second layer 2 separated by a vertical line 12 representing the interface between the first layer 1' and the second layer 2.

The "y" axis of Figure 4 shows the concentration of germanium found by the measurements.

The measurements were carried out by secondary ion mass spectrometry on three samples after they had undergone heat treatments at temperatures of 750°C, 800°C and 850°C for four hours; the respective results are shown by diffusion profiles 62, 63, and 64.

In accordance with that observed in the prior art, it has been observed that the higher the temperature is raised from about 800°C, the greater the diffusion of germanium in the thickness of the layer 2 of silicon subjacent to the layer 1' of $Si_{0.8}Ge_{0.2}$.

Figure 4 also comprises diffusion profiles calculated theoretically from data provided in the document by M Griglione et al entitled "Diffusion of Ge in $Si_{1-x}Ge_x/Si$ single quantum wells in inert and oxidizing ambients" (Journal of Applied Physics, vol 88, n° 3, August 1st, 2000), in which a study of a layer of relaxed silicon/$Si_{0.85}Ge_{0.15}$ was carried out. The diffusion profiles 52, 53, 54 were then found after integrating heat treatments at respective temperatures of 750°C, 800°C, 850°C for four hours into the calculations.

By respectively comparing the measured diffusion profiles 62, 63, 64 and the corresponding theoretical diffusion profiles 52, 53, 54, it can be seen that substantially less Ge was found in the second layer 2 of strained Si with distance from the interface 12 with the first layer 1' in the context of the measurements made by the Applicant than in the theoretical case of a second layer 2 of relaxed Si. This difference in Ge concentration between the measurements and theory becomes even greater with distance from the interface 12 between the two layers. In particular, from a depth of about 10 Å below the interface 12, the differences between theory and the measurements become substantial. Said differences are summarized in the table below, giving ratios between the theoretically calculated Ge concentrations and the Ge concentrations measured by the Applicant:

Depth	220 Angströms	230 Angströms	250 Angströms
Heat treatment at 800°C	1/9	1/70	1/600
Heat treatment at 850°C	1/2	1/6	1/25

The differences between the theory and the measurements in the case of prior heat treatment carried out at 750°C were smaller - see the diffusion profiles 62 and 52. Further, a measurement on a sample which had not undergone heat treatment produced a diffusion profile which was substantially identical to that produced for a sample treated at 750°C. The Applicant has thus confirmed that the diffusion profile does not change substantially between ambient temperature and 750°C.

In contrast, the Applicant has shown that the diffusion profiles 62 and 63 tend to be closer to the initial profile (after epitaxy) than the diffusion profiles of the prior art (i.e. diffusion profiles 53, 54).

Referring now to Figure 5, the Applicant has calculated the diffusion coefficient "D" (in square centimeters per second) (i.e. the y-axis) as a function of the temperature of the heat treatment carried out on the samples (the abscissa represents the inverse of the temperature "T" in kelvins multiplied by 10000).

Points 83 and 84 respectively show the diffusion coefficients found from the measured diffusion profiles 63 and 64 of Figure 3. Points 73 and 74 were found by Griglione (see the above document reference) and correspond to diffusions found after respective heat treatments at 800°C and 850°C for four hours.

It can thus be seen that the diffusion coefficients in the second layer 2 of strained Si are of the order of

four times lower than in a second layer 2 of relaxed Si at the temperatures under consideration.

The results obtained by the Applicant thus show that the diffusion of Ge is surprisingly reduced in the case of a second layer 2 of strained Si compared with the case in which it is of relaxed Si. Post-detachment heat treatments carried out at temperatures higher than those conventionally used can thus be envisaged.

The Applicant thus carried out high temperature rapid thermal annealing (RTA) in accordance with the invention, and has thus demonstrated that its influence on the diffusion of germanium in the second layer 2 of strained Si is much lower than that which could have been deduced from the prior art.

Carrying out an RTA can thus both reduce post-detachment roughness prior to selective etching, and sufficiently stabilize the bonding interface to limit problems with delamination during said selective etching.

Said post-detachment roughness has been limited in the past by being adapted in advance to the implantation conditions, as seen above (co-implantation of H and He), and/or by fracture annealing at 600°C, to reduce the roughness.

Further, RTA can result in encapsulation of the oxide layer by smoothing the layer of SiGe on the wafer sides, as described in FR 03/02623, which further tends to limit delamination problems at the interface at the time of selective etching.

Optionally, it is possible to carry out, prior to RTA, sacrificial oxidation of a portion of the first layer 1', which will then have the effect of reducing the thickness of the $Si_{1-x}Ge_x$ to be lifted off by etching and further reducing roughness prior to carrying out RTA.

Said sacrificial oxidation is carried out at a temperature of less than 650°C, for example. The thickness which is lifted off may be around 500 Å to

1500 Å, preferably about 1000 Å, depending on the thickness of the remaining first layer 1'.

In Figure 1f, the first layer 1' of $Si_{1-x}Ge_x$ is optionally removed to obtain a final strained $Si_{1-y}Ge_y$ on insulator structure. Optionally, the strained $Si_{1-y}Ge_y$ layer may then be made thicker by epitaxy.

To selectively remove the $Si_{1-x}Ge_x$ layer 1', selective chemical etching may be carried out using chemical agents adapted to the materials present.

Thus, in a first example, the second layer 2 is formed of strained Si (i.e. $y = 0$); it is then possible to use HF: H_2O_2: CH_3COOH, SC1 ($NH_4OH/H_2O_2/H_2O$), or HNA ($HF/HNO_3/H_2O$) to remove the residue of the first layer 1'.

A selectivity of about 40:1 between the SiGe and the sSi may be achieved with $CH_3COOH/H_2O_2/HF$.

One example of a concentration which may be selected for $CH_3COOH/H_2O_2/HF$ is 4:3:0.25, and for SC1, 1:1:5.

The etching time is directly correlated to the rate of etching. It is typically about 5 minutes for 800 Å to be etched with $CH_3COOH/H_2O_2/HF$.

In a second example, the first layer 1' has a Ge concentration of 20% or less (i.e. $x \leq 0.2$) and the second layer 2 has a Ge concentration of more than 25% (i.e. $y \geq 0.25$); it is then possible to use TMAH or KOH to remove the residue of the first layer 1'.

Carrying out RTA, optionally combined with prior co-implantation and/or plasma activation and/or low temperature heat treatment for reinforcing the bonding interface and/or sacrificial oxidation, having considerably reduced the surface roughness and non-uniformity of thickness in removed layers 1' and 2, thus allows selective etching to be carried out which is substantially identical to the prior art, but also dispenses with the disadvantages which could arise, such as the necessity to carry out prior mechanical polishing.

Further, reinforcing the bonding (carried out by RTA at least) is sufficient to overcome problems encountered with edge delamination mentioned above.

Finally, fine etching of the surface layer of strained $Si_{1-y}Ge_y$ (by SC1 treatment, for example) may follow selective etching to lift a small amount of material into which the Ge could have been able to diffuse.

The method may optionally be terminated by a high temperature stabilization step to close the bonding interface and/or by furnace annealing or RTA to carry out final smoothing of the strained $Si_{1-x}Ge_x$ layer if the roughness subsisting after selective etching has to be further smoothed.

Optionally, a final crystal growth step (epitaxy, for example MBE or CVD) can be carried out to thicken the second layer 2 formed of strained $Si_{1-y}Ge_y$.

In accordance with a second variation of the invention, referring now to Figures 2a and 2b, the donor wafer 10 comprises, in succession prior to removal, a first layer 1 formed of $Si_{1-x}Ge_x$, a second layer 2 formed of strained $Si_{1-y}Ge_y$, then a third layer 3 formed of $Si_{1-x}Ge_x$. The zone of weakness is then formed in accordance with the invention beneath the second layer 2, for example in the first layer 1. Selective etching of the $Si_{1-x}Ge_x$ can then be carried out after RTA, in accordance with the foregoing, to produce a final strained $Si_{1-y}Ge_y$ /$Si_{1-x}Ge_x$ on insulator structure 30 (as shown in Figure 2b) with a second layer 2 formed of strained $Si_{1-y}Ge_y$ and a third layer 3 formed of $Si_{1-x}Ge_x$.

Optionally, the second layer formed of strained $Si_{1-y}Ge_y$ can be rendered thicker by crystal growth.

Optionally and alternatively, a second selective strained $Si_{1-y}Ge_y$ chemical etching step may then be carried out.

When $x = 0$ (i.e. the second layer 2 is formed of strained Si), chemical species based, for example, on KOH

(potassium hydroxide), NH_4OH (ammonium hydroxide), TMAH (tetramethyl ammonium hydroxide), EDP (ethylene diamine/pyrocatechol/pyrazine) could then be employed. In that case, the second layer 2 formed of strained Si acts only as a stop layer protecting the third layer 3 formed of $Si_{1-x}Ge_x$ from the first chemical attack. A SiGeOI structure 30 (not shown) is thus obtained. Optionally, a layer of strained Si can be grown on the SiGeOI, said new strained layer possibly then having a crystalline structure of better quality than the first layer 1 which had already been etched.

In a third variation of the invention, referring to Figures 3a and 3b, the donor wafer 10 comprises, prior to removal, a multilayer structure comprising alternating first layers 1A, 1B, 1C, 1D, 1E formed of $Si_{1-x}Ge_x$ and second layers 2A, 2B, 2C, 2D, 2E formed of strained $Si_{1-y}Ge_y$. A plurality of removal steps of the invention can then be carried out from the same donor wafer 10, each removal then being followed by recycling the remaining portion of the donor wafer 10 to prepare it for a fresh removal. Thus, for example, a first structure 30A of strained $Si_{1-y}Ge_y$ on insulator and a second strained $Si_{1-y}Ge_y$ on insulator structure 30B will be formed of the same donor wafer 10. That type of removal is disclosed in United States document US2004/0053477.

In a particular case of the invention, each strained layer ["2" in Figures 1a to 1f, 2a and 2b, and "2A", "2B", "2C", "2D" or "2E" in Figures 3a and 3b] of the donor wafer 10 is thick, i.e. its thickness is greater than the critical equilibrium thickness (thickness from which elastic stresses start to relax) without relaxing its elastic strains. This is rendered possible by low temperature epitaxial formation. As an example, a layer of strained Si deposited at temperatures in the range from about 450°C to 650°C on a growth support formed of $Si_{0.8}Ge_{0.2}$ may typically reach a thickness in the range

from about 30 nm to 60 nm without said strains relaxing in one way or another.

If such a thick strained layer is thus formed, care must be taken not to exceed a certain limiting temperature (which is close to the deposition temperature) in the subsequent treatments, and in particular treatments which are between depositing the layer and detaching it by Smart-Cut®, to avoid relaxing the strains.

In this case of a thick strained layer, then, plasma activation prior to bonding (as discussed above) is advantageously carried out at a typical ambient temperature of less than about 100°C. Further, at least one bonding layer of dielectric material such as SiO_2 is advantageously formed on one or both surfaces to be bonded, said layer of dielectric material subsequently helping (i.e. after detachment) to retain the elastic strains. As a complement to plasma activation, post-detachment heat treatment at a temperature T (as discussed above) can be carried out, T advantageously being lower than the temperature at which the thick strained layer is deposited in the case in which no bonding layer has been provided.

Clearly, the skilled person could readily implement the invention when minor species are added to the $Si_{1-x}Ge_x$ and $Si_{1-y}Ge_y$ layers, adding, for example, doping species and/or carbon in small quantities (about 5% or less).

CLAIMS

1. A method for forming a semiconductor structure, which comprises:

providing a donor wafer that includes a first layer of $Si_{1-x}Ge_x$ and a second layer of $Si_{1-y}Ge_y$ located on the first layer, with x and *y* respectively, being in the range of 0 to 1, and x being different than y;

implanting atomic species into the donor wafer to form a zone of weakness in the first layer;

bonding the donor wafer to a receiver wafer;

detaching the second layer and a portion of the first layer from the donor wafer by supplying energy to bonded wafers sufficient to cause cleavage at the zone of weakness to form an intermediate structure thereof;

conducting a rapid thermal anneal of the intermediate structure at a temperature of about 1000°C or more for a period of time not exceeding 5 minutes; and

removing any remaining portions of the first layer of the intermediate structure to provide a semiconductor structure comprising the second layer on the receiving wafer.

2. The method of claim 1, wherein the remaining portions of the first layer are removed from the intermediate structure by selective etching.

3. The method of claim 1, wherein the rapid thermal anneal is carried out at a temperature of from about 1000°C to about 1200°C for about 10 seconds to about 30 seconds.

4. The method of claim 1, wherein the rapid thermal anneal is carried out in a reducing atmosphere that includes argon and that optionally includes hydrogen.

5. The method of claim 1, which further comprises conducting a sacrificial oxidation before the rapid thermal annealing to remove some of the remaining portions of the first layer of the intermediate structure.

6. The method of claim 1, which further comprises conducting plasma activation of a bonding surface of at least one of the donor wafer or receiving wafer before bonding the two together.

7. The method of claim 1, which further comprises conducting a heat treatment to reinforce bonding of the wafers wherein the heat treatment is carried out prior to the rapid thermal annealing at a temperature of about 350°C to about 800°C for about 30 minutes to 4 hours.

8. The method of claim 7, wherein the heat treatment is carried out after the detaching but continuously with the detaching, by simply changing the temperature from one that causes detaching to one that reinforces bonding of the wafers.

9. The method of claim 1, which further comprises conducting a heat treatment to reinforce bonding of the wafers, wherein the heat treatment is carried out after removing remaining portions of the first layer and at a temperature of about 1000°C to about 1100°C for about 2 hours.

10. The method of claim 1, wherein the implanted atomic species is hydrogen ions and the hydrogen ions are implanted at a dose of 3×10^{16} atoms/cm^2 to 10×10^{16} atoms/cm^2, and at an implantation energy of 20 keV to 80 keV.

11. The method of claim 1, wherein the implanted atomic species comprises a co-implantation of helium and hydrogen ions, and the helium and hydrogen ions are implanted at a dose of 1×10^{16} atoms/cm^2 and 1×10^{16} atoms/cm^2, respectively, and at implantation energies for each of 20 keV to 80 keV.

12. The method of claim 1 which further comprises growing additional $Si_{1-y}Ge_y$ on the second layer of the semiconductor structure after the removing step to thicken the second layer

13. The method of claim 12, wherein the second layer is formed of elastically strained $Si_{1-y}Ge_y$, and the donor wafer comprises a support substrate formed of bulk Si and a SiGe buffer structure beneath the first and second layers.

14. The method of claim 1 wherein the donor wafer further comprises a third layer formed of $Si_{1-x}Ge_x$ on the second layer where x is between 0 and 1.

15. The method of claim 13, which further comprises selective etching of the second layer as opposed to the third layer.

16. The method of claim 1, wherein the donor wafer comprises a support substrate formed of bulk Si, a SiGe buffer structure and a multilayer structure comprising alternating first layers formed of $Si_{1-x}Ge_x$ and second layers formed of strained $Si_{1-y}Ge_y$ to allow a plurality of removals to be made from the same donor wafer.

17. The method of claim 16, wherein each layer of strained $Si_{1-y}Ge_y$ is thicker than a critical equilibrium thickness where elastic stresses in the layer would otherwise start to relax.

18. The method of claim 16, wherein prior to implanting, further comprises forming the strained layer at a deposition temperature of about 450°C to about 650°C, wherein any treatments carried out between the forming and detaching steps are implemented at temperatures that are less than or equal to the deposition temperature.

19. The method of claim 12, wherein y equals 0.

20. The method of claim 1, wherein prior to bonding, the method further comprises a step of providing a bonding layer on the donor wafer, on the receiver wafer or on both, with the bonding layer comprising an electrically insulating oxide, nitride or oxynitride material.