

## SEMICONDUCTOR MEMORY DEVICE

### CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2017-046395, filed March 10, 2017, the entire contents of which are incorporated herein by reference.

### FIELD

Embodiments described herein relate generally to a semiconductor memory device.

### BACKGROUND

There are proposed semiconductor memory devices with 3-dimensional structures in which memory holes are formed in stacked bodies in which a plurality of electrode layers are stacked on substrates with insulating layers interposed therebetween and silicon bodies serving as channels are formed inside the memory holes via charge storage films. There are proposed technologies for forming control circuits of memory cell arrays with the 3-dimensional structures directly under or directly on the memory cell arrays.

However, in the examples, memory densities per area may not be sufficiently improved.

Examples of related art include JP-A-2011-204829 and JP-A-2016-62901.

### DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic sectional view illustrating a

semiconductor memory device according to a first embodiment.

FIG. 2 is a schematic perspective view illustrating the semiconductor memory device according to the first embodiment.

FIG. 3 is a schematic sectional view illustrating the semiconductor memory device according to the first embodiment.

FIG. 4 is an enlarged schematic sectional view illustrating a part of the semiconductor memory device according to the first embodiment.

FIG. 5 is a schematic perspective view illustrating the semiconductor memory device according to the first embodiment.

FIG. 6 is a schematic sectional view illustrating a method of manufacturing the semiconductor memory device according to the first embodiment.

FIG. 7 is a schematic sectional view illustrating the method of manufacturing the semiconductor memory device according to the first embodiment.

FIG. 8 is a schematic sectional view illustrating the method of manufacturing the semiconductor memory device according to the first embodiment.

FIG. 9 is a schematic sectional view illustrating the method of manufacturing the semiconductor memory device according to the first embodiment.

FIG. 10 is a schematic sectional view illustrating a semiconductor memory device according to a first modification example of the first embodiment.

FIG. 11 is a schematic sectional view illustrating a semiconductor memory device according to a second modification example of the first embodiment.

FIG. 12 is a schematic sectional view illustrating a semiconductor memory device according to a second embodiment.

FIG. 13 is a circuit diagram of the semiconductor memory device according to the second embodiment.

FIG. 14 is a block diagram illustrating a configuration of a system of the semiconductor memory device according to the second embodiment.

#### DETAILED DESCRIPTION

[0005] Exemplary embodiments provide a miniature semiconductor memory device with high performance.

[0006] In general, according to one embodiment, a semiconductor memory device includes a plurality of memory cell array layers that include a first surface and a second surface opposite to the first surface and do not include a substrate and that include a plurality of memory cells arranged 3-dimensionally in a memory cell array region and a surface wiring layer embedded in the first surface or/and the second surface. The surface wiring layer of each of the memory cell array layers is formed to overlap the first surface when viewed in a direction vertical to the first surface, and the surface wiring layers are bonded to each other so that the plurality of memory cell array layers are stacked.

[0008] Hereinafter, embodiments will be described with reference to the drawings. The same reference numerals are given to the same elements in the drawings.

[0009] (First Embodiment)

FIG. 1 is a schematic sectional view illustrating a semiconductor memory device according to a first embodiment. The semiconductor memory device according to the first embodiment has a structure in which a peripheral circuit layer 100 including a control circuit that controls writing, erasing, and reading data with respect to memory cells and a first memory cell array layer 200 including a plurality of first memory cells arranged 3-dimensionally are bonded and stacked to face each other and are attached. The semiconductor memory device has a structure in which the first memory cell array layer 200 and a second memory cell array layer 300 including a plurality of second memory cells arranged 3-dimensionally are bonded and stacked to face each other and are attached.

[0010] First, the first memory cell array layer 200 will be described. The first memory cell array layer 200 includes a first surface (lower surface) Sa1 and a second surface (upper surface) Sa2 opposite to the first surface in FIG. 1 and includes a first memory cell array 10a with a 3-dimensional structure. FIG. 2 is a schematic perspective view illustrating the semiconductor memory device according to the first embodiment and illustrating the first memory cell array

10a. In FIG. 2, some insulating layers such as inter-electrode insulating layers are not illustrated. In FIG. 2, the upper and lower sides in FIG. 1 are reversed, and thus the upper side is the first surface side and the lower side is the second surface side in FIG. 2.

[0011]In FIG. 2, two directions orthogonal to each other are set as the X and Y directions and a direction which is orthogonal to the X and Y directions (XY plane) and in which a plurality of electrode layers WL are stacked is set as the Z direction (a stacking direction).

[0012]The first memory cell array 10a includes a first stacked body 12a in which a plurality of layers of one electrode layer WL and one insulating layer 11 are alternately stacked. A plurality of first columnar portions 13a extending in the Z direction are formed inside the first stacked body 12a. The first columnar portions 13a are formed in, for example, a cylindrical shape or an elliptic cylindrical shape. For example, the plurality of first columnar portions 13a are arranged in a staggered pattern or a square grid pattern on the XY plane. The electrode layers WL are separated into a plurality of blocks in the Y direction and extend in the X direction.

[0013]The electrode layer WL is a layer that contains, for example, silicon as a main component. Further, the electrode layer WL contains boron as impurities for conductivity of a

silicon layer. The electrode layer WL may also contain metal silicide.

[0014]The insulating layer 11 mainly contains, for example, silicon and oxygen and is formed of a silicon oxide film ( $\text{SiO}_2$ ), a silicon oxynitride film ( $\text{SiON}$ ), or a carbon-containing silicon oxide film ( $\text{SiOC}$ ).

[0015]A drain-side selection gate SGD is formed in upper portions of the first columnar portions 13a on the side of the first surface Sa1 and a source-side selection gate SGS is formed in lower portions of the first columnar portions 13a on the side of the second surface Sa2. The drain-side selection gate SGD is formed on the uppermost electrode layer WL with the insulating layer 11 interposed therebetween. The source-side selection gate SGS is formed below the lowermost electrode layer WL with the insulating layer 11 interposed therebetween. Here, for example, the drain-side selection gate SGD and the source-side selection gate SGS can be formed to be thicker than the electrode layer WL of one layer.

[0016]First bit lines 16a are connected to upper ends of the first columnar portions 13a on the side of the first surface Sa1. The plurality of first bit lines 16a are formed of a metal. The plurality of first bit lines 16a are separated in the X direction to extend in the Y direction. The first bit lines 16a are formed on the drain-side selection gate SGD with the insulating layer 11 and an interlayer insulating layer 14

interposed therebetween.

[0017]A first source line 17a is connected to lower ends of the first columnar portions 13a on the side of the second surface Sa2. The first source line 17a is formed below the source-side selection gate SGS with an interlayer insulating layer 15 interposed therebetween. A first source-side wiring layer 19a is formed inside an interlayer insulating layer 18 at the lower ends of the first columnar portions 13a and further below the first source line 17a. The interlayer insulating layer 18 may be a stacked layer.

[0018]FIG. 3 is a schematic sectional view illustrating the semiconductor memory device according to the first embodiment and illustrating the vicinity of the first columnar portions. FIG. 4 is an enlarged schematic sectional view illustrating a portion A which is a part of the vicinity of the first columnar portion in FIG. 3. FIGS. 3 and 4 illustrate a cross section parallel to the YZ plane in FIG. 2.

[0019]As illustrated in FIG. 3, the first columnar portion 13a is formed inside an I-shaped memory hole formed inside the first stacked body 12a including the plurality of electrode layers WL and the plurality of insulating layers 11. A channel body 20 serving as a semiconductor channel is formed inside the memory hole. The channel body 20 is, for example, a silicon film. An impurity concentration of the channel body 20 is lower than an impurity concentration of the electrode layer WL.

[0020]As illustrated in FIG. 4, in a memory cell MC, a memory film 21 is formed between the inner wall of the memory hole and the channel body 20. The memory film 21 includes, for example, a block insulating film 22, a charge storage film 23, and a tunnel insulating film 24. Between the electrode layer WL and the channel body 20, the block insulating film 22, the charge storage film 23, and the tunnel insulating film 24 are formed in order from the electrode layer WL side.

[0021]The channel body 20 is formed in a cylindrical shape extending in the stacking direction of the stacked body. The memory film 21 is formed in a cylindrical shape while extending in the stacking direction of the stacked body to surround the outer circumferential surface of the channel body 20. The electrode layer WL surrounds the periphery of the channel body 20 via the memory film 21 interposed therebetween. A core insulating film 25 is formed inside the channel body 20. The core insulating film 25 is, for example, a silicon oxide film.

[0022]The block insulating film 22 comes into contact with the electrode layer WL, the tunnel insulating film 24 comes into contact with the channel body 20, and the charge storage film 23 is formed between the block insulating film 22 and the tunnel insulating film 24.

[0023]The channel body 20 functions as a channel of the memory cell MC and the electrode layer WL functions as a control gate of the memory cell. The charge storage film 23 functions as

a data storage layer that stores charges injected from the channel body 20. That is, the memory cell MC that has a structure in which the control gate surrounds around the channel at an intersection of the channel body 20 and each electrode layer WL is formed.

[0024]The semiconductor memory device according to the first embodiment can be free to electrically execute erasing and writing data. Thus, the semiconductor memory device is a nonvolatile semiconductor memory device capable of retaining stored contents even when power is turned off.

[0025]The memory cell MC is, for example, a charge trapping memory cell. The charge storage film 23 has several trap sites trapping charges and is, for example, a silicon nitride film. The memory cell MC may be a floating gate memory cell.

[0026]The tunnel insulating film 24 becomes a potential barrier when charges are injected from the channel body 20 to the charge storage film 23 or when charges stored in the charge storage film 23 are diffused to the channel body 20. The tunnel insulating film 24 is, for example, a silicon oxide film.

[0027]Alternatively, a stacked film (ONO film) that has a structure in which a silicon nitride film is interposed between a pair of silicon oxide films may be used as the tunnel insulating film. When the ONO film is used as the tunnel insulating film, an erasing operation can be executed in a low electric field compared to a silicon oxide film of a single

layer.

[0028]The block insulating film 22 prevents the charges stored in the charge storage film 23 from diffusing to the electrode layer WL. The block insulating film 22 includes, for example, a silicon nitride film 221 formed to come into contact with the electrode layer WL and a silicon oxide film 222 formed between the silicon nitride film 221 and the charge storage film 23.

[0029]By forming the silicon nitride film 221 which is a layer with a higher dielectric constant than the silicon oxide film 222 to be in contact with the electrode layer WL, it is possible to prevent back-tunneling electrons injected from the electrode layer WL at the time of erasing. That is, by using a stacked film of the silicon oxide film and the silicon nitride film as the block insulating film 35, it is possible to improve a charge blocking property.

[0030]As illustrated in FIGS. 2 and 3, the drain-side select transistor STD is formed in the upper portions of the first columnar portions 13a and the source-side select transistor STS is formed in the lower portions of the first columnar portions 13a.

[0031]The memory cell MC, the drain-side select transistor STD, and the source-side select transistor STS are vertical transistors in which a current flows in the stacking direction (the Z direction) of the stacked body.

[0032]The drain-side selection gate SGD functions as a gate electrode (control gate) of the drain-side select transistor STD. An insulating film 26 (see FIG. 3) that functions as a gate insulating film of the drain-side select transistor STD is formed between the drain-side selection gate SGD and the channel body 20. The channel body 20 of the drain-side select transistor STD formed in the first columnar portion 13a is connected to a bit line BL above the drain-side selection gate SGD.

[0033]The source-side selection gate SGS functions as a gate electrode (control gate) of the source-side select transistor STS. An insulating film 27 (see FIG. 3) that functions as a gate insulating film of the source-side select transistor STS is formed between the source-side selection gate SGS and the channel body 20. The channel body 20 of the source-side select transistor STS formed in the first columnar portion 13a is connected to a source line SL below the source-side selection gate SGS.

[0034]A first source-side wiring layer 19a is formed inside the interlayer insulating layer 18 further below the source line SL.

[0035]The plurality of memory cells MC, the drain-side select transistor STD, and the source-side select transistor STS are connected in series through the channel body 20 to configure one I-shaped memory string MS. By arranging the plurality of

memory strings MS in the X and Y directions, the plurality of memory cells MC are arranged 3-dimensionally in the X, Y, and Z directions.

[0036]FIG. 1 illustrates a region of an end of the foregoing first memory cell array 10a in the X direction. A stair structure 29 of the electrode layers WL extending in the X direction is formed at an end of a first memory cell array region 28a in which the plurality of memory cells MC are arranged. In the stair structure 29, the ends of each of the electrode layers WL of the layers in the X direction are formed in a stair shape. A plurality of contact plugs 30 connected to each of the electrode layers WL of the layers formed in the stair shape are formed in the stair structure 29. The contact plugs 30 are connected to each of the electrode layers WL of the layers in the stair shape to penetrate through the interlayer insulating layer 31.

[0037]In the stair structure 29, the selection gates SG (the drain-side selection gate SGD and the source-side selection gate SGS) are connected to contact plugs 32.

[0038]The contact plug 30 connected to the electrode layer WL is connected a word wiring layer 33. The contact plug 32 connected to the selection gate SG is connected to a selection gate wiring layer 34. The word wiring layer 33 and the selection gate wiring layer 34 are formed in the same layer.

[0039]The first memory cell array layer 200 does not include

a substrate. A first source-side wiring layer 19a is formed to be closer to the second surface side than a first source line SL.

At least parts of the word wiring layer 33 and the selection gate wiring layer 34 are led as a word-line lead portion 35 and a selection-gate-line lead portion 36, by other wiring layers or plugs, to the outside of the first memory cell array region 28a when viewed in a direction vertical to the first surface. The word-line lead portion 35 and the selection-gate-line lead portion 36 led to the outside of the first memory cell array region 28a are connected to a first signal line extraction electrode 37a formed outside the first memory cell array region 28a.

[0040]The channel body 20 of the first columnar portion 13a is electrically connected to the first bit line BL and the first source line SL. Similarly, at least parts of the first bit line BL and the first source line SL are led as a first bit-line lead portion and a first source-line lead portion (not illustrated) by other wiring layers or plugs to the outside of the first memory cell array region 28a when viewed in a direction vertical to the first surface. The first bit-line lead portion and the first source-line lead portion led outside the first memory cell array region 28a are connected to the first signal line extraction electrode 37a formed outside the first memory cell array region 28a.

[0041]A first surface wiring layer 38a and a second surface wiring layer 39a are formed on the first surface Sa1 and the second surface Sa2 of the first memory cell array layer 200. The first surface wiring layer 38a and the second surface wiring layer 39a are embedded in the first surface Sa1 and the second surface Sa2, respectively, so that front surfaces are exposed from interlayer insulating layers (not illustrated). Here, for example, the first signal line extraction electrode 37a is electrically connected to the first surface wiring layer 38a and the second surface wiring layer 39a formed on the first surface Sa1 and the second surface Sa2 of the first memory cell array layer 200, respectively. The first signal line extraction electrode 37a, the first surface wiring layer 38a, and the second surface wiring layer 39a penetrate through the first memory cell array layer 200.

[0042]First external connection electrodes 40a are formed outside the first memory cell array region 28a. That is, the first external connection electrodes 40a are formed in a region further outside than the stair structure in the memory cell array. The first external connection electrodes 40a are electrically connected to the first surface wiring layer 38a and the second surface wiring layer 39a formed on the first surface Sa1 and the second surface Sa2 of the first memory cell array layer 200. The first surface wiring layer 38a and the second surface wiring layer 39a are embedded in the first

surface Sa1 and the second surface Sa2, respectively, so that front surfaces are exposed from the interlayer insulating layers (not illustrated). The first external connection electrode 40a, the first surface wiring layer 38a, and the second surface wiring layer 39a penetrate through the first memory cell array layer 200.

[0043]The peripheral circuit layer 100 includes a circuit board 1. The circuit board 1 of the peripheral circuit layer 100 is, for example, a silicon substrate. A control circuit is formed on a circuit formation surface of the circuit board 1 of the peripheral circuit layer. As the control circuit, an integrated circuit including a transistor is formed. The transistor has a MOSFET structure that has a gate electrode and a source/drain region. The source/drain region of the MOSFET is connected to a circuit-side connection electrode 41 by another wiring layer or a plug. The circuit-side connection electrode 41 is electrically connected to a circuit-side wiring layer 42 formed on the circuit formation surface of the peripheral circuit layer 100. The circuit-side wiring layer 42 is embedded in the circuit formation surface so that a front surface is exposed from an interlayer insulating layer (not illustrated).

[0044]The second memory cell array layer 300 has the same configuration as the first memory cell array layer 200 illustrated in FIGS. 1 to 4. That is, the second memory cell

array layer 300 includes a third surface (lower surface) Sb1 and a fourth surface (upper surface) Sb2 opposite to the third surface in FIG. 1 and includes a second memory cell array 10b with a 3-dimensional structure. The other same configuration will not be described.

[0045]The second memory cell array layer 300 does not include a substrate. A second source-side wiring layer 19b is further formed to be closer to the fourth surface than the second source line SL.

As in the first memory cell array layer 200, at least parts of the word wiring layer 33 and the selection gate wiring layer 34 are led as a word-line lead portion 35 and a selection-gate-line lead portion 36 by other wiring layers or plugs to the outside of a second memory cell array region 28b when viewed in a direction vertical to the third surface. The word-line lead portion 35 and the selection-gate-line lead portion 36 led outside the second memory cell array region 28b are connected to a second signal line extraction electrode 37b formed outside the second memory cell array region 28b.

[0046]The channel body 20 of the second columnar portion 13b is electrically connected to the second bit line BL and the second source line SL. Similarly, at least parts of the second bit line BL and the second source line SL are led as a second bit-line lead portion and a second source-line lead portion by other wiring layers or plugs to the outside of the second

memory cell array region 28b when viewed in the direction vertical to the third surface. The second bit-line lead portion and the second source-line lead portion led outside the second memory cell array region 28b are connected to the second signal line extraction electrode 37b formed outside the second memory cell array region 28b. A configuration of the second memory cell array region 28b is the same as that inside the first memory cell array layer 200, and thus reference numerals are not given.

[0047]A third surface wiring layer 38b and a fourth surface wiring layer 39b are formed on the third surface Sb1 and the fourth surface Sb2 of the second memory cell array layer 300. The third surface wiring layer 38b and the fourth surface wiring layer 39b are embedded in the third surface Sb1 and the fourth surface Sb2, respectively, so that front surfaces are exposed from interlayer insulating layers (not illustrated). Here, for example, the second signal line extraction electrode 37b is electrically connected to the third surface wiring layer 38b and the fourth surface wiring layer 39b formed on the third surface and the fourth surface of the second memory cell array layer 300, respectively. The second signal line extraction electrode and the third and fourth surface wiring layers penetrate through the second memory cell array layer 300.

[0048]Second external connection electrodes 40b are formed outside the second memory cell array region 28b. That is, the

second external connection electrodes 40b are formed in a region further outside than the stair structure in the memory cell array. The second external connection electrodes 40b are electrically connected to the third surface wiring layer 38b and the fourth surface wiring layer 39b formed on the third surface Sb1 and the fourth surface Sb2 of the second memory cell array layer 300. The third surface wiring layer 38b and the fourth surface wiring layer 39b are embedded in the third surface Sb1 and the fourth surface Sb2, respectively, so that front surfaces are exposed from interlayer insulating layers (not illustrated). The second external connection electrodes 40b, the third surface wiring layer 38b, and the fourth surface wiring layer 39b penetrate through the second memory cell array layer 300. An external connection pad 52 is formed on a surface wiring layer electrically connected to the second external connection electrodes 40b among the fourth surface wiring layers 39b.

[0049]As illustrated in FIG. 1, the first surface wiring layer 38a formed on the first surface Sa1 is attached to be bonded with the circuit-side wiring layer 42 formed on the circuit formation surface. The first surface wiring layer 38a and the circuit-side wiring layer 42 are formed of, for example, copper or copper alloys which have copper as a main component. An insulating film (not illustrated) is formed around the first surface wiring layer 38a and the circuit-side wiring layer 42.

The insulating film is, for example, an inorganic film or a resin film. The first memory cell array layer 200 and the peripheral circuit layer 100 are electrically connected via the first surface wiring layer 38a and the circuit-side wiring layer 42.

[0050]As illustrated in FIG. 1, the second surface wiring layer 39a formed on the second surface Sa2 is attached to be bonded with the third surface wiring layer 38b formed on the third surface Sb1. The second surface wiring layer 39a and the third surface wiring layer 38b are formed of, for example, copper or copper alloys which have copper as a main component. An insulating film (not illustrated) is formed around the second surface wiring layer 39a formed on the second surface and the third surface wiring layer 38b formed on the third surface Sb1. The insulating film is, for example, an inorganic film including a silicon nitride film. The first memory cell array layer and the second memory cell array layer are electrically connected via the second surface wiring layer 39a and the third surface wiring layer 38b.

[0051]When the insulating film around the wiring layers is an inorganic film, the wiring layers can be bonded to each other on the bonding surfaces and the inorganic films can be bonded using hydrogen bonding. Accordingly, when the inorganic film is used as the insulating film, a gap between the bonding surfaces rarely occurs. Therefore, it is preferable to use

the inorganic film in that it is not necessary to perform under-filling using a resin film.

[0052]FIG. 5 is a schematic perspective view illustrating the semiconductor memory device according to the first embodiment and illustrating an electric connection state of the peripheral circuit layer, the first memory cell array layer, and the second memory cell array layer.

[0053]As illustrated in FIG. 5, the peripheral circuit layer 100, the first memory cell array layer 200, and the second memory cell array layer 300 are electrically connected by the first signal line extraction electrodes, the second signal line extraction electrodes, the first external connection electrodes, and the second external connection electrodes (not illustrated). The signal line extraction electrodes are formed outside the memory cell array regions 28a and 28b and the external connection electrodes are formed in a region which is outside the memory cell array regions and is further outside than the stair structure in the memory cell array. The signal line extraction electrode and the external connection electrode of the memory cell array layer are formed in overlapping regions when viewed in the direction vertical to the first surface Sa1. The signal line extraction electrode is electrically connected to the surface wiring layers 39a and 39b and the external connection electrode of the second memory cell array layer 300 which is the uppermost layer is

electrically connected to the external connection pad 52. In FIG. 5, only parts of electric connection states of the first signal line extraction electrodes, the second signal line extraction electrodes, the first external connection electrodes, and the second external connection electrodes are illustrated and the other parts are not illustrated.

[0054]A method of manufacturing the semiconductor memory device according to the first embodiment will be described with reference to FIGS. 6 to 9. FIGS. 6 to 9 are diagrams illustrating one cross-section of the semiconductor memory device in a method of manufacturing the semiconductor memory device according to the first embodiment.

[0055]As illustrated in FIG. 6, a control circuit including transistors and the like are formed on the circuit board 1 and the peripheral circuit layer 100 including the circuit-side wiring layer 42 of which a front surface is exposed from the insulating film (not illustrated) is formed. The first insulating layer 50 serving as a buffer layer, for example, a silicon oxide film under another substrate 2, is formed, the first source-side wiring layers 19a and the first source line 17a are formed under the first insulating layer 50, and the first selection gates SG, the plurality of electrode layers WL, and the like are formed under the first source line 17a. Next, the memory strings MS, the stair structure 29, and the like are formed. Further, the first external connection

electrodes 40a, the first signal line extraction electrodes 37a, and the first surface wiring layers 38a of which front surfaces are exposed from the insulating films (not illustrated) are formed to form the first memory cell array layer 200. Subsequently, the circuit-side wiring layer 42 of the peripheral circuit layer 100 and the first surface wiring layer 38a of the first memory cell array layer 200 are stacked to face each other.

[0056]Next, as illustrated in FIG. 7, the peripheral circuit layer 100 and the first memory cell array layer 200 are stacked. At this time, the circuit-side wiring layer 42 and the first surface wiring layer 38a are bonded. As a bonding method, for example, these layers are bonded by applying a mechanical pressure to be subjected to diffusion bonding. Alternatively, an inert plasma treatment is performed on the bonding surfaces and the layers are bonded using hydrogen bond produced by forming OH groups on the bonding surfaces. Alternatively, these layers are bonded using an organic adhesive or the like. Thereafter, for example, the substrate 2 is removed using a chemical liquid such as KOH. At this time, the insulating films around the wiring layers can also be bonded.

[0057]Since the memory cell array layer does not include a substrate, deformation easily occurs due to stress applied to the memory cell array layer and the stacked semiconductor memory device is considered to be bent. Accordingly, the

second insulating layer 51 is formed. The second insulating layer 51 is a layer that has stress in an opposite direction to a bent state occurring after the substrate is removed and is formed as a stress adjusting film. As the second insulating film 51, for example, a silicon nitride film is formed. In this way, it is possible to alleviate stress occurring in the semiconductor memory device, and thus it is possible to prevent a bent state of the semiconductor memory device.

[0058]Next, the first insulating layer 50 and the second insulating layer 51 are removed to form grooves so that the upper surfaces of the first external connection electrodes 40a and the first signal line extraction electrodes 37a are exposed. As illustrated in FIG. 8, the second surface wiring layers 39a which are bonding metals are formed in the grooves such that the upper surfaces of the second surface wiring layers 39a are exposed.

[0059]Next, subsequently to FIG. 8, the same processes as those in FIGS. 6 to 8 are repeated on the first memory cell array layer 200 instead of the peripheral circuit layer 100 illustrated in FIG. 6 and on the second memory cell array layer 300 instead of the first memory cell array layer 200 illustrated in FIG. 6. As illustrated in FIG. 9, the external connection pad 52 is formed on the surface wiring layer electrically connected to the second external connection electrodes 40b among the fourth surface wiring layers 39b exposed to the upper

surfaces. In this way, it is possible to form the semiconductor memory device in which the peripheral circuit layer 100, the first memory cell array layer 200, and the second memory cell array layer 300 are stacked.

[0060]In the first embodiment, the second memory cell array layer 300 is stacked on the first memory cell array layer 200. However, another memory cell array layer of one layer or multiple layers may be stacked on the second memory cell array layer 300. At this time, at least some layers of the other memory cell array layer of one layer or multiple layers may include a substrate. In this case, it is possible to reduce a bent state of the stacked semiconductor memory device.

[0061]Only a stacked body of the memory cell array layer may be formed without stacking the peripheral circuit layer 100.

[0062](First Modification Example)

FIG. 10 is a schematic sectional view illustrating the semiconductor memory device according to a first modification example of the first embodiment. A wiring layer 61 is formed to connect a memory string MS1 of the first memory cell array layer 200 to a memory string MS2 of the second memory cell array layer 300. The wiring layer 61 is formed inside the memory cell array region and is connected to the first source-side wiring layer 19a of the first memory cell array layer 200 and the second bit line 16b of the second memory cell array layer 300. The first memory cell array layer and the second memory

cell array layer are connected without interposing signal line extraction electrodes formed outside the memory cell array region.

[0063]In the first modification example, the first memory cell array layer and the second memory cell layer are connected using the wiring layers formed inside the memory cell array region in addition to the signal line extraction electrodes formed outside the memory cell array region.

[0064]By forming the semiconductor memory device in this way, it is possible to reduce electrode areas necessary to connect the memory cell array layers, and thus it is possible to reduce chip areas.

[0065](Second Modification Example)

FIG. 11 is a schematic sectional view illustrating the semiconductor memory device according to a second modification example of the first embodiment. The external connection electrode will not be described.

[0066]At least parts of the word wiring layer and the selection gate wiring layer of the first memory cell array layer 200 are led as the word-line lead portion 35 and the selection-gate-line lead portion 36 by other wiring layers or plugs and are folded inside the first memory cell array region 28a when viewed in a direction vertical to the first surface Sa1. The word-line lead portion 35 and the selection-gate-line lead portion 36 led inside the first memory

cell array region 28a are connected to the first signal line extraction electrodes 37a formed inside the first memory cell array region 28a.

[0067] Similarly, at least parts of the first bit line BL and the first source line SL are led as a first bit-line lead portion and a first source-line lead portion by other wiring layers or plugs and are folded inside the first memory cell array region 28a when viewed in a direction vertical to the first surface Sa1 (not illustrated). The first bit-line lead portion and the first source-line lead portion led inside the first memory cell array region 28a are connected to the first signal line extraction electrode 37a formed inside the first memory cell array region 28a.

[0068] The first source-side wiring layer 19a on the side of the second surface Sa2 is connected to the first signal line extraction electrode 37a formed inside the first memory cell array region 28a. Here, some of the first signal line extraction electrodes 37a may be formed outside the first memory cell array region 28a.

[0069] The first surface wiring layer 38a and the second front surface wiring layer 39a are formed on the first surface Sa1 and the second surface Sa2 of the first memory cell array layer 200, respectively, inside the memory cell array region. The first surface wiring layer 38a and the second surface wiring layer 39a formed inside the memory cell array region are

electrically connected to the first signal line extraction electrodes 37a.

[0070]As in the first memory cell array layer 200, at least parts of the word wiring layer and the selection gate wiring layer of the second memory cell array layer 300 are led as the word-line lead portion 35 and the selection-gate-line lead portion 36 by other wiring layers or plugs and are folded inside the second memory cell array region 28b when viewed in a direction vertical to the third surface Sb1. The word-line lead portion 35 and the selection-gate-line lead portion 36 led inside the second memory cell array region 28b are connected to the second signal line extraction electrodes 37b formed inside the second memory cell array region 28b.

[0071]In addition, at least parts of the second bit line BL and the second source line SL are led as a second bit-line lead portion and a second source-line lead portion by other wiring layers or plugs and are folded inside the second memory cell array region 28b when viewed in a direction vertical to the third surface (not illustrated). The second bit-line lead portion and the second source-line lead portion led inside the second memory cell array region 28b are connected to the second signal line extraction electrode 37b formed inside the second memory cell array region 28b. Here, some of the second signal line extraction electrodes 37b may also be formed outside the second memory cell array region 28b.

[0072]On the third surface Sb1 of the second memory cell array layer 300, the third front surface layer 38b is formed inside the memory cell array region. The third surface wiring layer 38 formed inside the memory cell array region is electrically connected to the second signal line extraction electrode 37b. Here, on the fourth surface Sb2 of the second memory cell array layer 300, the fourth surface wiring layer (not illustrated) may be formed inside the memory cell array region. In this case, the fourth surface wiring layer formed inside the memory cell array region is electrically connected to the second signal line extraction electrode 37b.

[0073]Accordingly, the signal line extraction electrode of each memory cell array layer is connected to the surface wiring layer formed inside the memory cell array region and the surface wiring layer of each memory cell array layer can be formed in each overlapping region when viewed in the direction vertical to the first surface. Accordingly, when the plurality of memory cell array layers are stacked, it is possible to further reduce chip areas and reduces wiring lengths, and thus it is possible to prevent operation delay.

[0074]According to the second modification example, at least some of the bit lines or the work lines are folded inside the memory cell array region. The signal line extraction electrodes connected via the bit-line lead portion and the word-line lead portion are formed inside the memory cell array

region. The signal line extraction electrode of each memory cell array layer is connected to the surface wiring layer formed inside the memory cell array region and the surface wiring layer of each memory cell array layer can be formed in each overlapping region when viewed in the direction vertical to the first surface. Accordingly, when the plurality of memory cell array layers are stacked, it is possible to further reduce chip areas and reduce wiring lengths, and thus it is possible to prevent operation delay.

[0075]According to the first embodiment, the first memory cell array layer 200 and the second memory cell array layer 300 do not include a substrate (for example, a silicon substrate). Accordingly, when first memory cell array layer 200 and the second memory cell array layer 300 are stacked and electrically connected, these layers can be connected without forming a through silicon via (TSV). Accordingly, it is not necessary to perform a substrate etching process which takes cost or a processing time and to form an insulating film to prevent short-circuiting between a substrate and a via. Thus, it is possible to achieve a reduction in cost and an improvement in a throughput.

[0076]The memory cell array layer and the peripheral circuit layer are formed in different wafer processes. Therefore, even when a high-temperature heating process is necessary at the time of forming the memory cell array layer, it is possible

to prevent impurity diffusion of the transistors of the peripheral circuit layer or an adverse influence such as deterioration in a metal wiring layer.

[0077]The memory cell array layer is stacked so that the first surface faces the peripheral circuit layer. The bit line or the word line is led to the first surface of the memory cell array layer and the bit line or the word line is connected to the signal line extraction electrode. Since the memory cell array layer is stacked so that the first surface faces the peripheral circuit layer, it is possible to reduce a dragging distance of the electrode layer, and thus it is possible to prevent an adverse influence on an operation speed.

[0078]Further, according to the first embodiment, the memory cell array layers of the plurality of layers are stacked on the peripheral circuit layer. Accordingly, when the stacked body of one memory cell array layer has 48 layers, a memory cell array having 96 layers which is a double of the 48 layers can be realized, for example, using a process technique for 48 layers by stacking two memory cell array layers. Accordingly, it is possible to easily improve a memory density.

[0079]Further, at least some of the bit lines or the word lines are led outside the memory cell array region, and the signal line extraction electrodes connected via the bit-line lead portion and the word-line lead portion are formed outside the memory cell array region. In addition, external connection

electrodes are formed in a region which is outside the memory cell array region and is further outside the stair structure in the memory cell array. The signal line extraction electrode and the external connection electrode of each memory cell array layer are formed in each overlapping region when viewed in the direction vertical to the first surface. Accordingly, when the plurality of memory cell array layers are stacked, it is possible to reduce wiring lengths, and thus it is possible to prevent operation delay.

[0080]Alternatively, at least some of the bit lines or the word lines are repeated inside the memory cell array region. The signal line extraction electrode connected via the bit-line lead portion and the word-line lead portion is formed inside the memory cell array region. The signal line extraction electrode of each memory cell array layer is connected to the surface wiring layer formed inside the memory cell array region and the surface wiring layer of each memory cell array layer is formed in each overlapping region when viewed in the direction vertical to the first surface. Accordingly, when the plurality of memory cell array layers are stacked, it is possible to further reduce chip areas and reduce wiring lengths, and thus it is possible to prevent operation delay.

[0081]The external connection electrode and the surface wiring layer connected to the external connection electrode are formed at least to penetrate a layer (here, the first memory cell array

layer) vertically interposed by the memory cell array layer or/and the peripheral circuit layer. The signal line extraction electrode and the surface wiring layer connected to the signal line extraction electrode are formed at least to penetrate a layer (here, the first memory cell array layer) vertically interposed by the memory cell array layer or/and the peripheral circuit layer. Accordingly, when the plurality of memory cell array layers are stacked, it is possible to further reduce wiring lengths. Thus, it is possible to further prevent operation delay and improve reliability.

[0082]Further, the external connection electrode can have layout not connected to a memory cell and an external signal can be input from the external connection pad to the peripheral circuit layer without interposing the memory cell. In this way, it is possible to further prevent an adverse influence on operation delay or the like. Since the signal line extraction electrode is electrically connected to each memory cell array layer even in a route of non-connection to the memory cell, a signal line of each layer is connected to the signal line extraction electrode without interposing the memory cell. In this way, it is possible to further prevent an adverse influence on operation delay or the like.

[0083]The memory cell array layer does not include a substrate and it is not necessary to form silicon through electrode such as TSV. On the side of the second surface (the side of the

fourth surface) of the memory cell array layer, the source-side wiring layer is formed instead of forming a substrate. Accordingly, it is possible to connect the stacked memory cell array layer to any layer and it is possible to increase wiring regions without an increase in chip areas.

[0084]Further, the first source-side wiring layer can be used as the first source-line lead portion of the first source line SL. The second source-side wiring layer can be used as the second source-line lead portion of the second source line SL. In this way, by forming the source-side wiring layer on the side of the second surface (the side of the fourth surface) of the source line in the memory cell array which includes the memory cell string in which the columnar portion has the I shape, it is possible to efficiently reduce a wiring length from the source line to the signal line extraction electrode.

The signal line extraction electrode and the surface wiring layer of the second memory cell array layer may be formed to penetrate the second memory cell array layer, as in the first memory cell array layer. In this case, it is preferable to penetrate the second memory cell array layer in that a device structure can be common to the first memory cell array layer and the second memory cell array layer and characteristics such as stress occurring in the memory cell array layer can be achieved. In addition, it is preferable to penetrate the second memory cell array layer in that processes can be common

to the first memory cell array layer and the second memory cell array layer and the memory cell array layer can efficiently be manufactured.

[0085]In the first memory cell array layer or the second memory cell array layer, the bit line or the word line is led to the side of the first surface or the side of the third surface and the bit line or the word line is connected to the signal line extraction electrode. The first memory cell array layer is stacked so that the first surface faces the peripheral circuit layer and the second memory cell array layer is stacked so that the third surface faces the first memory cell array layer. That is, the first memory cell array layer and the second memory cell array layer are stacked so that the signal lines are led in the same direction and directions of the first memory cell array layer and the second memory cell array layer are uniform. In this way, since the bit lines and the word lines are led to the side (the lower side in FIG. 1) on which the peripheral circuit layer is formed and are stacked on the peripheral circuit layer, it is possible to reduce a dragging distance of the electrode layer, and thus it is possible to prevent an adverse influence on an operation speed.

[0086]When the first memory cell array layer and the second memory cell array layer are stacked to face each other without being uniform in the directions thereof, it is necessary to provide one of the memory cell array layers on, for example,

a tape, remove a substrate on the tape, and stack the memory cell array layer so that the surface on which the substrate is removed faces the peripheral circuit layer or the other memory cell array layer. When the first memory cell array layer and the second memory cell array layer are stacked so that the directions thereof are uniform, it is not necessary to use a tape or the like. That is, the memory cell array layer can be formed by stacking the memory cell array layer formed on the substrate on the peripheral circuit layer so that the front surface of the substrate is upward and removing the substrate. Accordingly, it is preferable to stack the first memory cell array layer and the second memory cell array layer so that the directions thereof are uniform in that the first memory cell array layer and the second memory cell array layer are easily formed without using a tape or the like.

[0087](Second Embodiment)

Next, a semiconductor memory device according to a second embodiment will be described. The basic configuration is the same as that of the first embodiment. Therefore, the matters described in the first embodiment will not be described.

[0088]FIG. 12 is a schematic sectional view illustrating the semiconductor memory device according to the second embodiment. In FIG. 12, one memory cell array layer is further stacked on the semiconductor memory device in FIG. 1. The peripheral circuit layer 100, the first memory cell array layer 200, the

second memory cell array layer 300, and the third memory cell array layer 400 are formed in order from the lower side.

[0089]Here, as illustrated in FIG. 12, in the stacked second memory cell array layer 300, a wiring layer 71 connected to a memory string MS3 is formed between a third surface wiring layer 38b formed on the third surface Sb1 and a fourth surface wiring layer 39b formed on the fourth surface Sb2. That is, the second memory cell array layer 300 is connected to the upper and lower memory cell array layers by the wiring layer 71 via the memory string MS3.

[0090]FIG. 13 is a circuit diagram of the semiconductor memory device according to the second embodiment. FIG. 13 illustrates a part of a circuit of the memory string MS3 connected to the wiring layer 71. A plurality of memory cells are formed and some of the memory cells are not illustrated. In the plurality of memory cells, the drain-side select transistor STD and the source-side select transistor STS are formed and an array layer ID formed for each memory cell array layer is stored. The circuit of the memory string MS3 functions as a part of an array layer selection circuit selecting an array layer.

[0091]FIG. 14 is a block diagram illustrating a configuration of a system of the semiconductor memory device according to the second embodiment. FIG. 14 illustrates the configuration of the system of the semiconductor memory device including the

array layer selection circuit formed in the memory string MS3 connected to the wiring layer 71.

[0092]In each memory cell array layer, an address line and an array layer select signal line are input as signal lines. In the memory cell array layer, whether the memory cell array layer is selected is determined in accordance with the array layer select signal line and the stored array layer ID and the address line is input to a memory cell array.

[0093]By forming the semiconductor memory device in this way, the memory cell array layer can be selected using a transistor and a memory cell inside the memory string MS3 without individually selecting the memory cell array using each signal line. Even in the semiconductor memory device including the plurality of stacked memory cell array layers, it is possible to considerably reduce the number of wirings.

[0094]In this way, each memory cell array layer may be connected to the upper and lower memory cell array layers using the wiring layer 71 for each memory block or memory area of the second memory cell array layer. By forming the semiconductor memory device in this way, the memory area or the memory block can be selected using each transistor and each memory cell in each memory string MS. Even in the semiconductor memory device including the plurality of stacked memory cell array layers, it is possible to considerably reduce the number of wirings.

[0095]The embodiments have been described with reference to

the drawings. However, the present disclosure is not limited thereto.

[0096]In the present disclosure, the example in which the circuit board is contained has been described. However, a case in which only the memory cell array layers are stacked is also included in the scope of the present disclosure.

[0097]Various design changes in the configuration of the memory cell array for realizing the present disclosure can be made by those skilled in the art and are included in the scope of the present disclosure without departing from the gist of the present disclosure.

[0098]According to still another aspect of the present disclosure, a semiconductor memory device including 3-dimensional memory cell arrays with different configurations is provided.

[0099]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

5 a peripheral circuit layer that includes a circuit board, a control circuit formed on a circuit formation surface of the circuit board, and a circuit-side wiring layer formed on the circuit formation surface of the circuit board and electrically connected to the control circuit;

10 a first memory cell array layer which includes a first surface and a second surface opposite to the first surface and does not include a first substrate and which includes a plurality of first memory cells arranged 3-dimensionally in a memory cell array region, a first signal line extraction electrode, a first external connection electrode formed outside  
15 the memory cell array region when viewed in a direction vertical to the first surface, and a first surface wiring layer and a second surface wiring layer connected to the first signal line extraction electrode and the first external connection electrode and formed in the first and second surfaces, respectively, in  
20 which the first surface is stacked to face the peripheral circuit layer, and the circuit-side wiring layer and the first surface wiring layer are bonded; and

a second memory cell array layer which includes a third surface and a fourth surface opposite to the third surface and  
25 does not include a second substrate and which includes a plurality of second memory cells arranged 3-dimensionally in the memory cell array region, a second signal line extraction electrode, a second external connection electrode formed outside the memory cell array region when viewed in a direction vertical  
30 to the third surface, and a third surface wiring layer and a fourth surface wiring layer connected to the second signal line extraction electrode and the second external connection electrode and formed in the third and fourth surfaces,

respectively, in which the third surface is stacked to face the first memory cell array layer, and the second surface wiring layer and the third surface wiring layer are bonded.

- 5     2.     The semiconductor memory device according to claim 1,  
          wherein the circuit-side wiring layer and the first  
          surface wiring layer are directly bonded and the second surface  
          wiring layer and the third surface wiring layer are directly  
          bonded.

10

3.     The semiconductor memory device according to claim 1 or 2,  
          wherein the plurality of first memory cells include a  
          first stacked body in which a plurality of insulating layers and  
          a plurality of electrode layers are alternately stacked and  
15     first columnar portions extending in a stacking direction of the  
          first stacked body, a first bit line is electrically connected  
          to the first columnar portion on a side of the first surface, a  
          first source line is electrically connected to the first  
          columnar portion on a side of the second surface, and a first  
20     source-side wiring layer is formed to be closer to the side of  
          the second surface than the first source line.

4.     The semiconductor memory device according to any one of  
          the preceding claims,

- 25     wherein the plurality of second memory cells include a  
          second stacked body in which a plurality of insulating layers  
          and a plurality of electrode layers are alternately stacked and  
          second columnar portions extending in a stacking direction of  
          the second stacked body, a second bit line is electrically  
30     connected to the second columnar portion on a side of the third  
          surface, a second source line is electrically connected to the  
          second columnar portion on a side of the fourth surface, and a

second source-side wiring layer is formed to be closer to the side of the fourth surface than the second source line.

5. The semiconductor memory device according to claim 1 or 2,  
5 wherein the plurality of first memory cells include a first stacked body in which a plurality of insulating layers and a plurality of electrode layers are alternately stacked and first columnar portions extending in a stacking direction of the first stacked body, a first bit line is electrically connected  
10 to the first columnar portion on a side of the first surface, a first source line is electrically connected to the first columnar portion on a side of the second surface, and a first source-side wiring layer is formed to be closer to the side of the second surface than the first source line,  
15 the plurality of second memory cells include a second stacked body in which a plurality of insulating layers and a plurality of electrode layers are alternately stacked and second columnar portions extending in a stacking direction of the second stacked body, a second bit line is electrically connected  
20 to the second columnar portion on a side of the third surface, a second source line is electrically connected to the second columnar portion on a side of the fourth surface, and a second source-side wiring layer is formed to be closer to the side of the fourth surface than the second source line, and  
25 the first source-side wiring layer of the first memory cell array layer is connected to the second bit line of the second memory cell array layer inside the memory cell array region when viewed in the direction vertical to the first surface.

30

6. The semiconductor memory device according to any one of the preceding claims,

wherein the second surface wiring layer and the third surface wiring layer respectively connected to the first signal line extraction electrode and the second signal line extraction electrode are formed inside the memory cell array region.

5

7. The semiconductor memory device according to any one of the preceding claims, further comprising:

at least one another memory cell array layer that is stacked to face the second memory cell array layer, thereby  
10 including three or more layers of the plurality of memory cell array layers.

8. The semiconductor memory device according to any one of the preceding claims,

15 wherein in the first memory cell array layer or the second memory cell array layer, a memory string that includes a memory cell storing an array layer ID and a transistor selecting the first memory cell array layer or the second memory cell array layer as a part of an array layer select circuit is formed, and  
20 the memory string is electrically connected to the first signal line extraction electrode of the first memory cell array layer or the second signal line extraction electrode of the second memory cell array.

25 9. The semiconductor memory device according to claim 7,  
wherein in at least one memory cell array layer among the plurality of memory cell array layers, a memory string that includes a memory cell storing an array layer ID and a transistor selecting the memory cell array layer as a part of an  
30 array layer select circuit is formed.

10. The semiconductor memory device according to claim 9,

wherein the plurality of memory cell array layers are at least three memory cell array layers and a part of the array layer select circuit is formed in one memory cell array layer vertically interposed between other memory cell array layers among the plurality of memory cell array layers.

11. The semiconductor memory device according to claim 9 or 10, wherein a part of the array layer select circuit is formed for each memory area or memory block of at least one layer of the memory cell array layers.

12. A semiconductor memory device comprising:  
a plurality of memory cell array layers that include a first surface and a second surface opposite to the first surface and do not include a substrate and that include a plurality of memory cells arranged 3-dimensionally in a memory cell array region and a surface wiring layer embedded in the first surface or/and the second surface,

wherein the surface wiring layer of each of the memory cell array layers is formed to overlap an adjacent surface wiring layer when viewed in a direction vertical to the first surface, and the surface wiring layers are bonded to each other so that the plurality of memory cell array layers are stacked, and

wherein in at least one memory cell array layer among the plurality of memory cell array layers, a memory string that includes a memory cell storing an array layer ID and a transistor selecting the memory cell array layer as a part of an array layer select circuit is formed.

13. The semiconductor memory device according to claim 12, wherein the plurality of memory cell array layers are at least three memory cell array layers and a part of the array

layer select circuit is formed in one memory cell array layer vertically interposed between other memory cell array layers among the plurality of memory cell array layers.

- 5 14. The semiconductor memory device according to claim 12,  
wherein a part of the array layer select circuit is formed for each memory area or memory block of at least one layer of the memory cell array layers.