Description

Title of the invention: Piezoelectric-on-insulator (POI) substrate and method for producing a piezoelectric-on-insulator (POI) substrate

[001]. The invention relates to a piezoelectric-on-insulator (POI) substrate comprising, in this order, a support substrate, a trapping structure, a dielectric layer and a piezoelectric layer, and also to a process for manufacturing such a POI substrate.

[002]. Such substrates are known in the prior art, for example a POI substrate comprising a single-crystal silicon substrate, a polycrystalline silicon trapping structure, a silicon oxide layer and a piezoelectric layer, in particular a lithium tantalate (LTO) or lithium niobate (LNO) layer. The trapping structure allows losses linked to parasitic conduction effects at the interface between the support substrate and the dielectric layer to be reduced. Specifically, the trapping layer, which is inserted between the support substrate and the dielectric layer, serves to reduce the lifetime of the charges in this region.

[003]. However, it is observed that, during heat treatments in the context of or subsequent to the manufacture of the POI substrates, metal elements of the piezoelectric layer, such as lithium, can diffuse through the dielectric layer and the trapping structure as far as the interface with the support substrate. The accumulation of these metal elements reduces the performance qualities of the trapping structure and the suppression of parasitic currents is thus negatively affected.

[004]. It is possible to increase the thickness of the trapping layer to increase the number of traps available. However, in this case, parasitic modes are seen in devices using the POI substrate, such as filters, sensors etc.

[005]. The object of the invention is thus to increase the number of traps with less risk of parasitic effects.

[006]. According to an aspect of the present disclosure, there is provided a piezoelectric-on-insulator (POI) substrate comprising: a support substrate, in particular a silicon-based substrate, a piezoelectric layer, in particular a layer of lithium tantalate (LTO) or of lithium niobate (LNO), a dielectric layer, in particular a silicon oxide layer, sandwiched between the piezoelectric layer and the support substrate, and a trapping structure sandwiched between the dielectric layer and the support substrate, comprising a first trapping layer based on polycrystalline or amorphous or porous silicon, preferably based on polycrystalline silicon, and the trapping structure comprises a second trapping layer based on silicon carbide, characterized in that the first trapping layer is positioned between the support substrate and the second trapping layer.

[007]. The addition of a second trapping layer with a different material in the trapping structure allows the number of traps to be increased, without having to increase the total thickness of the trapping structure to the same extent as would be necessary in the case of a single-material trapping structure.

[008]. According to one embodiment, the second trapping layer may be based on silicon carbide. A second layer based on silicon carbide allows efficient reduction of parasitic currents.

[009]. According to one embodiment, the second trapping layer based on silicon carbide may be thinner than the first layer. Thus, the provision of a thinner silicon carbide layer allows the number of traps to be increased, while at the same time limiting the appearance of parasitic modes due to the presence of the trapping structure, notably in comparison with a single-material silicon-based trapping layer containing the same number of traps.

[0010]. According to one embodiment, the second trapping layer based on silicon carbide may have a thickness of less than or equal to 500 nm, in particular a thickness of less than or equal to 200 nm, more particularly less than or equal to 50 nm. Even at such low thicknesses, there is a sufficient increase in the number of traps.

[0011]. According to one embodiment, the first silicon-based trapping layer may have a thickness of less than or equal to 2 μm, in particular less than or equal to 1 μm. By using a second trapping layer, it becomes possible to keep the thickness of the first trapping layer sufficiently low. Thus, parasitic modes due to this layer cannot develop, or at least their contribution remains negligible.

[0012]. According to one embodiment, the second trapping layer may be formed directly on the first trapping layer. A compact structure may thus be maintained.

[0013]. According to one embodiment, the first trapping layer is positioned between the support substrate and the second trapping layer. This facilitates the formation of the trapping structure, as a silicon carbide layer is deposited at a lower temperature than a silicon layer.

[0014]. According to one embodiment, the trapping structure comprises only the first trapping layer and the second trapping layer.

[0015]. According to one embodiment, the trapping structure is arranged directly on the substrate and the dielectric layer is arranged directly on the trapping structure.

[0016]. According to another aspect of the present disclosure, there is provided a process for manufacturing a piezoelectric-on-insulator (POI) substrate as described above and comprising the steps of: providing a support substrate, in particular a silicon-based substrate, providing a substrate comprising a piezoelectric layer, in particular a substrate comprising lithium tantalate (LTO) or lithium niobate (LNO), forming a trapping structure over the support substrate, forming a dielectric layer, in particular a silicon oxide layer, over the piezoelectric substrate and/or over the trapping structure, assembling the substrate comprising a piezoelectric layer with the support substrate such that the dielectric layer and the trapping structure are sandwiched between the piezoelectric layer and the support substrate, characterized in that the formation of the trapping structure involves forming a first layer based on

polycrystalline or amorphous or porous silicon on the support substrate, preferably based on polycrystalline silicon, and, subsequently, forming a second trapping layer based on silicon carbide.