

STORAGE DEVICES THAT SUPPORT CACHED PHYSICAL ADDRESS VERIFICATION AND METHODS OF OPERATING SAME

REFERENCE TO PRIORITY APPLICATIONS

[0001] This application claims priority to Korean Patent Application Nos. 10-2018-0019784, filed February 20, 2018, and 10-2018-0064106, filed June 4, 2018, in the Korean Intellectual Property Office, the disclosures of which are hereby incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to storage devices and methods of operating same.

BACKGROUND

[0003] In order to read data stored in a storage device including a flash memory, a host may transfer a logical block address (LBA) of the data to be read to the storage device. Then, after the storage device converts the LBA received from the host into a physical address (PA) for accessing the flash memory, for example, using an FTL (Flash Translation Layer), the storage device may provide the data, which is addressed to the PA, to the host.

[0004] In another situation, the host may include a cache table to cache information about the PA used in the storage device. Based on this configuration, the host transmits the LBA and the cached PA mapped to the LBA to the storage device, and the storage device may directly access the flash memory, using the cached PA received from the host, without requiring conversion of the LBA into the PA.

[0005] However, in this latter situation, since the PA cached in the host is not guaranteed to always be valid, the storage device needs to check whether the PA received from the host has a valid value in a LBA-PA mapping relation.

SUMMARY

[0006] Aspects of the present disclosure provide a storage device for checking the validity of a cached PA provided from a host in a simple and efficient manner, in an architecture in which a host caches a PA (Physical Address) of a storage device.

[0007] Aspects of the present disclosure also provide a method for operating a storage device for checking the validity of a cached PA provided from a host in a simple and efficient manner, in an architecture in which the host caches the PA of the storage device.

[0008] The aspects of the present disclosure are not restricted those mentioned above and another aspect which is not mentioned will be clearly understood by a person skilled in the art from the description below.

[0009] According to an aspect of the present disclosure, there is provided a storage device including a descramble module which receives a read command including logical block address (LBA) information and first meta information from a host, and descrambles the first meta information to acquire first signature information and first physical address (PA) information for accessing a flash memory. A compare module is provided to compare a value of the first signature information with a value of second signature information (e.g., stored in advance) to determine whether or not the value of the first signature information and the value of second signature information are equal to each other. An access module is provided, which accesses a data region of the flash memory, using the first PA information, when the value of the first signature information and the value of the second signature information are equal to each other.

[0010] According to another aspect of the present disclosure, there is provided a storage device including a descramble module which receives a read command including logical block address (LBA) information and first meta information from a host, and descrambles the first meta information to acquire first signature information and first physical address (PA) information for accessing a flash memory. A compare module is provided, which compares a value of the first signature information with a value of second signature information stored in advance to determine the validity of the first PA information.

[0011] According to another aspect of the present disclosure, there is provided a storage device including a descramble module which receives a read command including logical block address (LBA) information and first meta information from a host, and descrambles the first meta information to acquire first signature information and first physical address (PA) information for accessing a flash memory. A compare module is provided, which compares a value of the first signature information with a value of second signature information in a meta region of the flash memory to determine validity of the first PA information.

[0012] According to another aspect of the present disclosure, there is provided a method for operating a storage device, which includes receiving a read command including logical block address (LBA) information and first meta information from a host, and descrambling the first meta information to acquire first signature information and first physical address (PA) information for accessing the flash memory. An operation is also performed to compare a value of the first signature information with a value of the second signature information stored in advance to determine validity of the first PA information.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The above and other aspects and features of the present disclosure will become more apparent by describing in detail example embodiments thereof with reference to the attached drawings, in which:

[0014] FIG. 1 is a block diagram that illustrates a semiconductor system according to an embodiment of the present disclosure;

[0015] FIG. 2 is a detailed block diagram that illustrates a host and a storage device according to an embodiment of the present disclosure;

[0016] FIG. 3 is a schematic diagram that illustrates a sequence of operations performed by the host and storage device of FIG. 2, according to embodiments of the present disclosure;

[0017] FIG. 4 is a schematic diagram for explaining an embodiment of a meta region of FIG. 2;

[0018] FIG. 5 is a schematic diagram that illustrates operations performed by the scramble module of FIG. 2;

[0019] FIG. 6 is a block diagram that illustrates a configuration and operation of a host and a storage device according to an embodiment of the present disclosure;

[0020] FIG. 7 is a block diagram that illustrates a configuration and operation of the host and the storage device according to an embodiment of the present disclosure;

[0021] FIG. 8 is a block diagram that illustrates a configuration and operation of the host and the storage device according to an embodiment of the present disclosure;

[0022] FIG. 9 is a block diagram that illustrates a configuration and operation of the host and the storage device according to an embodiment of the present disclosure;

[0023] FIG. 10 is a block diagram that illustrates a configuration and operation of the host and the storage device according to an embodiment of the present disclosure;

[0024] FIG. 11 is a block diagram that illustrates a configuration and operation of the host and the storage device according to an embodiment of the present disclosure;

[0025] FIG. 12 is a block diagram that illustrates a configuration and operation of the host and the storage device according to an embodiment of the present disclosure;

[0026] FIG. 13 is a schematic diagram for explaining an example of the meta region of FIG. 12; and

[0027] FIG. 14 is a block diagram that illustrates a configuration and operation of the host and the storage device according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0028] The present invention now will be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout.

[0029] It will be understood that, although the terms first, second, third, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

[0030] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the present invention. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprising", "including", "having" and variants thereof, when used in this specification, specify the presence of stated features, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, steps, operations, elements, components, and/or groups thereof. In contrast, the term "consisting of" when used in this specification, specifies the stated features, steps, operations, elements, and/or components, and precludes additional features, steps, operations, elements and/or components.

[0031] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the present invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0032] FIG. 1 is a schematic diagram for explaining a semiconductor system according to an embodiment of the present disclosure. Referring to FIG. 1, a semiconductor system 1 according to an embodiment of the present disclosure includes a host 100 and a storage device 200. In some embodiments of the present

disclosure, the host 100 and the storage device 200 may be connected to each other through an electric interface, such as a UFS (Universal Flash Storage), SCSI (Small Computer System Interface), SAS (Serial Attached SCSI), SATA (Serial Advanced Technology Attachment), PCIe (Peripheral Component Interconnect Express), eMMC (embedded MultiMediaCard), FC (Fiber Channel), ATA (Advanced Technology Attachment), IDE (Integrated Drive Electronics), USB (Universal Serial Bus), and IEEE 1394 (Firewire). However, the scope of the present disclosure is not limited thereto, and may be applied to another type of interface that allows data to be transmitted and received between the host 100 and the storage device 200.

[0033] Hereinafter, for the sake of clarity and convenience of explanation throughout the core of the present disclosure, the description will be given assuming that the host 100 and the storage device 200 are electrically coupled/connected to each other via the UFS electrical interface, the host 100 is a UFS host, and the storage device 200 is a UFS memory device, but the scope of the present disclosure is not limited thereto and is applicable to other types of storage, which use other types of interfaces including the above-described electrical interface.

[0034] As shown by FIG. 1, the host 100 includes an application 110, a driver 120, a host controller 130, and a UIC (Universal Flash Storage Interconnection Layer) 140, which operates as a host interface. In some embodiments of the present disclosure, the host 100 may further include a buffer memory. The buffer memory may be used as a main memory of the host 100, and/or may be used as a cache memory, a temporary memory or the like for temporarily storing the data. In some embodiments of the present disclosure, the buffer memory may include volatile memory including DRAM (Dynamic Random Access Memory), but the scope of the present disclosure is not limited thereto.

[0035] The application 110 may control the semiconductor system 1 on the basis of a set of commands which is executed by the host 100 and can be used in the semiconductor system 1. The driver 120 may drive the storage device 200 connected to the host 100. For example, the driver 120 may: (i) receive a command for controlling the storage device 200 from the application 110, (ii) process the command

using the host controller 130, and then (iii) provide the processing result thereof to the application 110. The application 110 and the driver 120 may be implemented in hardware or software, or as a combination of hardware/software, but the scope of the present disclosure is not limited thereto.

[0036] The host controller 130 controls the overall operation inside the host 100. For example, the host controller 130 may transmit the data stored in the buffer memory to the storage device 200 through the host interface 140, in response to a write command received from the driver 120. Further, the host controller 130 may also receive data from the storage device 200 through the host interface 140, in response to a read command received from the driver 120.

[0037] The host interface 140 may exchange data with the UIC 240 corresponding to the device interface of the storage device 200 through the data lines DIN, DOUT. Alternatively, the host interface 140 may provide the UIC 240 of the storage device 200 with a reference clock REFCLK that may be used for at least a partial operation of the storage device 200. In some embodiments of the present disclosure, the UIC 140 of the host 100 and the UIC 240 of the storage device 200 handle the connection between the host 100 and the storage device 200 and may adopt, for example, MIPI UniPro or MIPI M-PHY.

[0038] As shown, the storage device 200 can include a device controller 230, a UIC 240, and a non-volatile memory (NVM) 250. The device controller 230 controls the overall operation inside the device 230. For example, the device controller 230 may perform operations of writing, reading or erasing the data requested by the host 100 for the non-volatile memory 250. Therefore, like the host 100, the storage device 200 may further include a buffer memory.

[0039] The non-volatile memory 250 may include a flash memory, an MRAM (Magnetoresistive Random Access Memory), a PRAM (Phase-change Random Access Memory), FeRAM (Ferroelectric Random Access Memory) and the like, but the scope of the present disclosure is not limited thereto. However, for the sake of convenience of explanation, the non-volatile memory 250 will be described as having a flash-type memory architecture.

[0040] FIG. 2 is a block diagram for explaining a host and a storage device according to an embodiment of the present disclosure. FIG. 3 is a block diagram for explaining an operation example of the descramble module 232 of FIG. 2. FIG. 4 is a block diagram for explaining an embodiment of the meta region 254 of FIG. 2. And, FIG. 5 is a block diagram for explaining an operation example of the scramble module 238 of FIG. 2.

[0041] Referring to FIG. 2, the host 100 according to an embodiment of the present disclosure includes a command generate module 132 and a cache table 134.

[0042] In some embodiments of the disclosure, the command generate module 132 may be implemented as part of the host controller 130 of FIG. 1, but the scope of the disclosure is not limited thereto, and the command generate module 132 may be implemented as a separate module electrically connected to the host controller 130. On the other hand, in some embodiments of the present disclosure, the cache table 134 is loaded into the buffer memory described in FIG. 1, and the host controller 130 or the command generate module 132 may access the cache table 134 through the buffer memory.

[0043] The command generate module 132 generates a data access command including, for example, a read command READ CMD and a write command WRITE CMD, and transmits the data access command to the storage device 200. For example, the read command READ CMD corresponds to a command to provide data stored in the flash memory 250 of the storage device 200 to the host 100, and the write command WRITE CMD corresponds to a command to store the data, which is provided to the device 200 together with the write command WRITE CMD by the host 100, to the flash memory 250.

[0044] Specifically, when the command generate module 132 transmits the read command READ CMD to the storage device 200, the read command READ CMD includes LBA (Logical Block Address) information on the data that the host 100 intends to read. For example, in order for the host 100 to read the data addressed to the LBA#5, when the host 100 transmits the LBA information having the value of LBA#5 as the read command READ CMD to the device 200, the device 200 determines the

actual PA (Physical Address), which is mapped to the LBA#5, and accesses the flash memory 250 based on the PA.

[0045] The PA information mapped to the LBA information in this way is cached through the cache table 134 of the host 100. For example, when PA#5 mapped to LBA#5 is determined as a value of 15 in the device 200, the device 200 may provide information, in which the PA#5 mapped to LBA#5 is 15, to the host 100. Then, the host 200 inserts information, in which PA#5 mapped to LBA#5 is 15, into the cache table 134. Thereafter, when generating the read command READ CMD for reading the data addressed to the LBA#5, the command generate module 132 of the host 200 may include the information on PA#5 of 15 in the read command READ CMD, and may transmit the information to the device 200. In this way, the device 200 that has received the cached PA information on the host 100 may directly and advantageously use the cached PA information, but without requiring conversion of LBA into PA in order to access the data.

[0046] However, the cache table 134 managed in the host 100 may not always have latest LBA-PA mapping information. For example, while the value of PA#5 mapped to LBA#5 is cached in the cache table 134, the LBA-PA mapping relation of the device 200 may change as much as possible. Therefore, when the device 200 receives the provision of the cached PA information from the host 200, it is necessary to determine the validity of the cached PA information.

[0047] Referring to FIGS. 2 and FIG. 3, in combination, to this end (i.e., determining validity), in the present embodiment, the command generate module 132 generates a read command READ CMD including LBA information LBA, 300a and first meta information META_H, 300b. Here, the LBA information LBA includes an LBA value of data to be read by the host 100, for example, the value of LBA#5.

[0048] The first meta information META_H is input in the cache table 134, and then may be provided to the command generate module 132. The first meta information META_H includes first signature information SGN_H and first PA information PA_H. In particular, the first signature information SGN_H may include a value used for the

device 200 to determine the validity of the first PA information PA_H, and the first PA information PA_H includes the PA value mapped to the LBA information LBA.

[0049] In the present embodiment, the first meta information META_H is scrambled data generated by scrambling the first signature information SGN_H and the first PA information PA_H, and may be generated in the device 200 and transmitted to the host 100. Therefore, the command generate module 132 transmits the read command READ CMD including the LBA information LBA and the first meta information META_H provided from the cache table 134 to the device 200.

[0050] Alternatively, the storage device 200 according to an embodiment of the present disclosure includes a descramble module 232, a compare module 234, an access module 236, and a scramble module 238. And, in some of these embodiments, the descramble module 232, the compare module 234, the access module 236 and the scramble module 238 may be implemented as a part of the device controller 230, but the scope of the present disclosure is not limited thereto, and they may be implemented as another module electrically connected to the device controller 230.

[0051] The descramble module 232 receives the read command READ CMD from the host 100, and descrambles the first meta information META_H included in the read command READ CMD to acquire the first signature information SGN_H and the first PA information PA_H for accessing the flash memory 250. For example, as shown by FIG. 3, the descramble module 232 may use the LBA information LBA and global signature information GSGN (described hereinbelow) to descramble the first meta information META_H. However, in some embodiments of the present disclosure, the meta data 310 in which the first meta information META_H is descrambled may further include parity information 310a, in addition to the first signature information SGN_H 310b and the first PA information PA_H 310c.

[0052] The compare module 234 (see, e.g., FIG. 2) compares the value of the first signature information SGN_H with the value of the previously stored second signature information SGN_D to determine the validity of the first PA information PA_H. To this end, in some embodiments of the present disclosure, the compare module 234 may compare the value of the first signature information SGN_H with the value of the

previously stored second signature information SGN_D to determine whether the values are equal to each other.

[0053] Specifically, when the value of the first signature information SGN_H is equal to the value of the second signature information SGN_D, the compare module 234 may determine that the value of the first PA information PA_H is valid. Alternatively, when the value of the first signature information SGN_H and the value of the second signature information SGN_D are different from each other, the compare module 234 may determine that the value of the first PA information PA_H is invalid.

[0054] When it is determined that the first PA information PA_H is valid, the access module 236 may access the data region 252 of the flash memory 250, using the first PA information PA_H. But, when it is determined that the first PA information PA_H is invalid, the access module 236 loads the second PA information from the flash memory 250, and may access the data region 252, using the second PA information.

[0055] In particular, when the value of the first signature information SGN_H and the value of the second signature information SGN_D are equal to each other, the access module 236 may access the data region 252 of the flash memory 250, using the first PA information PA_H. But, when the value of the first signature information SGN_H and the value of the second signature information SGN_D are different from each other, the access module 236 may load the second PA information from the flash memory 250 and may access the data region 252, using the second PA information. Advantageously, by comparing the value of the first signature information SGN_H with the second signature information SGN_D in this manner, it is possible to inspect the validity of the cached PA in a simple and highly efficient manner.

[0056] The scrambling module 238 scrambles the second signature information SGN_D and the second PA information to generate second meta information META_D. That is, the scrambling module 238 may provide the second signature information SGN_D stored in the device 200 at that time and the efficient second PA information, as the second meta information META_D, to the cache table 134 of the host 100.

[0057] In particular, referring to FIG. 5 together, the scrambling module 238 may use the LBA information LBA and the global signature information GSGN to be described

later to scramble the second signature information SGN_D and the second PA information PA. On the other hand, in some embodiments of the present disclosure, the metadata 320 to be scrambled may further include parity information, in addition to the second signature information SGN_D and the second PA information PA.

[0058] The second signature information SGN_D may be stored in the meta region 254 of the flash memory 250. In this case, the compare module 234 may compare the value of the first signature information SGN_H with the value of the second signature information SGN_D stored in the meta region 254 to determine whether the values are equal to each other.

[0059] Referring now to FIGS. 1-4, the meta region 254 may include a plurality of meta regions, for example, a first meta region 2542 and a second meta region 2544. The first meta region 2542 may store the first meta region signature information SGN_D1 of the first LBA set. In other words, the first meta region 2542 may store first meta region signature information SGN_D1 having the same value (e.g., 1) in the first LBA set including LBA#1 to LBA#5. Also, the first meta region signature information SGN_D1 may also have the same value in PA#1 to PA#5 corresponding to LBA#1 to LBA#5.

[0060] The second meta region 2544 may store the second meta region signature information SGN_D2 of the second LBA set, which is distinguished from the first LBA set. In other words, the second meta region 2544 may store the second meta region signature information SGN_D2 having the same value (e.g., 5) in the second LBA set including LBA#6 to LBA#10. Also, the second meta region signature information SGN_D2 may also have the same value in PA#6 to PA#10 corresponding to LBA#6 to LBA#10.

[0061] The second signature information SGN_D stored in advance in the device 200 may be determined as the first meta region signature information SGN_D1 or the second meta region signature information SGN_D2 in accordance with the value of the LBA information LBA. For example, when the LBA information LBA corresponds to LBA#5, the second signature information SGN_D may be determined as the first meta region signature information SGN_D1, and when the LBA information LBA

corresponds to LBA#8, the second signature information SGN_D may be determined as the second meta region signature information SGN_D2.

[0062] In some embodiments of the present disclosure, the host 100 and the device 200 may transmit and receive the data access commands and the data to and from each other through the data lines DIN, DOUT described in FIG. 1. The operation of the storage device 200 according to various embodiments of the present disclosure will be described referring now to the embodiments of FIGS. 6 through 14.

[0063] FIG. 6 is a block diagram for explaining the operation of the host and the storage device according to an embodiment of the present disclosure. Referring to FIG. 6, in the present embodiment, the storage device 200 may generate the second meta information META_D of the LBA#5 and provide it to the cache table 134 of the host 100. First, it is assumed that the first meta region 2542 in the meta region 254 of the storage device 200 is a meta region corresponding to LBA#5. The scramble module 238 scrambles the first meta region signature information SGN_D1 (i.e., the second signature information SGN_D) of the first meta region 2542 and the second PA information to generate the second meta region information META_D.

[0064] For example, when the value of the first meta region signature information SGN_D1 of the first meta region 2542 on the current storage device 200 is 1 and the value of the second PA information stored in the first meta region 2542 is 15, the scramble module 238 performs scrambling on the assumption that the value of 15 of PA#5 mapped to LBA#5 is valid.

[0065] In particular, as described above, the scramble module 238 may generate the second meta information META_D, using the LBA information and the global signature information GSGN having a value of 10 together.

[0066] The second meta information META_D generated by the scramble module 238 may be transmitted to the host 100 and inserted into the cache table 134. As illustrated in FIG. 6, the cache table 134 may include a record including an LBA field 134a, a meta information field 134b, and a validity flag field 134c, but the scope of the present disclosure is not limited thereto, and the internal form of the record may be various. In the present embodiment, the validity flag field 134c has a first value (for

example, "V") in the sense that META#5 stored in the cache table 134 together with LBA#5 has the valid value.

[0067] FIG. 7 is a block diagram for explaining the operation of the host and the storage device according to the embodiment of the present disclosure. Referring to FIG. 7, in the present embodiment, the command generate module 132 of the host 100 generates the read command READ CMD including the LBA information 300a of the LBA#5 and the first meta information META_H, 300b provided from the cache table 134. Further, the command generate module 132 transmits the read command READ CMD to the storage device 200.

[0068] The descramble module 232 of the storage device 200 receives the read command READ CMD from the host 100, and descrambles the first meta information META_H to acquire the first signature information SGN_H and the first PA information PA_H for accessing the flash memory 250. In the present embodiment, it is assumed that the value of the first signature information SGN_H acquired by descrambling the first meta information META_H is 1, and the value of the first PA information PA_H is 15.

[0069] The compare module 234 of the storage device 200 compares the value of the first signature information SGN_H acquired by descrambling the first meta information META_H with the value of the second signature information SGN_D stored in advance. In this embodiment, assuming that the first meta region 2542 in the meta region 254 is a meta region corresponding to LBA#5, the compare module 234 compares 1 as the value of the first signature information SGN_H with 1 as the value of the first meta region signature information SGN_D1 (i.e., the second signature information META_H) to determine the validity of the first PA information PA_H acquired by descrambling the first meta information META_H.

[0070] Since the value of the first signature information SGN_H is the same as the value of the second signature information SGN_D, the access module 236 of the storage device 200 considers that the first PA information PA_H acquired by descrambling the first meta information META_H is valid, accesses the data region

252 of the flash memory 250 using the same, and transmits the accessed data to the host 100.

[0071] FIG. 8 is a block diagram for explaining the operation of the host and the storage device according to the embodiment of the present disclosure. Referring to FIG. 8, this embodiment is different from the embodiment of FIG. 7 in that the value of the second signature information SGN_D is changed to 2. As a reason for change in the value of the second signature information SGN_D, for example, there is a situation where the host 100 transmits the write command WRITE CMD to the storage device 200, a case where garbage collection is performed inside the storage device 200 and the like. This will be described later with reference to FIGS. 9 to 14.

[0072] Similarly to the embodiment of FIG. 7, the command generate module 132 of the host 100 generates the read command READ CMD including the LBA information 300a of the LBA#5 and the first meta information META_H, 300b provided from the cache table 134, and transmits the read command READ CMD to the storage device 200.

[0073] The descramble module 232 of the storage device 200 receives the read command READ CMD from the host 100, and descrambles the first meta information META_H to acquire the first signature information SGN_H, and the first PA information PA_H for accessing the flash memory 250. In the present embodiment, it is assumed that the value of the first signature information SGN_H acquired by descrambling the first meta information META_H is 1, and the value of the first PA information PA_H is 15.

[0074] The compare module 234 of the storage device 200 compares the value of the first signature information SGN_H acquired by descrambling the first meta information META_H with the value of the second signature information SGN_D stored in advance. In this embodiment, assuming that the first meta region 2542 in the meta region 254 is a meta region corresponding to LBA#5, the compare module 234 compares 1 as the value of the first signature information SGN_H with the 1 as the first meta region signature information SGN_D1 (i.e., the second signature information SGN_D) to

determine the validity of the first PA information PA_H acquired by descrambling the first meta information META_H.

[0075] Since the value of the first signature information SGN_H and the value of the second signature information SGN_D are different from each other, the access module 236 of the storage device 200 considers that the first PA information PA_H acquired by descrambling the first meta information META_H is invalid. As a result, the access module 236 accesses the data region 252, using the second PA information newly loaded from the flash memory 250, instead of the first PA information PA_H, and transmits the accessed data to the host 100.

[0076] FIG. 9 is a block diagram for explaining the operation of the host and the storage device according to the embodiment of the present disclosure. Referring to FIG. 9, in the present embodiment, the host 100 may transmit a write command WRITE CMD to the storage device 200. For example, the host 100 may transmit the LBA information of the data to be written and the data to be written to the storage device 200.

[0077] In such a case, since the LBA-PA mapping relation which was defined inside the storage device 200 is newly formed, the host 100 may invalidate the cached record, by changing the validity flag field 134c of the record in the cache table 134 to a second value (e.g., "IV"), while transmitting the write command WRITE CMD to the storage device 200.

[0078] In the present embodiment, the storage device 200 further includes a WMC management module 239. The WMC management module 239 is a module that manages the PA information and the signature information associated with the LBA information contained in the write command WRITE CMD, using the write map cache (WMC) table 260, when receiving the write command WRITE CMD from the host 100.

[0079] For example, when the write command WRITE CMD of LBA#5 is received from the host 100, the WMC management module 239 inserts the value of PA#5 newly determined while being associated with LBA#5, and the value obtained by changing (for example, increasing by 1) the first meta region signature information SGN_D1 of the first meta region 2542 corresponding to LBA#5, into the write map cache table 260.

As illustrated in FIG. 9, the write map cache table 260 may include a record including an LBA field 260a, a PA field 260b and a second signature information field 260c, but the scope of the present disclosure is not limited thereto, and the internal form of the record may be various.

[0080] FIG. 10 is a block diagram for explaining the operation of the host and the storage device according to an embodiment of the present disclosure. Referring to FIG. 10, in this embodiment, the command generate module 132 of the host 100 generates the read command READ CMD including the LBA information 300a of the LBA#5, and the first meta information META_H, 300b provided from the cache table 134. Further, the command generate module 132 transmits the read command READ CMD to the storage device 200.

[0081] The descramble module 232 of the storage device 200 receives the read command READ CMD from the host 100, and descrambles the first meta information META_H to acquire the first signature information SGN_H and the first PA information PA_H for accessing the flash memory 250. In the present embodiment, it is assumed that the value of the first signature information SGN_H acquired by descrambling the first meta information META_H is 2, and the value of the first PA information PA_H is 21.

[0082] The compare module 234 of the storage device 200 compares the value of the first signature information SGN_H acquired by descrambling the first meta information META_H with the value of the second signature information SGN_D stored in advance. Unlike the case of FIG. 7, in the present embodiment, the compare module 234 compares 2 as the value of the first signature information SGN_H with 2 as the value stored in the write map cache table 260 to determine the validity of the first PA information PA_H acquired by descrambling the first meta information META_H.

[0083] Since the value of the first signature information SGN_H is the same as the value of the second signature information SGN_D stored in the write map cache table 260, the access module 236 of the storage device 200 considers that the first PA information PA_H acquired by descrambling the meta information META_H is valid,

accesses the data region 252 of the flash memory 250 using the same, and transmits the accessed data to the host 100.

[0084] FIG. 11 is a block diagram for explaining the operation of the host and the storage device according to the embodiment of the present disclosure. Referring to FIG. 11, this embodiment is different from the embodiment of FIG. 10 in that the value of the first signature information SGN_H acquired by descrambling the first meta information META_H is 1, and the value of the first PA information PA_H is 15.

[0085] As in the embodiment of FIG. 10, the command generate module 132 of the host 100 generates the read command READ CMD including the LBA information 300a of the LBA#5 and the first meta information META_H, 300b provided from the cash table 134, and transmits the read command READ CMD to the storage device 200.

[0086] The descramble module 232 of the storage device 200 receives the read command READ CMD from the host 100, and descrambles the first meta information META_H to acquire the first signature information SGN_H and the first PA information PA_H for accessing the flash memory 250.

[0087] The compare module 234 of the storage device 200 compares the value of the first signature information SGN_H acquired by descrambling the first meta information META_H with the value of the second signature information SGN_D stored in advance. Unlike the case of FIG. 8, in this embodiment, the compare module 234 compares 1 as the value of the first signature information SGN_H, with 2 as the value stored in the write map cache table 260 to determine the validity of the first PA information PA_H acquired by descrambling the first meta information META_H.

[0088] Since the value of the first signature information SGN_H and the value of the second signature information SGN_D are different from each other (i.e., $1 \neq 2$), the access module 236 of the storage device 200 considers that the first meta information META_H acquired by descrambling the first PA information PA_H is invalid. As a result, the access module 236 accesses the data region 252, using the second PA information newly loaded from the flash memory 250, instead of the first PA information PA_H, and transmits the accessed data to the host 100.

[0089] FIG. 12 is a block diagram for explaining the operation of the host and the storage device according to the embodiment of the present disclosure, and FIG. 13 is a block diagram for explaining an example of the meta region of FIG. 12. Referring to FIG. 12, the garbage collection may be performed on the data region 252 of the storage device 250. The garbage collection may be performed in the entire regions of the data region 252, or may be performed in some regions. In this case, the previous LBA-PA mapping relation on the region of the data region 252 in which the garbage collection is executed may be entirely invalidated.

[0090] In the present embodiment, the storage device 250 may further include a garbage collection module (GC module) 270. When the garbage collection is performed on at least a part of the data region 252, the garbage collection module 270 changes the value of the first meta region signature information SGN_D1 or the second meta region signature information SGN_D2. For example, referring to FIG. 12 and FIG. 13 together, it is possible to know that the values of PA#1 to PA#5 for LBA#1 to LBA#5 corresponding to the first meta region 2542 are changed, and the garbage collection module 270 changes the value of the first meta region signature information SGN_D1 from 1 to 2, accordingly.

[0091] As a result, the cached PA provided from the host 100 for the LBA affected by the garbage collection is handled as an inevitably invalid value, and thereafter, the storage device 250 accesses the data region 252, using the second PA information newly loaded from the flash memory 250.

[0092] FIG. 14 is a block diagram for explaining the operation of the host and the storage device according to the embodiment of the present disclosure. Referring to FIG. 14, as in the embodiment of FIG. 12, when the garbage collection is performed on the entire region or a partial region of the data region 252 of the storage device 250 and the garbage collection module 270 changes the value of the first meta region signature information SGN_D1 or the second meta region signature information SGN_D2, an overflow may occur.

[0093] For example, when the value of the first meta region signature information SGN_D1 is expressed by n bits, values that the first meta region signature information

SGN_D1 may have are in the range of 0 to 2^n-1 . When n is 4, the values that the first meta region signature information SGN_D1 may have are in the range of 0 to 7.

[0094] When the garbage collection module 270 increases by 1 to change the value of the first meta region signature information SGN_D1, if the value is a value of 2^n out of range, the value may not be expressed by n bits. Therefore, when the value of the first meta region signature information SGN_D1 or the second meta region signature information SGN_D2 is changed and an overflow condition occurs. In response, the garbage collection module 270 resets the value of the changed first meta region signature information SGN_D1 or the second meta region signature information SGN_D2 to, for example, 0. In addition, when the value of the first meta region signature information SGN_D1 or the second meta region signature information SGN_D2 is changed and an overflow occurs, the garbage collection module 270 changes the value of the global signature information GSGN to another value. For example, the value of the global signature information GSGN is changed from 10 to 50, as shown by FIG. 14.

[0095] Thus, as described above, and according to various embodiments of the present disclosure, it is possible to inspect the validity of the cached PA provided by the host in a simple and highly efficient manner, in the architecture in which the host operates to cache PAs of the storage device.

[0096] In concluding the detailed description, those skilled in the art will appreciate that many variations and modifications may be made to the preferred embodiments without substantially departing from the principles of the present disclosure. Therefore, the disclosed preferred embodiments of the disclosure are used in a generic and descriptive sense only and not for purposes of limitation.

What is claimed is:

1. A storage device comprising:

a descramble module configured to descramble at least a portion of a read command, which includes logical block address (LBA) information and first meta information, into first signature information and first physical address (PA) information for accessing a memory,

wherein the first signature information is cached in a cache table;

a compare module configured to compare the first signature information against stored signature information to thereby determine an equivalency or discrepancy there between; and

an access module configured to use the first PA information to access a data region of the memory, upon determination of the equivalency by said compare module.

2. The storage device of claim 1, wherein said access module is further configured to load second PA information from the memory and access the data region using the second PA information, upon determination of the discrepancy by said compare module.

3. The storage device of claim 1 or claim 2, wherein the memory is a flash memory; wherein the stored signature information is second signature information; and wherein the flash memory includes a meta region which stores the second signature information.

4. The storage device of claim 3, wherein the meta region includes a first meta region and a second meta region; wherein the first meta region stores first meta region signature information on a first LBA set and the second meta region stores second meta region signature information on a second LBA set different from the first LBA set; and wherein the second signature information is equivalent to the first meta region signature information or the second meta region signature information in accordance with the value of the LBA information.

5. The storage device of claim 4, further comprising:

a garbage collection module (GC module) configured to change the value of the first meta region signature information or the second meta region signature information, when garbage collection is performed on at least a part of the data region.

6. The storage device of claim 5, wherein the flash memory further comprises a global signature information storage region which stores global signature information; wherein said garbage collection module is configured to reset the changed value of the first meta region signature information or the second meta region signature information, when: (i) the value of the first meta region signature information or the second meta region signature information is changed and an overflow occurs, and (ii) the garbage collection module changes the value of the global signature information to another value.

7. The storage device of claim 6, wherein said descramble module descrambles the first meta information, using the global signature information.

8. The storage device of claim 6 or claim 7, further comprising:

a scrambling module configured to scramble the second signature information and the second PA information associated with the second signature information using the global signature to thereby generate second meta information.

9. The storage device of any one of claims 1 to 8, further comprising:

a WMC management module configured to manage the PA information and the signature information associated with the LBA information included in a write command, using a write map cache (WMC) table, when the write command is received from a host.

10. The storage device of claim 9, wherein said compare module is configured to compare the value of the first signature information with the value of the second signature information stored in the write map cache table to thereby determine whether the value of the first signature information and the value of the second signature information are equal to each other.

11. A storage device comprising:

a descramble module configured to receive a read command including logical block address (LBA) information and first meta information from a host, and further configured to descramble the first meta information to acquire first signature information and first physical address (PA) information for accessing a flash memory, wherein the first signature information is cached in a cache table; and
a compare module configured to compare a value of the first signature information with a value of second signature information to determine the validity of the first PA information.

12. The storage device of claim 11, wherein the compare module determines that the value of the first PA information is valid when the value of the first signature information is equal to the value of the second signature information; and wherein the compare module determines that the value of the first PA information is invalid when the value of the first signature information is different from the value of the second signature information.

13. The storage device of claim 12, further comprising an access module configured to access a data region of the flash memory using the first PA information, when the first PA information is determined to be valid, and further configured to load second PA information from the flash memory and accesses the data region using the second PA information, when the first PA information is determined to be invalid.

14. The storage device of any of claims 11 to 13, wherein the flash memory includes a meta region which stores the second signature information, and wherein said compare module compares the value of the first signature information with the value of the second signature information stored in the meta region.

15. The storage device of claim 14, wherein the meta region includes a first meta region and a second meta region; wherein the first meta region stores first meta region signature information on a first LBA set; wherein the second meta region stores second meta region signature information on a second LBA set distinguished from the first LBA set; and wherein the second signature information is determined as the

first meta region signature information or the second meta region signature information in accordance with the value of the LBA information.

16. The storage device of any of claims 11 to 15, further comprising:

a WMC management module which manages the PA information and the signature information associated with the LBA information included in a write command, using a write map cache (WMC) table, when the write command is received from the host.

17. The storage device of claim 16, wherein the compare module is configured to compare the value of the first signature information with the value of the second signature information stored in the write map cache table.

18. A storage device comprising:

a descramble module configured to receive a read command including logical block address (LBA) information and first meta information from a host, and further configured to descramble the first meta information to acquire first signature information and first physical address (PA) information for accessing a flash memory, wherein the first signature information is cached in a cache table; and

a compare module configured to compare a value of the first signature information with a value of second signature information stored in advance in a meta region of the flash memory to thereby determine validity of the first PA information.

19. The storage device of claim 18, wherein the meta region includes a first meta region and a second meta region; wherein the first meta region stores first meta region signature information on a first LBA set; wherein the second meta region stores second meta region signature information on a second LBA set distinguished from the first LBA set; and wherein the second signature information is determined as the first meta region signature information or the second meta region signature information in accordance with the value of the LBA information.

20. The storage device of claim 18 or claim 19, wherein said compare module determines that the value of the first PA information is valid when the value of the first

signature information is equal to the value of the second signature information, and said compare module determines that the value of the first PA information is invalid when the value of the first signature information is different from the value of the second signature information.