NON-PLANAR TRANSITOR FIN FABRICATION

BACKGROUND

Embodiments of the present description generally relate to the field of microelectronic device fabrication and, more particularly, to the fabrication of non-planar transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 is a perspective view of non-planar transistors;

FIG. 2 illustrates a top plan view of a technique of implanting non-planar transistor fins, as known in the art.

FIG. 3 illustrates a side cross-sectional view of a technique of implanting non-planar transistor fins, as known in the art.

FIG. 4 illustrates a side cross-sectional view of depositing a conformal blocking layer on a plurality of non-planar transistor fin, according to an embodiment of the present description.

FIG. 5 illustrates a side cross-sectional view of a portion of the conformal blocking layer of FIG. 4 having been removed and the exposed non-planar transistor fins being implanted with a dopant, according to an embodiment of the present description.

FIG. 6 is flow diagram of a process of using a conformal block layer to implant selected non-planar transistor fins according to an embodiment of the present description.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the

various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

In the fabrication of non-planar transistors, such as tri-gate transistors and FinFETs, non-planar semiconductor bodies may be used to form transistors capable of full depletion with very small gate lengths (e.g., less than about 30 nm). These semiconductor bodies are generally fin-shaped and are, thus, generally referred to as transistor "fins". For example in a tri-gate transistor, the transistor fins have a top surface and two opposing sidewalls formed on a bulk semiconductor substrate or a silicon-on-insulator substrate. A gate dielectric may be formed on the top surface and sidewalls of the semiconductor body and a gate electrode may be formed over the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the sidewalls of the semiconductor body. Thus, since the gate dielectric and the gate electrode are adjacent to three surfaces of the semiconductor body, three separate channels and gates are formed. As there are three separate channels formed, the semiconductor body can be fully depleted when the transistor is turned on. With regard to finFET transistors, the gate material and the electrode only contact the sidewalls of the semiconductor body, such that two separate channels are formed (rather than three in tri-gate transistors).

Embodiments of the present description relate to the doping of fins within non-planar transistors, wherein a conformal blocking material layer may be used to achieve a substantially uniform doping throughout the non-planar transistor fins.

FIG. 1 is a perspective view of a number of non-planar transistors 100_1 and 100_2 (shown as "sets"), including a number gates formed on transistor fins, which are formed on a substrate. In an embodiment of the present disclosure, a substrate 102 may be a monocrystalline silicon substrate. The substrate 102 may also be other types of substrates, such as silicon-on-insulator ("SOI"), germanium, gallium arsenide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and the like, any of which may be combined with silicon.

Each of the non-planar transistors 100_1 and 100_2, shown as tri-gate transistors, includes transistor fins 112_1 and 112_2 which may have isolation regions 104, such as silicon oxide (SiO_2), between each of the transistor fins 112_1 and 112_2 as well as between the non-planar transistors 100_1 and 100_2 themselves. The isolation regions 104 may be formed by any known fabrication process, as will be understood to those skilled in the art.

Each of the transistor fins 112_1 and 112_2 may have a top surface 114_1 and 114_2 and a pair of laterally opposite sidewalls, sidewalls 116_1 and 116_2 and opposing sidewall 118_1 and 118_2, respectively.

As further shown in FIG. 1, at least one transistor gate 132_1, 132_2, 132_3 may be formed over each of the transistor fins 112_1 and 112_2, respectively. The transistor gates 132_1, 132_2, 132_3 may be fabricated by forming gate dielectric layers 134_1 and 134_2 on or adjacent to the transistor fin top surfaces 114_1 and 114_2 and on or adjacent to the transistor fin sidewalls 116_1 and 116_2 and the opposing transistor fin sidewalls 118_1 and 118_2. Gate electrodes 136_1, 136_2, 136_3 may be formed on or adjacent the gate dielectric layers 134_1 and 134_2, respectively. In one embodiment of the present disclosure, the transistor fins 112_1 and 112_2 run in a direction substantially perpendicular to the transistor gates 132_1, 132_2, 132_3, respectively.

The gate dielectric layers 134_1 and 134_2 may be formed from any well-known gate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials such as hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The gate dielectric

layers 134_1 and 134_2 can be formed by well-known techniques, such as by depositing a gate electrode material, such as chemical vapor deposition ("CVD"), physical vapor deposition ("PVD"), atomic layer deposition ("ALD"), and then patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

The gate electrodes 136_1, 136_2, 136_3 can be formed of any suitable gate electrode material. In an embodiment of the present disclosure, the gate electrodes 136_1, 136_2, 136_3 may be formed from materials that include, but are not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. The gate electrodes 136_1, 136_2, 136_3 can be formed by well-known techniques, such as by blanket depositing a gate electrode material and then patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

A source region and a drain region (not shown) may be formed in the transistor fins 112_1 and 112_2 on opposite sides of the gate electrodes 136_1, 136_2, 136_3, respectively. The source and drain regions may be formed by doping the transistor fins 112_1 and 112_2. As will be understood to those skilled in that art, doping is a process of introducing impurities into semiconducting materials for the purpose changing its conductivity and electronic properties. This is generally achieved by ion implantation of either P-type ions (e.g. boron) or N-type ions (e.g. phosphorus), collectively called "dopants".

In order to achieve a uniform doping along a height H (see FIG. 3) of the transistor fins 112_1 and 112_2, the dopants may be implanted into the transistor fins 112_1 and 112_2 at an angle (shown as arrows 144 and 146 of FIGs. 3 and 5) from either side of the transistor fins 112_1 and 112_2 (e.g. toward sidewalls $116_1/116_2$ and toward sidewalls $118_1/118_2$). By implanting the dopants at an angle from either side of the transistor fins 112_1 and 112_2, the dopants are primarily implanted through the laterally opposite sidewalls pairs, e.g. the transistor fin sidewalls 116_1 and 118_1 and opposing transistor fin sidewalls 116_2 and 118_2 (see FIG. 1). As will be understood to those skilled in the art, identical implantation from each side of the transistor fins 112_1 and 112_2, may achieve uniform doping across the height H (see FIG. 3) of the transistor fins 112_1 and 112_2, which may be critical for optimal performance of the non-planar transistors (e.g. non-planar transistors 100_1 and 100_2 of FIG. 1). It is understood that the implantation may be

perpendicular to the substrate 102, i.e. substantially directly into the transistor fin top surface 114_1 and 114_2.

As shown in FIGs. 2 and 3, in a convention process of implanting an dopant, areas which are not to be implanted with a dopant (shown as transistor fins 112_1) may be covered with a relatively thick layer of blocking material 142, such as a photoresist material. For the sake of clarity, neither the isolation regions 104 nor the substrate 102, as shown in FIG. 1, are illustrated in FIGs. 2 and 3, and the gate electrode is labeled simply as element 136.

The blocking material layer 142 may be formed with a known deposition and lithography techniques, wherein the blocking material layer 142 may be deposited over all of entire structure, which is followed by the formation of an etch mask with a lithographic technique and the portions of the blocking material layer 142 are etched away to expose desired areas (i.e., the transistor fins 112_2). However, although the blocking material layer 142 may successfully block the implantation of the transistor fins 112_1, the relative thickness of the blocking material layer 142 may also shadow and block some of the implantation to the transistor fins 112_2 where the implantation is desired. The blocked ion implantation is illustrated as dashed arrows 146. The non-blocked ion implantation is illustrated as solid arrows 144.

As it can be seen in FIG. 3, the partial blocking of the implantation (i.e. arrows 146) of the transistor fins 112_2 may result in an undesired non-uniform doping along the height H of the transistor fins 112_2. One solution to this issue would be to use greater spacing between the exposed and unexposed areas such that blocking of the implantation to the transistor fins 112_2 would not occur. However, such a solution is at contrary to the desire to continually scale down the size of microelectronic devices, as will be understood to those skilled in the art.

FIGs. 4 and 5 illustrate one embodiment of the present description. As shown in FIG. 4, a blocking layer 148 may be conformally deposited over the transistor fins 112_1 and 112_2. As will be understood to those skilled in the art, conformal deposition will result in the conformal blocking material layer 148 having substantially the same thickness on the surfaces of the transistors fins 112_1 and 112_2 (e.g. on the top surface 114_1 and the sidewalls 116_1 and 118_1, and on the top surface 114_2 and the sidewalls 116_2 and 118_2, respectfully). For the sake of clarity, neither the isolation regions 104 nor the substrate 102, as shown in FIG. 1, are illustrated in FIGs. 4 and 5, and the gate electrode is labeled simply as element 136.

The conformal blocking material layer 148 may comprise any material capable of blocking the implantation of a selected dopant. In one embodiment, the conformal blocking material layer 148 may be a dielectric material, including but not limited to silicon dioxide, silicon nitride, silicon carbide, silicon oxynitride, silicon oxycarbide, silicon cyanide, and silicon oxycyanide. As will be understood, other materials such as metals, including atomic layer deposited titanium nitride, may also be used as the conformal blocking material layer 148. The conformal blocking material layer 148 may be formed with a known conformal deposition technique, including but not limited to chemical vapor deposition ("CVD"), atomic layer deposition ("ALD"), and the like. It is understood that the conformal blocking material layer 148 should be sufficiently thick to block the implant material. In one embodiment, the conformal blocking material layer 148 may be greater than about 2nm. Additionally, the conformal blocking material layer 148 should be thin enough to form a conformal layer between the transistor fins (e.g. elements 114_1 and 114_2). For example, if the transistor fins are 40nm apart, then the conformal blocking material 148 should be less than about 20nm in thickness.

As shown in FIG. 5, a portion of the conformal blocking material layer 148 may be removed to expose desired transistor fins for implantation (e.g. transistor fins 112_2). This may be achieved by the formation of an etch mask with a lithographic technique and etching away the selected portions of the conformal blocking material layer 148, as will be understood to those skilled in the art.

As it can be seen in FIG. 5, the conformal blocking material layer 148 allows for uniform doping along the height H of the transistor fins 112_2, as the dopant ions can be evenly implanted from both sides for the transistor fins 112_2 (e.g. toward sidewalls $116_1/116_2$ and toward sidewalls $118_1/118_2$). The blocked implantation is illustrated as dashed arrows 146, and non-blocked implantation is illustrated as solid arrows 144.

An embodiment of one process of using a conformal blocking material layer 148 during dopant ion implantation is illustrated in a flow diagram 200 of FIG. 6. As defined in block 210, a conformal blocking layer may be formed on transistor fins in a non-planar transistor. A photoresist material may be patterned in at least one area on the conformal blocking layer, as defined in block 220. As defined in block 230, the conformal blocking layer may be removed, such as by etching, in at least one area not covered by the photoresist material to expose at least one transistor fin to be doped by ion implantation. The photoresist material may be removed, as defined in block 240. As defined in block

250, the at least one transistor fin may then be doped by ion implantation. The conformal blocking material layer may then be removed, as defined in block 260.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 4 and 5. The subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art. Furthermore, the subject matter may also be used in any appropriate application outside of the microelectronic device fabrication field.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A method comprising:

forming a conformal blocking material layer on a plurality of transistor fins in a non-planar transistor;

removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins;

performing an ion implantation on the at least one exposed transistor fin; and

removing the conformal blocking material layer.

2. The method of claim 1, wherein forming a conformal blocking layer comprises forming a conformal dielectric blocking material layer.

3. The method of claim 2, wherein forming a conformal dielectric blocking layer comprises forming a conformal dielectric blocking material layer.

4. The method of claim 1, wherein removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, comprises:

patterning a photoresist material on at least one portion of the conformal blocking material layer;

etching the conformal blocking material layer in areas not covered by the photoresist material; and

removing the photoresist material.

5. The method of claim 1, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on the at least one exposed transistor fin.

6. The method of claim 5, wherein performing an angled ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on opposing sidewalls of the at least one exposed transistor fin.

7. The method of claim 1, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing a P-type ion implantation on the at least one exposed transistor fin.

8. The method of claim 1, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an N-type ion implantation on the at least one exposed transistor fin.

9. A method comprising:

forming a non-planar transistor having a plurality of transistor fins;

forming a conformal blocking material layer on the plurality of transistor fins such that at least one of the plurality of transistor fins is covered by the conformal blocking material layer and at least one of the plurality of transistor fins is not covered by the conformal blocking material layer; and

performing an ion implantation on the at least one transistor fin not covered by the conformal blocking material layer.

10. The method of claim 9, wherein forming the conformal blocking material layer comprises:

depositing the conformal blocking material layer on plurality of transistor fins; and

removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins;

11. The method of claim 10, wherein removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, comprises:

patterning a photoresist material on at least one portion of the conformal blocking material layer; and

etching the conformal blocking material layer in areas not covered by the photoresist material.

12. The method of claim 9, further comprising removing the conformal blocking material layer.

13. The method of claim 9, wherein forming a conformal blocking material layer comprises forming a conformal dielectric blocking material layer.

14. The method of claim 9, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on the at least one exposed transistor fin.

15. The method of claim 14, wherein performing an angled ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on opposing sidewalls of the at least one exposed transistor fin.

16. The method of claim 9, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing a P-type ion implantation on the at least one exposed transistor fin.

17. The method of claim 9, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an N-type ion implantation on the at least one exposed transistor fin.

18. A microelectronic device, comprising:

at least one non-planar transistor having a plurality of transistor fins; and

at least one of the plurality of transistor fins having a substantially uniform ion doping

along the height of the transistor fin, wherein doping is performed by a process comprising:

forming a conformal blocking material layer on the plurality of transistor fins such that at least one of the plurality of transistor fins is covered by the conformal blocking material layer and at least one of the plurality of transistor fins is not covered by the conformal blocking material layer; and

performing an ion implantation on the at least one transistor fin not covered by the conformal blocking material layer.

19. The microelectronic device of claim 18, wherein forming the conformal blocking material layer comprises:

depositing the conformal blocking material layer on plurality of transistor fins; and

removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins;

20. The microelectronic device of claim 19, wherein removing a portion of the conformal blocking material layer to expose at least one of the plurality of transistor fins, comprises:

patterning a photoresist material on at least one portion of the conformal blocking material layer; and

etching the conformal blocking material layer in areas not covered by the photoresist material.

21. The microelectronic device of claim 18, further comprising removing the conformal blocking material layer.

22. The microelectronic device of claim 18, wherein forming a conformal blocking material layer comprises forming a conformal dielectric blocking material layer.

23. The microelectronic device of claim 18, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on the at least one exposed transistor fin.

24. The microelectronic device of claim 23, wherein performing an angled ion implantation on the at least one exposed transistor fin comprises performing an angled ion implantation on opposing sidewalls of the at least one exposed transistor fin.

25. The microelectronic device of claim 18, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing a P-type ion implantation on the at least one exposed transistor fin.

26. The microelectronic device of claim 18, wherein performing an ion implantation on the at least one exposed transistor fin comprises performing an N-type ion implantation on the at least one exposed transistor fin.