

PROGRAMMABLE LOGIC DEVICE

Disclosed is a programmable logic device (PLD) which can undergo dynamic configuration at a high speed. The PLD includes a plurality of programmable logic elements (PLEs) and a switch for selecting electrical connection between the PLEs. The switch includes a plurality of circuit groups each of which includes first and second transistors. The second transistors of the circuit groups are electrically connected in parallel with one another. In each of the circuit groups, the electrical conduction between a source and a drain of the second transistor is determined based on configuration data held at a node between the gate of the second transistor and a drain of the first transistor, which allows the selection of the electrical connection and disconnection between the programmable logic elements by the selection of one of the circuit groups.

Fig. 3