

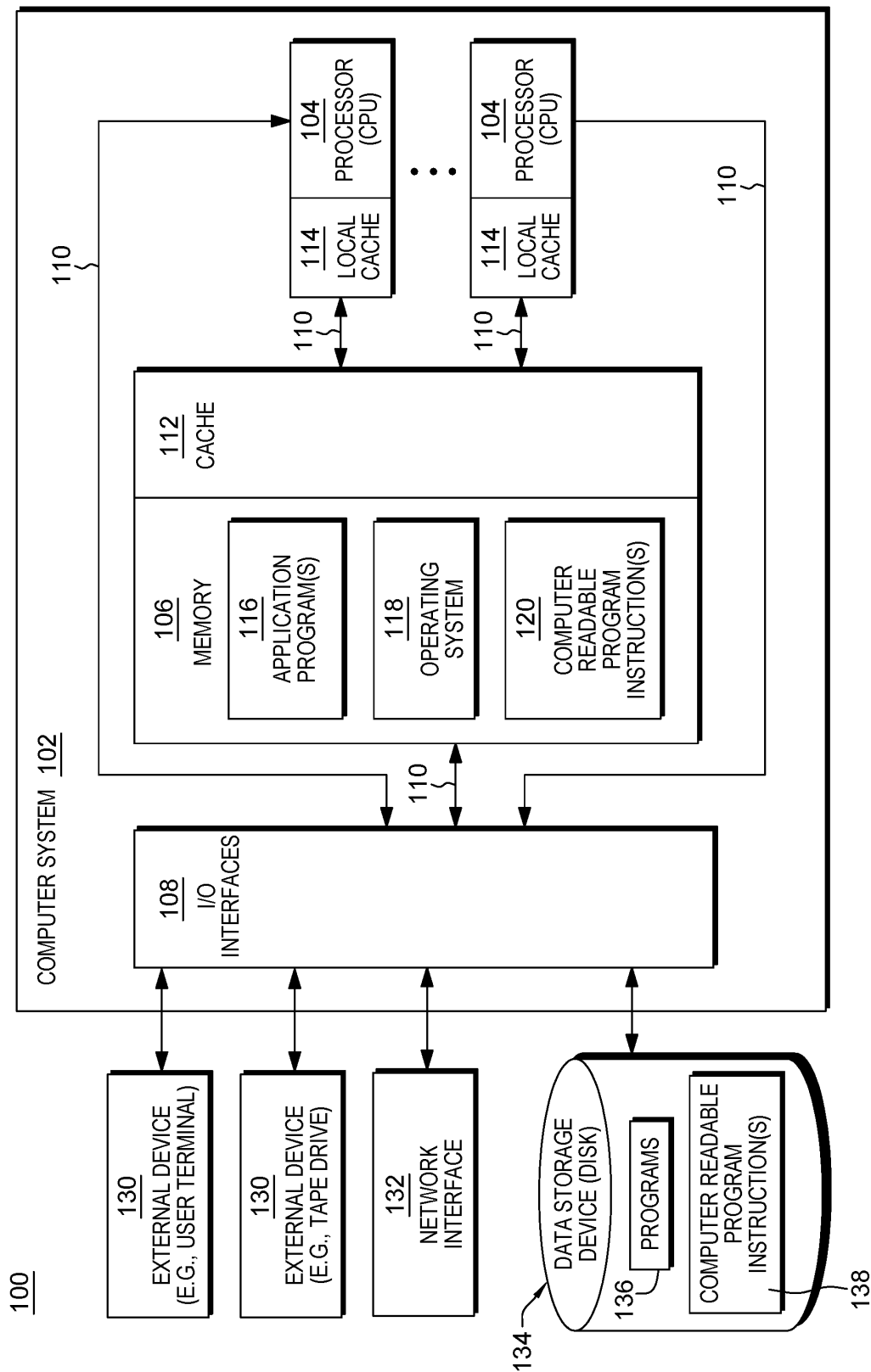


FIG. 1A

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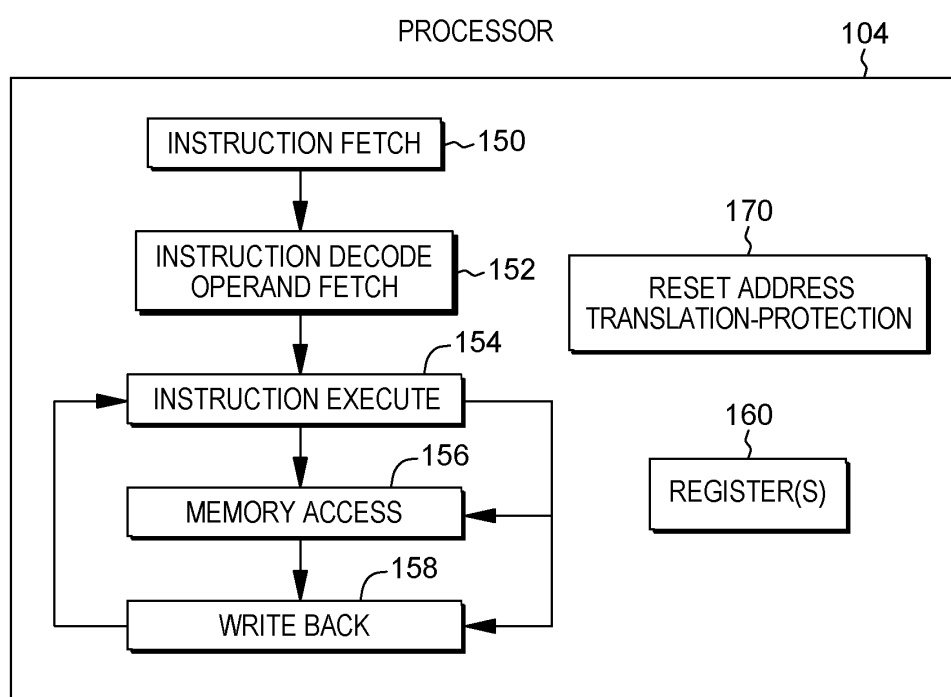


FIG. 1B

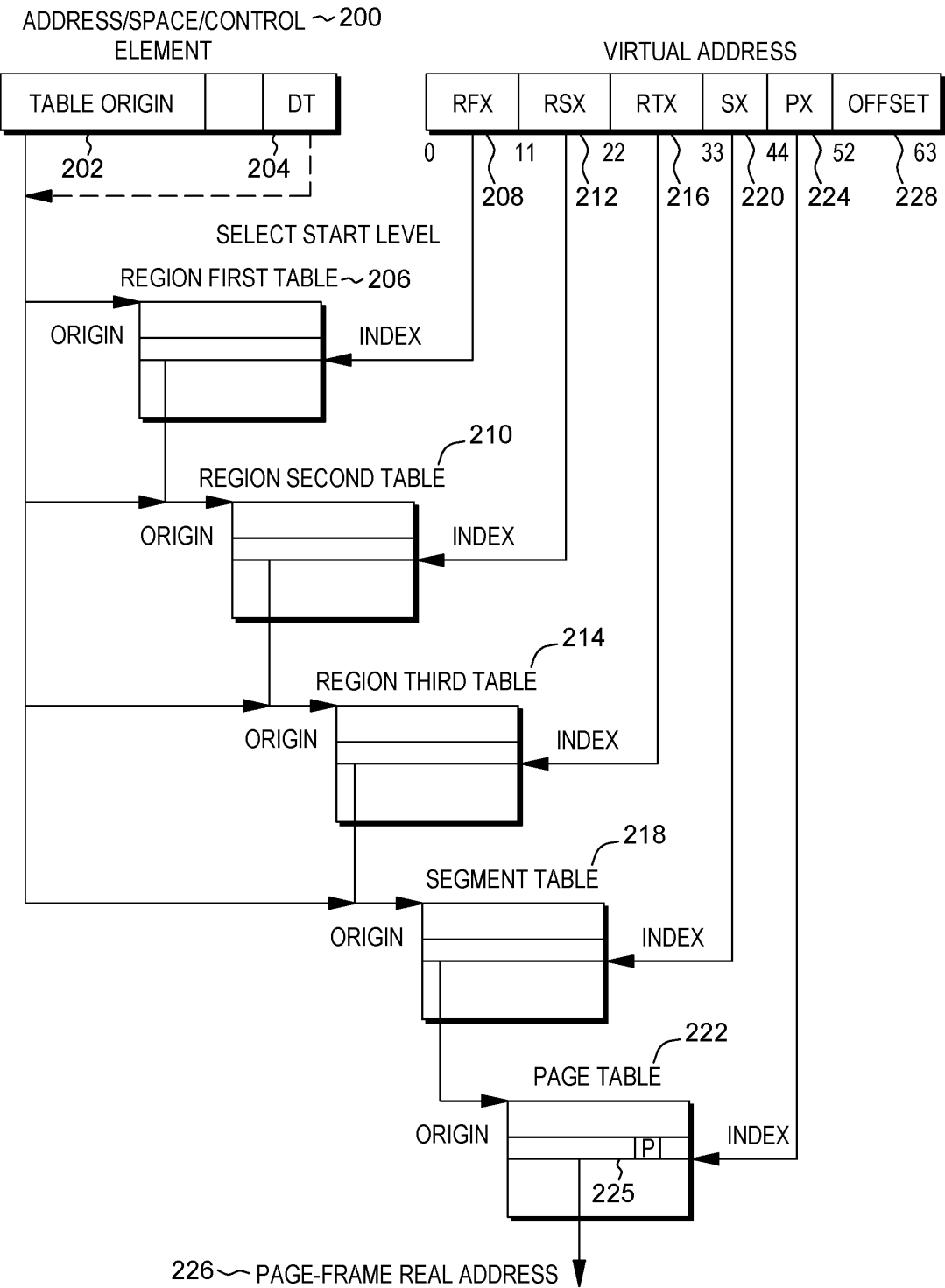


FIG. 2A

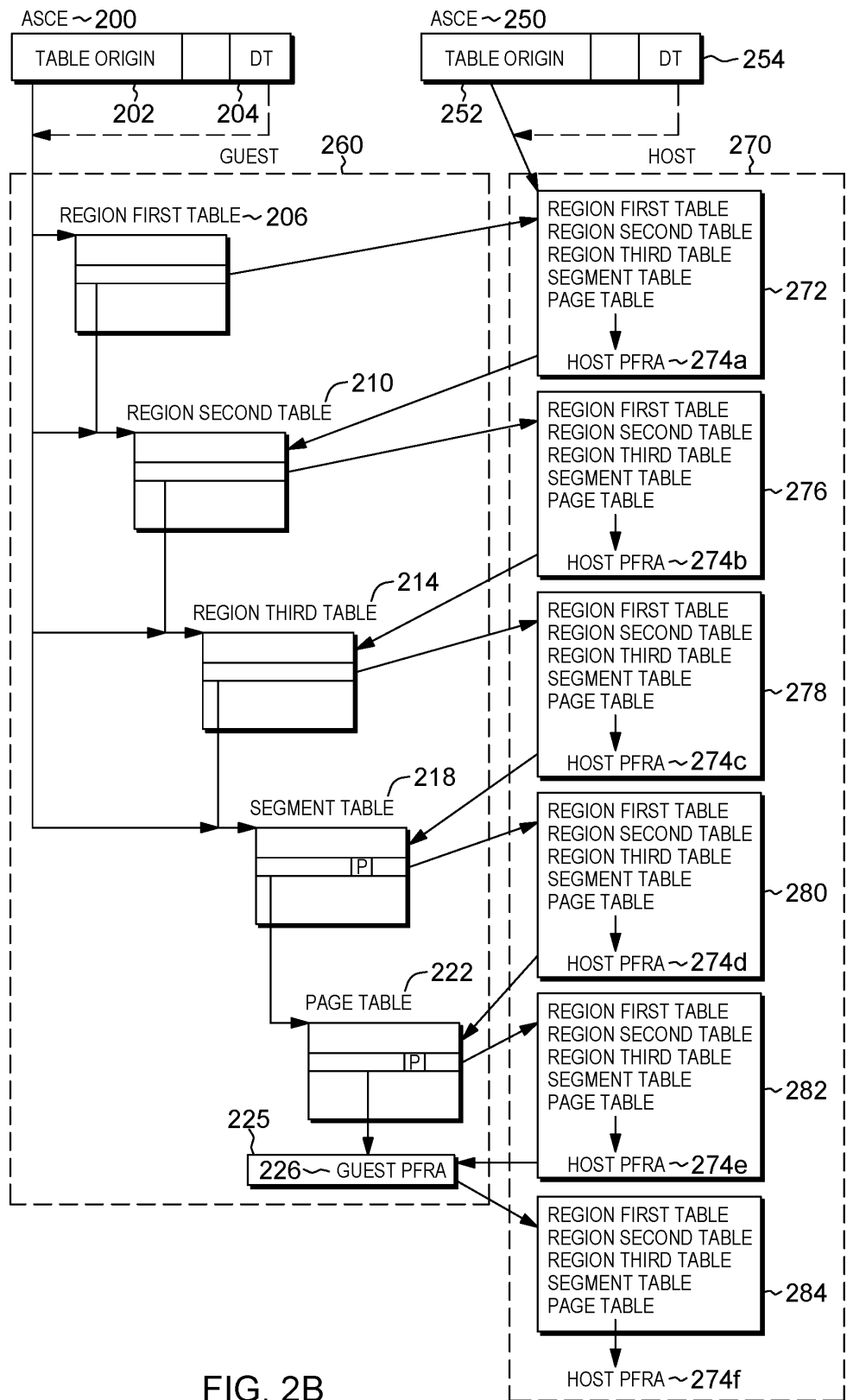


FIG. 2B

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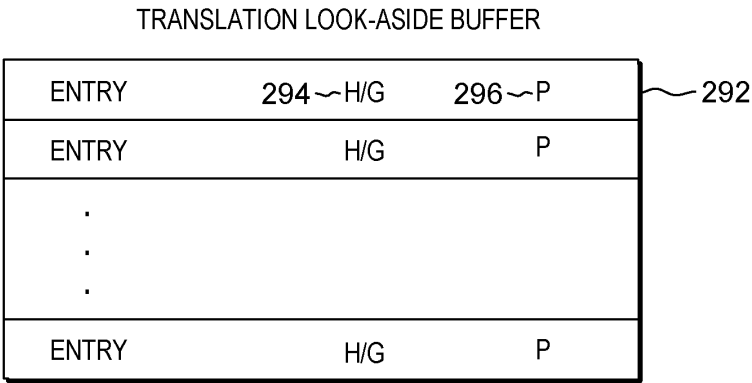


FIG. 2C

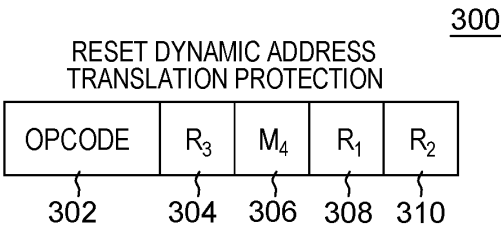


FIG. 3A

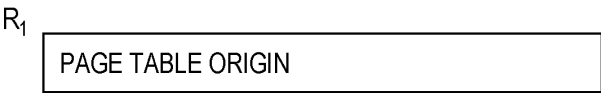


FIG. 3B

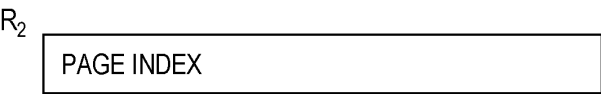


FIG. 3C

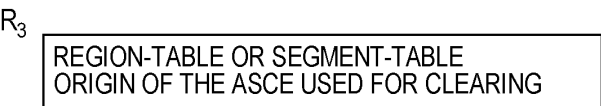


FIG. 3D

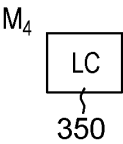
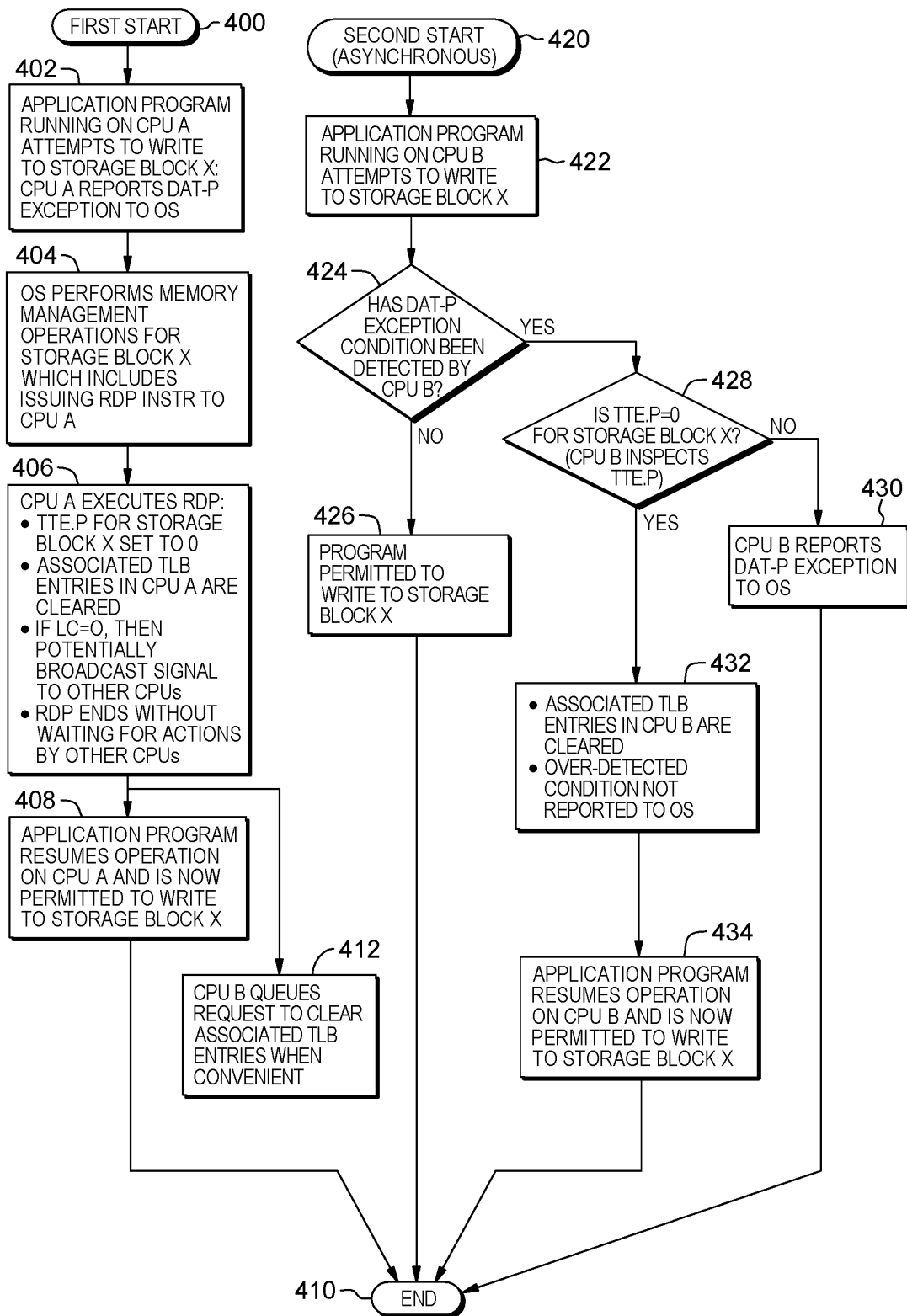
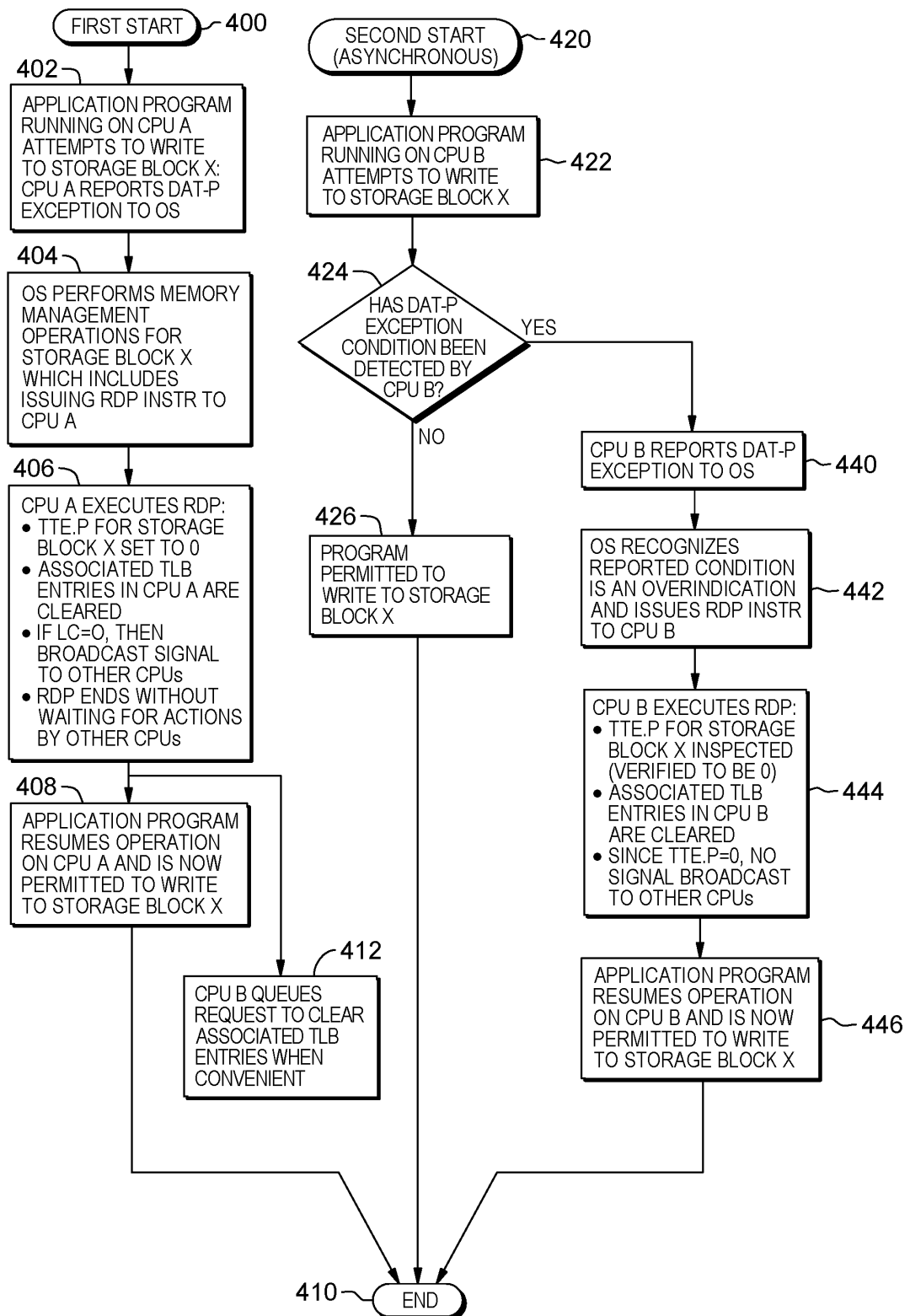


FIG. 3E

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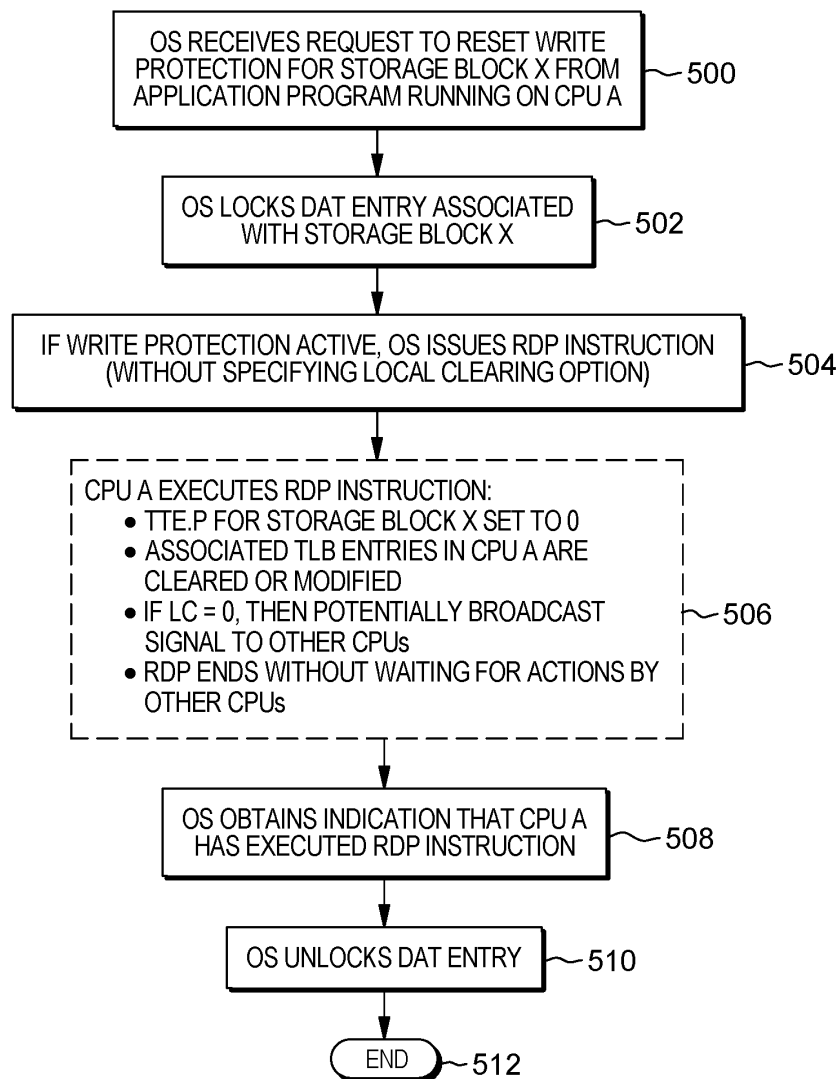


FIG. 5A

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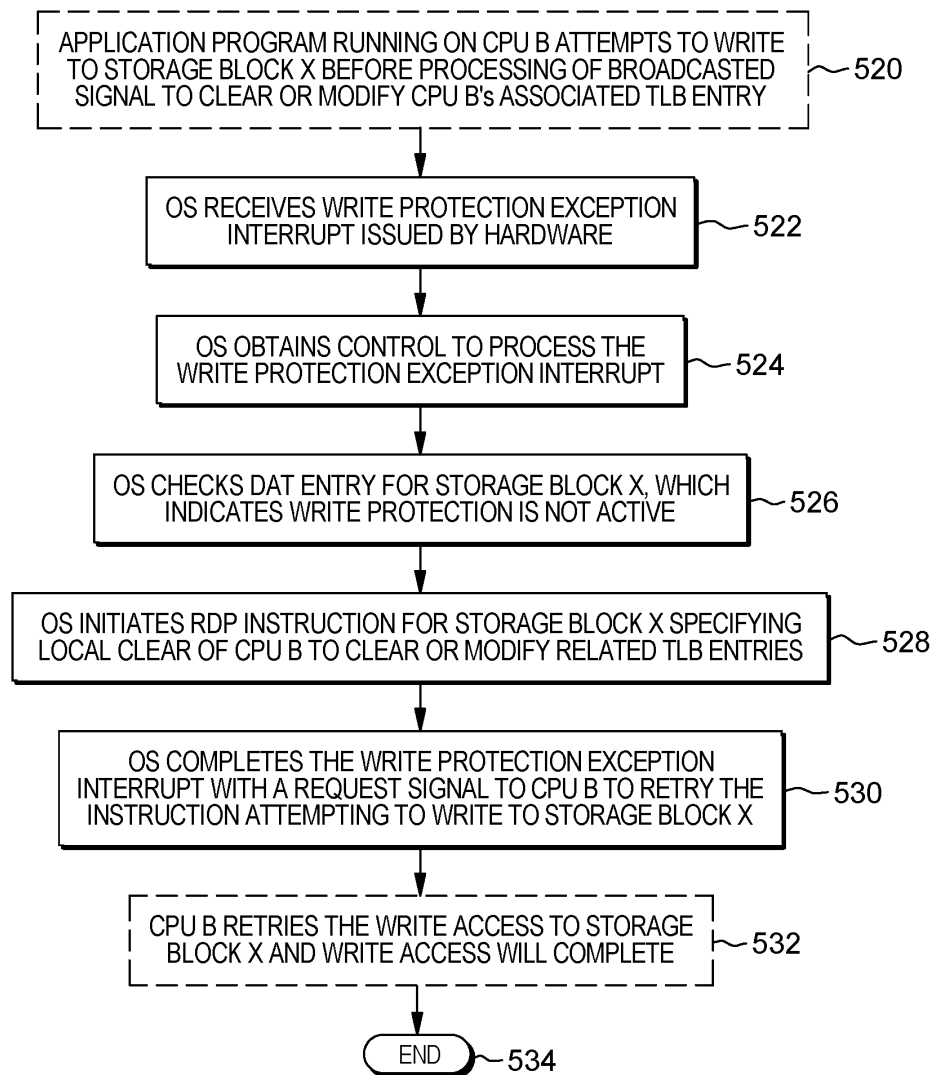


FIG. 5B

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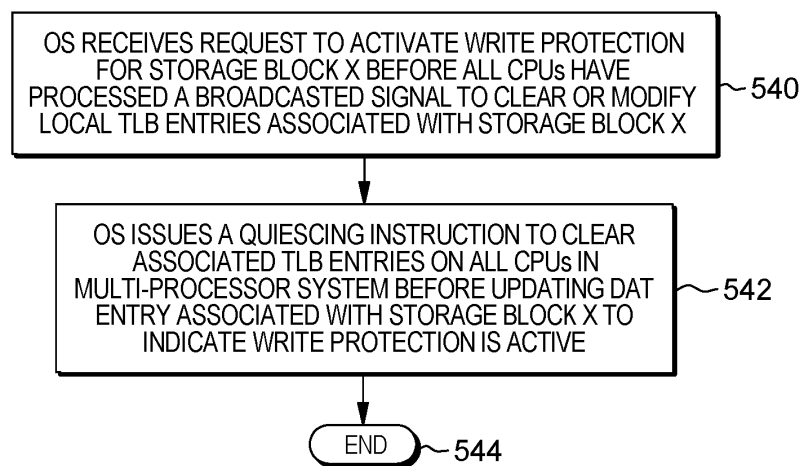


FIG. 5C

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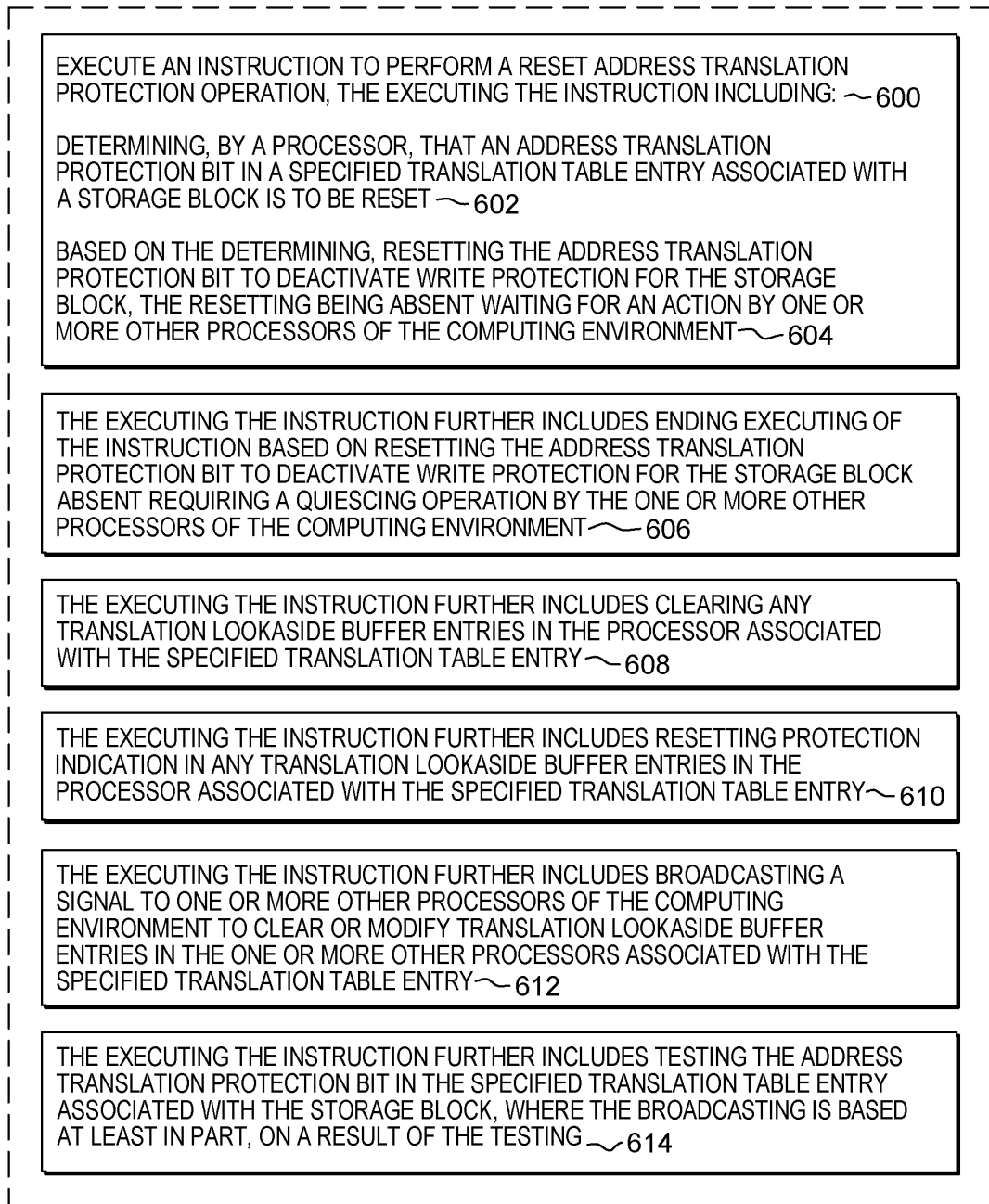


FIG. 6A

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ANOTHER PROCESSOR OF THE ONE OR MORE OTHER PROCESSORS ATTEMPTS A WRITE ACCESS TO THE STORAGE BLOCK WITHOUT THE OTHER PROCESSOR'S ASSOCIATED TRANSLATION LOOKASIDE BUFFER ENTRIES HAVING BEEN CLEARED OR MODIFIED, RESULTING IN AN ADDRESS TRANSLATION PROTECTION EXCEPTION CONDITION, AND BASED THEREON, THE OTHER PROCESSOR CAN INSPECT THE ADDRESS TRANSLATION PROTECTION BIT TO IDENTIFY THAT THE ADDRESS TRANSLATION PROTECTION EXCEPTION CONDITION IS AN OVER-INDICATION, AND BASED ON THE INSPECTION IDENTIFYING THAT THE ADDRESS TRANSLATION PROTECTION EXCEPTION CONDITION IS THE OVER-INDICATION, WRITE ACCESS TO THE STORAGE BLOCK IS PERMITTED ~ 616

ANOTHER PROCESSOR OF THE ONE OR MORE OTHER PROCESSORS ATTEMPTS A WRITE ACCESS TO THE STORAGE BLOCK WITHOUT THE OTHER PROCESSOR'S ASSOCIATED TRANSLATION LOOKASIDE BUFFER ENTRIES HAVING BEEN CLEARED OR MODIFIED, RESULTING IN AN ADDRESS TRANSLATION PROTECTION EXCEPTION CONDITION, AND BASED THEREON, THE OTHER PROCESSOR CAN INSPECT THE ADDRESS TRANSLATION PROTECTION BIT TO IDENTIFY THAT THE ADDRESS TRANSLATION PROTECTION EXCEPTION CONDITION IS AN OVER-INDICATION, AND BASED ON THE INSPECTION IDENTIFYING THAT THE ADDRESS TRANSLATION PROTECTION EXCEPTION CONDITION IS THE OVER-INDICATION, THE OTHER PROCESSOR CLEARS OR MODIFIES ITS ASSOCIATED TRANSLATION LOOKASIDE BUFFER OF ENTRIES CONTAINING THE OVER-INDICATED ADDRESS TRANSLATION PROTECTION BIT ~ 618

WHERE ANOTHER PROCESSOR OF THE ONE OR MORE OTHER PROCESSORS ATTEMPTS A WRITE ACCESS TO THE STORAGE BLOCK WITHOUT THE OTHER PROCESSOR'S ASSOCIATED TRANSLATION LOOKASIDE BUFFER ENTRIES HAVING BEEN CLEARED OR MODIFIED, RESULTING IN AN OVER-INDICATED ADDRESS TRANSLATION PROTECTION EXCEPTION CONDITION, AND BASED THEREON, REPORTS THE EXCEPTION CONDITION TO AN OPERATING SYSTEM OF THE COMPUTING ENVIRONMENT, BASED ON WHICH THE OPERATING SYSTEM ISSUES TO THE OTHER PROCESSOR THE INSTRUCTION TO PERFORM THE RESET ADDRESS TRANSLATION PROTECTION OPERATION AT THE OTHER PROCESSOR OF THE ONE OR MORE OTHER PROCESSORS ~ 620

FIG. 6B

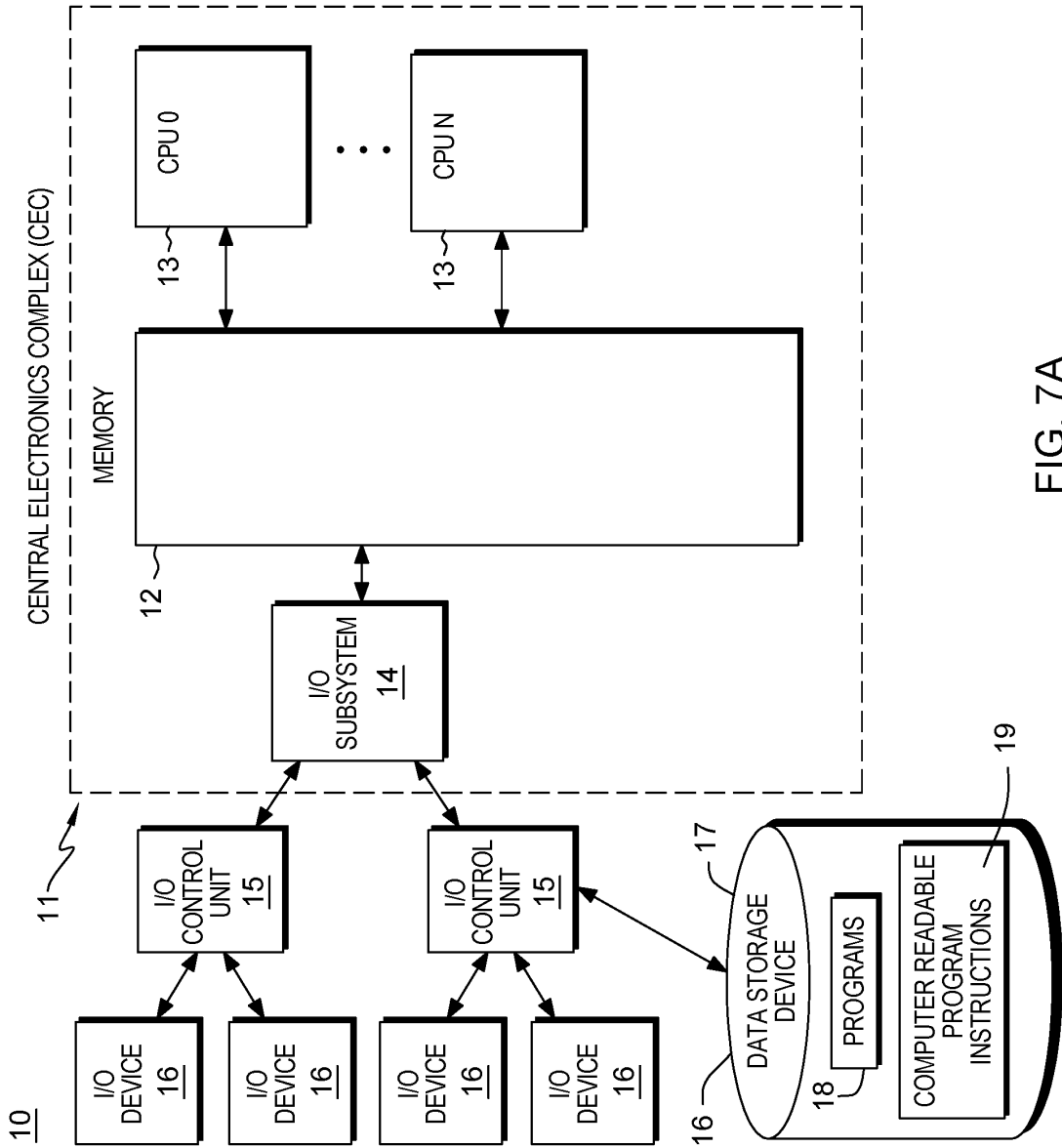


FIG. 7A

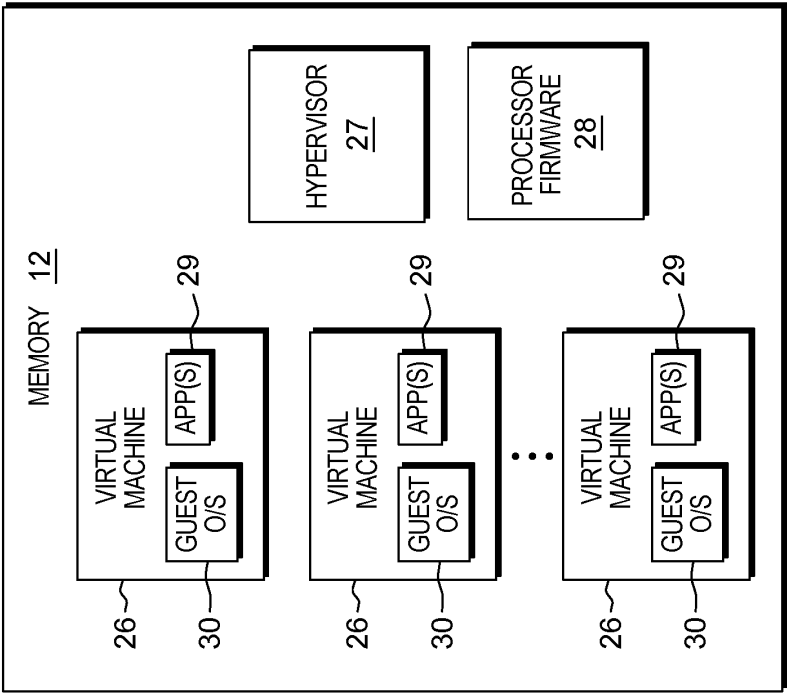


FIG. 7C

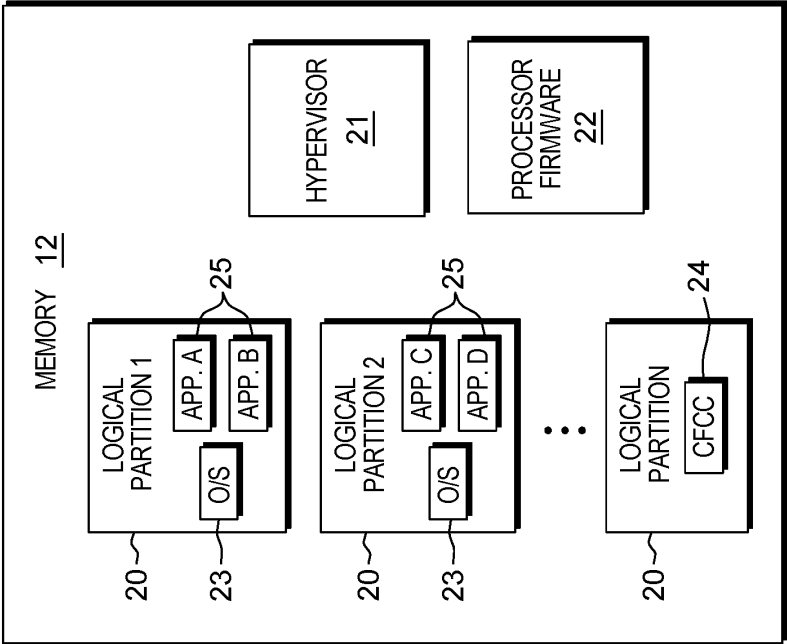


FIG. 7B

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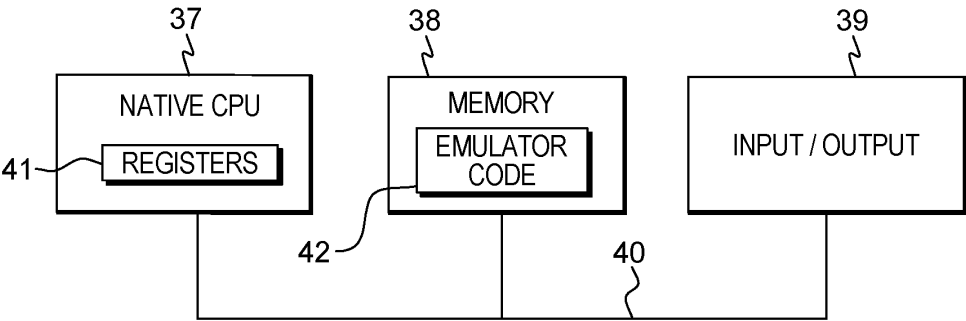


FIG. 8A

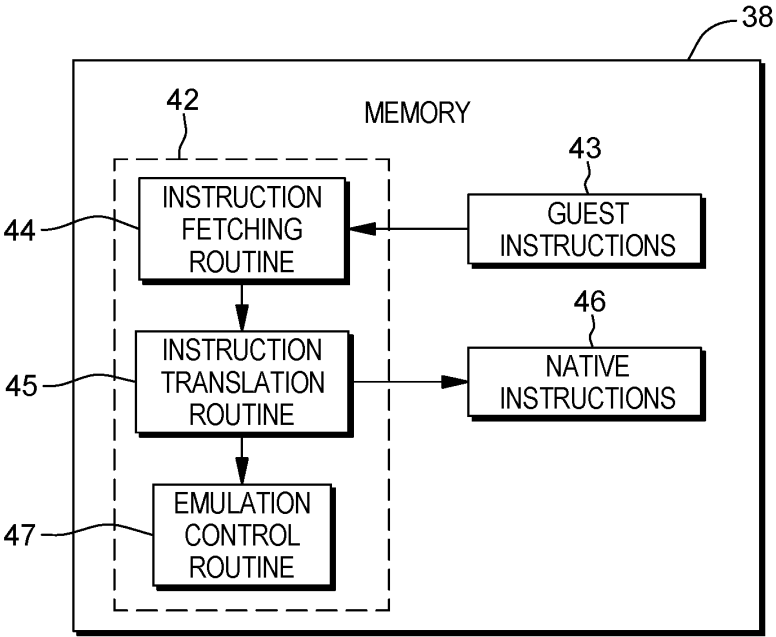


FIG. 8B

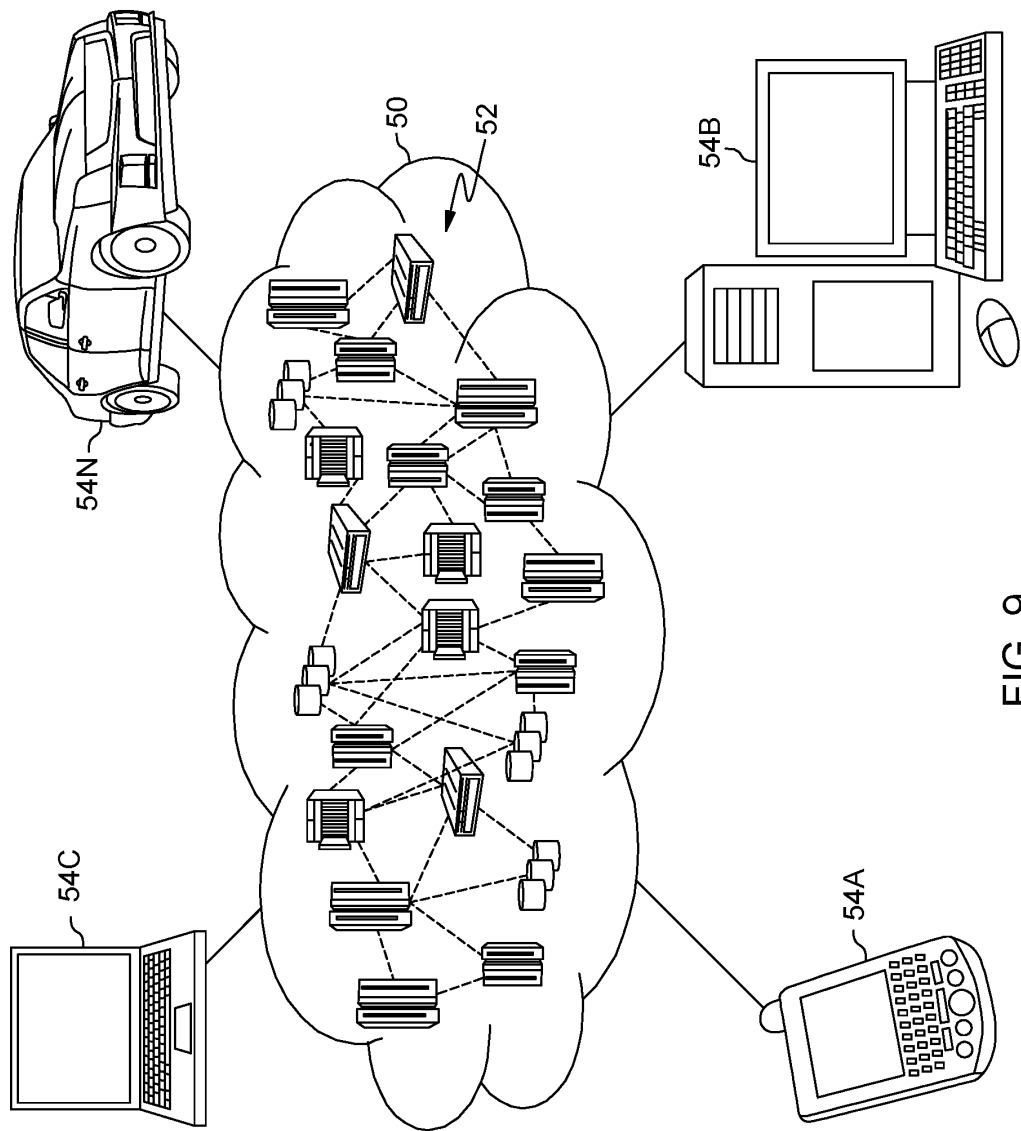


FIG. 9

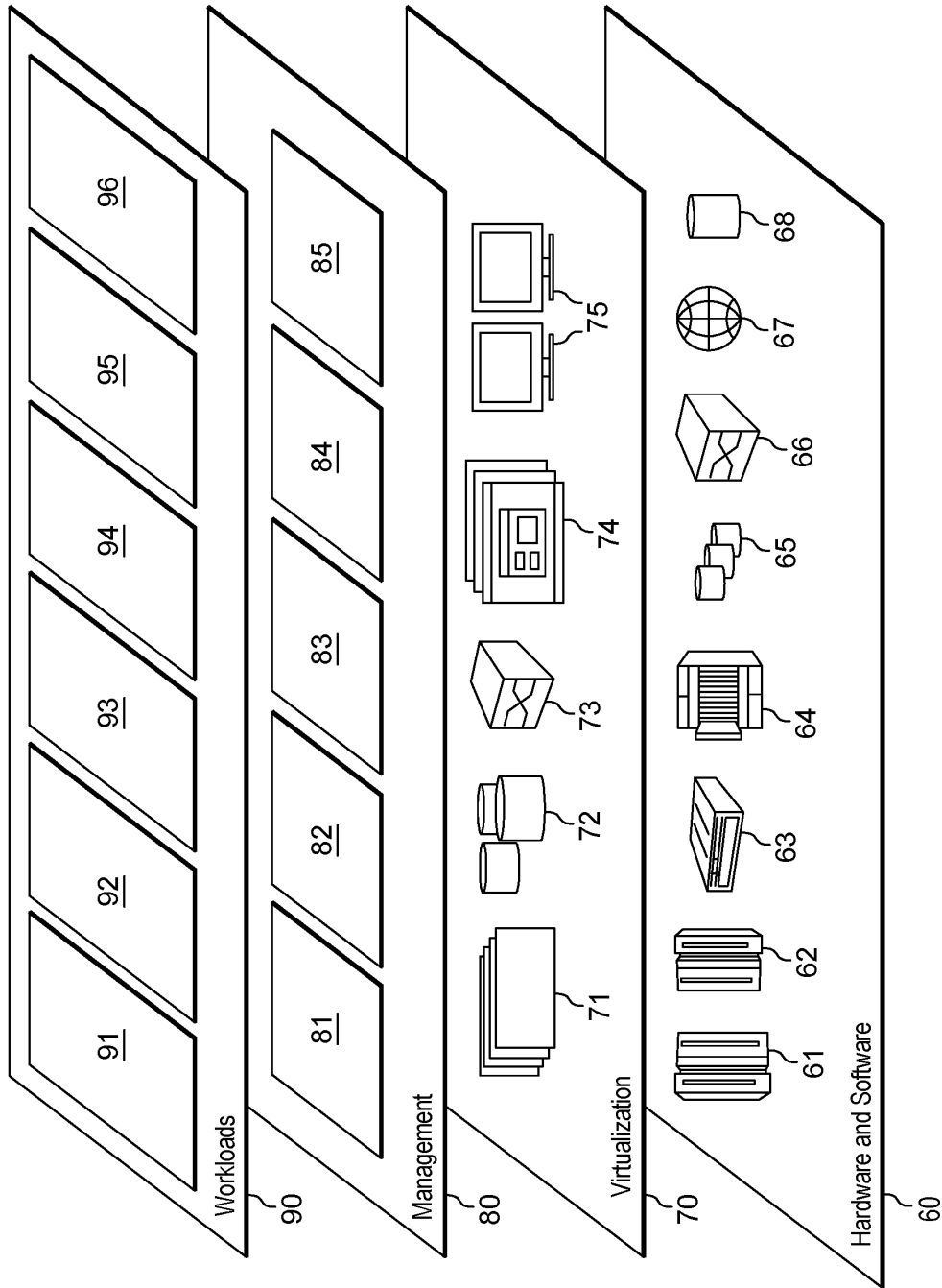


FIG. 10