CLAIMS

What is claimed is:

1. An apparatus comprising:

a chamber,

a plurality of N semiconductor processing stations arranged in a nominally circular pattern within the chamber, each semiconductor processing station having a corresponding pedestal, and each pedestal having a corresponding target location, wherein the corresponding target location of each pedestal is representative of a location which, when a wafer is placed on that pedestal and centered on that pedestal's corresponding target location, results in that wafer being considered centered on that pedestal for a given semiconductor wafer processing operation;

a rotational indexer having a central hub and a plurality of N indexer arms, the central hub rotatable relative to the chamber about a first axis nominally located at the center of the circular pattern, each indexer arm having a proximal end fixedly mounted to the central hub and a distal end that supports a rotatable wafer support that is configured to rotate about a corresponding second axis relative to the indexer arms; and

a controller including one or more memory devices and one or more processors, wherein the one or more memory devices and the one or more processors are operatively connected and the one or more memory devices store computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to:

a) select an embarkation pedestal from the plurality of pedestals,

b) select a destination pedestal from the plurality of pedestals,

c) select a selected rotatable wafer support from the plurality of rotatable wafer supports,

d) cause at least one of the central hub and the selected rotatable wafer support to rotate about the first axis and to rotate about the second axis of the selected rotatable wafer support relative to the indexer arms, respectively, such that a corresponding reference point that is fixed with respect to the selected rotatable wafer support and offset from the second axis of the selected rotatable wafer support by a first non-zero distance in a direction perpendicular to the second axis of the selected rotatable wafer support is centered on an estimated center of a wafer located at the semiconductor processing station associated with the embarkation pedestal when viewed along a direction parallel to the first axis,

e) cause the wafer located at the semiconductor processing station associated with the embarkation pedestal to be placed on the selected rotatable wafer support after the corresponding reference point for the selected rotatable wafer support is centered on the estimated center of the wafer located at the semiconductor procession station associated with the embarkation pedestal when viewed along a direction parallel to the first axis,

f) cause at least one of the central hub and the selected rotatable wafer support to rotate about the first axis and to rotate about the second axis of the selected rotatable wafer support relative to the indexer arms, respectively, such that the corresponding reference point for the selected rotatable wafer support is centered above the corresponding target location of the destination pedestal, and

g) cause the wafer on the selected rotatable wafer support to be lifted off of the selected rotatable wafer support after the corresponding reference point for the selected rotatable wafer support is centered above the corresponding target location of the destination pedestal.

2. The apparatus of claim 1, wherein the one or more memory devices further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to, for a given set of M wafers, perform (a) through (g) M times, once for each wafer, wherein $2 \leq M \leq N$.

3. The apparatus of claim 2, wherein the one or more memory devices further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to cause at least some rotation of the central hub about the first axis to occur for at least part of (d) and at least part of (f) simultaneously for all M wafers.

4. The apparatus of either claim 2 or claim 3, wherein the one or more memory devices further store additional computer-executable instructions which, when executed by the one or more processors, cause at least one of the following to occur: (e) to be performed at different times for at least two of the M wafers and (g) to be performed at different times for at least two of the M wafers.

5. The apparatus of any one of claims 2 through 4, wherein $N = 4$ and $3 \leq M \leq 4$.

6. The apparatus of any one of claims 1 through 5, wherein the first distance is selected to be larger than twice an estimated maximum pedestal location tolerance within the chamber.

7. The apparatus of any one of claims 1 through 6, wherein the one or more memory devices further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to, for (d), use the corresponding target location of the embarkation pedestal as the estimated center of the wafer located at the semiconductor processing station associated with the embarkation pedestal.

8. The apparatus of any one of claims 1 through 6, further comprising, for each semiconductor processing station, one or more corresponding wafer position sensors configured to obtain information from which a location of the center of a wafer placed on the pedestal of the corresponding semiconductor processing station can be determined, wherein the one or more memory devices further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to:

h) determine, prior to (e), the location of the center of the wafer located at the semiconductor processing station associated with the embarkation pedestal using the information from the wafer position sensors for the corresponding wafer processing station, and

i) use, in (d), the location of the center of the wafer as determined in (h) as the estimated center of the wafer located at the semiconductor processing station associated with the embarkation pedestal.

9. The apparatus of any one of claims 1 through 8, wherein the positions of the second axes relative to the central hub are not movable responsive to control signals caused to be sent by the one or more processors and no part of each rotatable wafer support is movable relative to the remainder of that rotatable wafer support responsive to control signals caused to be sent by the one or more processors.

10. The apparatus of any one of claims 1 through 9, further comprising, at each semiconductor processing station, a corresponding lift pin mechanism with a corresponding plurality of lift pins, each lift pin mechanism configured to controllably extend and retract the corresponding plurality of lift pins such that uppermost surfaces of the corresponding plurality

of lift pins are movable between at least locations above and below an uppermost surface of the pedestal of the corresponding semiconductor processing station.

11. The apparatus of claim 10, wherein the one or more memory devices further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to, prior to performing (f):

h) cause any wafers being supported by the rotatable wafer supports other than the selected rotatable wafer support to each be placed on the lift pins of a corresponding one of the semiconductor processing stations, and

i) place one of the wafers on the selected rotatable wafer support when the selected rotatable wafer support is not supporting one of the wafers.

12. The apparatus of claim 11, wherein the one or more memory devices further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to control the rotational indexer such that the indexer arms and the rotatable wafer supports are in a first configuration immediately prior to performing (h) and immediately before (i).

13. One or more non-transitory, computer-readable media storing computer-executable instructions for controlling one or more processors of a semiconductor processing tool having a chamber with a plurality of N semiconductor processing stations, each having a corresponding pedestal with a corresponding target location, arranged therewithin and a rotational indexer having a central hub and a plurality of N indexer arms each having a distal end that supports a corresponding rotatable wafer support, wherein the computer-executable instructions, when executed, cause the one or more processors to:

a) select an embarkation pedestal from the plurality of pedestals,

b) select a destination pedestal from the plurality of pedestals,

c) select a selected rotatable wafer support from the plurality of rotatable wafer supports,

d) cause at least one of the central hub and the selected rotatable wafer support to rotate about the first axis and to rotate about the second axis of the selected rotatable wafer support relative to the indexer arms, respectively, such that a corresponding reference point that is fixed with respect to the selected rotatable wafer support and offset from the second axis of the selected rotatable wafer support by a first non-zero distance in a direction perpendicular to the

second axis of the selected rotatable wafer support is centered on an estimated center of a wafer located at the semiconductor processing station associated with the embarkation pedestal when viewed along a direction parallel to the first axis,

e) cause the wafer located at the semiconductor processing station associated with the embarkation pedestal to be placed on the selected rotatable wafer support after the corresponding reference point for the selected rotatable wafer support is centered on the estimated center of the wafer located at the semiconductor procession station associated with the embarkation pedestal when viewed along a direction parallel to the first axis,

f) cause at least one of the central hub and the selected rotatable wafer support to rotate about the first axis and to rotate about the second axis of the selected rotatable wafer support relative to the indexer arms, respectively, such that the corresponding reference point for the selected rotatable wafer support is centered above the corresponding target location of the destination pedestal, and

g) cause the wafer on the selected rotatable wafer support to be lifted off of the selected rotatable wafer support after the corresponding reference point for the selected rotatable wafer support is centered above the corresponding target location of the destination pedestal.

14. The one or more non-transitory, computer-readable media of claim 13, wherein the one or more non-transitory, computer-readable media further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to, for a given set of M wafers, perform (a) through (g) M times, once for each wafer, wherein $2 \leq M \leq N$.

15. The one or more non-transitory, computer-readable media of claim 14, wherein the one or more non-transitory, computer-readable media further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to cause at least some rotation of the central hub about the first axis to occur for at least part of (d) and at least part of (f) simultaneously for all M wafers.

16. The one or more non-transitory, computer-readable media of either claim 14 or claim 15, wherein the one or more non-transitory, computer-readable media further store additional computer-executable instructions which, when executed by the one or more processors, cause at least one of the following to occur: (e) to be performed at different times

for at least two of the M wafers and (g) to be performed at different times for at least two of the M wafers.

17. The one or more non-transitory, computer-readable media of any one of claims 14 through 16, wherein $N = 4$ and $3 \leq M \leq 4$.

18. The one or more non-transitory, computer-readable media of any one of claims 13 through 17, wherein the first distance is selected to be larger than twice an estimated maximum pedestal location tolerance within the chamber.

19. The one or more non-transitory, computer-readable media of any one of claims 13 through 18, wherein the one or more non-transitory, computer-readable media further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to, for (d), use the corresponding target location of the embarkation pedestal as the estimated center of the wafer located at the semiconductor processing station associated with the embarkation pedestal.

20. The one or more non-transitory, computer-readable media of any one of claims 13 through 18, the one or more non-transitory, computer-readable media further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to:

h) determine, prior to (e), the location of the center of the wafer located at the semiconductor processing station associated with the embarkation pedestal using information from one or more wafer position sensors for the corresponding wafer processing station, and

i) use, in (d), the location of the center of the wafer as determined in (h) as the estimated center of the wafer located at the semiconductor processing station associated with the embarkation pedestal.

21. The one or more non-transitory, computer-readable media of any one of claims 13 through 20, wherein the one or more non-transitory, computer-readable media further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to, prior to performing (f):

h) cause any wafers being supported by the rotatable wafer supports other than the selected rotatable wafer support to each be placed on lift pins of a corresponding one of the semiconductor processing stations, and

i) place one of the wafers on the selected rotatable wafer support when the selected rotatable wafer support is not supporting one of the wafers.

22. The one or more non-transitory, computer-readable media of claim 21, wherein the one or more non-transitory, computer-readable media further store additional computer-executable instructions which, when executed by the one or more processors, cause the one or more processors to control the rotational indexer such that the indexer arms and the rotatable wafer supports are in a first configuration immediately prior to performing (h) and immediately before (i).