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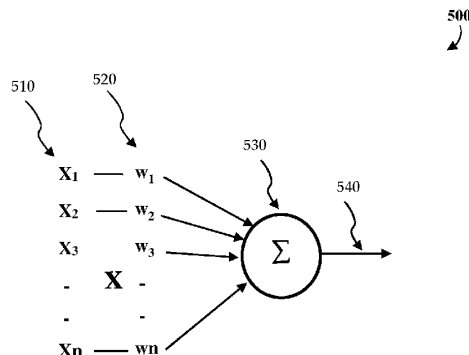


FIG. 5

(57) Abstract: A method for generating in semiconductor hardware a dot product of two floating-point vectors. The method accesses the elements of the two vectors and performs a multiply in hardware. Before performing the multiply, the exponents of the elements can be checked to determine if the result would exceed the range of the fixed-point accumulator and the multiplication of the elements skipped if exceeded. The elements passing the optional check are multiplied. The resulting product is converted to a fixed-point number and summed with an accumulator. The dot product hardware can be part of an integrated semiconductor implementation of a neural network.

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