WHAT IS CLAIMED IS:

1. A memory device, comprising:

a substrate;

a stacked structure including a plurality of gate layers and a plurality of interlayer insulating layers that are alternately stacked on the substrate in a vertical direction, the stacked structure including a row of cutouts, each of the cutouts extending in a first horizontal direction and being configured to cut the plurality of gate layers, the cutouts being apart from each other and arranged in a cell region of the stacked structure in the first horizontal direction; and

a row of channel structures, the channel structures being arranged in the cell region in the first horizontal direction, each of the channel structures extending in the vertical direction to penetrate the plurality of gate layers,

wherein, at a first height relative to the substrate, a maximum width of an end portion of at least one cutout of the row of cutouts is greater than a maximum width of a center portion of the at least one cutout, the maximum widths being determined in a second horizontal direction that is perpendicular to the first horizontal direction.

2. The memory device as claimed in claim 1, wherein, at the first height, a distance in the second horizontal direction from the end portion to the row of channel structures is less than a distance in the second horizontal direction from the center portion to the row of channel structures.

3. The memory device as claimed in claim 1 or claim 2, wherein a maximum width of the end portion at a second height is less than the maximum width of the end

portion at the first height, the second height being less than the first height relative to the substrate, the maximum widths being determined in the second horizontal direction.

4. The memory device as claimed in claim 1 or claim 2, wherein, at a second height that is less than the first height relative to the substrate, a maximum width of the end portion is equal to or less than the maximum width of the center portion, the maximum widths being determined in the second horizontal direction.

5. The memory device as claimed in any one of the previous claims, wherein:

the plurality of gate layers includes at least one bottom gate layer, a plurality of intermediate gate layers on the at least one bottom gate layer, and at least one top gate layer on the plurality of intermediate gate layers, and

the stacked structure further includes a row of top cutouts that are spaced apart from each other and arranged in the first horizontal direction in the cell region, each of the top cutouts extending in the first horizontal direction between two neighboring cutouts in the row of cutouts while cutting the at least one top gate layer but not cutting the plurality of intermediate gate layers and the at least one bottom gate layer.

6. The memory device as claimed in any one of claims 1 to 4, wherein:

the plurality of gate layers includes at least one bottom gate layer, a plurality of intermediate gate layers on the at least one bottom gate layer, and at least one top gate layer on the plurality of intermediate gate layers, and

the stacked structure further includes a row of bottom cutouts that are spaced apart from each other and arranged in the first horizontal direction in the cell region, each of the bottom cutouts extending in the first horizontal direction between two neighboring cutouts

in the row of the cutouts while cutting the at least one bottom gate layer but not cutting the plurality of intermediate gate layers and the at least one top gate layer.

7. The memory device as claimed in any one of the previous claims, further comprising a semiconductor layer between the substrate and the stacked structure, and a plurality of support patterns each surrounded by the semiconductor layer, at least one of the plurality of support patterns overlapping at least one of the rows of the cutouts in the vertical direction.

8. The memory device as claimed in claim 7, wherein the at least one of the plurality of support patterns overlaps two neighboring end portions in the row of the cutouts in the vertical direction.

9. The memory device as claimed in claim 8, wherein a bottom surface of at least one of the two neighboring end portions is upwardly convex relative to the substrate.

10. A memory device, comprising:

a substrate;

a stacked structure including a plurality of gate layers and a plurality of interlayer insulating layers that are alternately stacked on the substrate in a vertical direction; and

channel structures arranged in a cell region of the stacked structure in a first row, a second row, and a third row that extend in a first horizontal direction, the channel structures each extending in the vertical direction to penetrate the plurality of gate layers,

wherein:

the stacked structure includes:

a first row of discontinuous cutouts that discontinuously cut the plurality of gate layers in the first horizontal direction between the first row of channel structures and the second row of the channel structures in the cell region; and

continuous cutouts that continuously cut the plurality of gate layers in the first horizontal direction in the cell region, and

the second and third rows of the channel structures are between the first row of discontinuous cutouts and the continuous cutouts,

wherein, at a first height relative to the substrate, a maximum width of an end portion of at least one discontinuous cutout of the first row of discontinuous cutouts is greater than a maximum width of a center portion of the at least one discontinuous cutout, the maximum widths being determined in a second horizontal direction that is perpendicular to the first horizontal direction.

11. The memory device as claimed in claim 10, wherein, at the first height relative to the substrate, the maximum width of the center portion of the at least one discontinuous cutout is less than a maximum width of the continuous cutouts, the maximum widths being determined in the second horizontal direction.

12. The memory device as claimed in claim 10 or claim 11, wherein the continuous cutouts continuously cut the plurality of gate layers in a connection region of the stacked structure in the first horizontal direction.

13. The memory device as claimed in claim 10, wherein the stacked structure further includes a second row of discontinuous cutouts that discontinuously cut the

plurality of gate layers in the first horizontal direction between the second row of channel structures and the third row of channel structures in the cell region.

14. The memory device as claimed in claim 13, wherein:

a gap is present between two neighboring cutouts in the first row of discontinuous cutouts,

a gap is present between two neighboring discontinuous cutouts in the second row of discontinuous cutouts, and

the gap between the two neighboring cutouts in the first row of discontinuous cutouts is not aligned with the gap between the two neighboring discontinuous cutouts in the second row of discontinuous cutouts in the second horizontal direction.

15. The memory device as claimed in any one of claims 10 to 14, wherein:

the plurality of gate layers includes at least one bottom gate layer, a plurality of intermediate gate layers on the at least one bottom gate layer, and at least one top gate layer on the plurality of intermediate gate layers,

the stacked structure further includes rows of discontinuous top cutouts that discontinuously cut the at least one top gate layer in the first horizontal direction and do not cut a plurality of intermediate conductive layers and the at least one bottom gate layer, and

each of the discontinuous top cutouts extends between two neighboring discontinuous cutouts in the first row of discontinuous cutouts.

16. A memory device, comprising:

a substrate;

a stacked structure including a plurality of gate layers and a plurality of interlayer insulating layers that are alternately stacked on the substrate in a vertical direction; and

a plurality of channel structures in a cell region of the stacked structure, the channel structures extending in the vertical direction to penetrate the plurality of gate layers,

wherein:

the stacked structure includes a row of cell region cutouts, each of the cell region cutouts extending in a first horizontal direction and cutting the plurality of gate layers,

the cell region cutouts are spaced apart from each other and are arranged in the first horizontal direction in the cell region,

the stacked structure includes a row of connection region cutouts, each of the connection region cutouts extending in the first horizontal direction and cutting the plurality of gate layers, and

the connection region cutouts are spaced apart from each other and are arranged in the first horizontal direction in a connection region,

wherein at a first height relative to the substrate, a maximum width of an end portion of at least one cell region cutout among the row of cell region cutouts is greater than a maximum width of a center portion of the at least one cell region cutout, the maximum widths being determined in a second horizontal direction that is perpendicular to the first horizontal direction.

17. The memory device as claimed in claim 16, wherein:

at the first height, a maximum width of an end portion of at least one connection region cutout is greater than a maximum width of a center portion of the at least one connection region cutout,

the maximum widths being determined in the second horizontal direction.

18. The memory device as claimed in claim 17, wherein, at the first height, the maximum width of the end portion of the at least one cell region cutout is less than the maximum width of the end portion of the at least one connection region cutout.

19. The memory device as claimed in claim 16, wherein, at a second height relative to the substrate, a maximum width of the end portion of the at least one cell region cutout among the row of the cell region cutouts is greater than a maximum width of an end portion of at least one connection region cutout among the row of the connection region cutouts, the maximum widths being determined in the second horizontal direction.