

PATENT SPECIFICATION

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COMPLETE SPECIFICATION

Semiconductor Devices and Methods of Manufacture

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices both in discrete form and in integrated circuit form, and to methods of producing such devices making use of epitaxial deposition techniques.

According to the present invention, a semiconductor device includes a body of monocrystalline semiconductor material and a distinct region of monocrystalline semiconductor material comprising an epitaxial deposit on and upstanding from a plane surface portion of the said body, the upstanding region being edge isolated by continuous insulating material which leaves uncovered at least part of the surface of the upstanding region opposite the said surface of the body, and an electrical contact to the upstanding region, the contact covering the surface area of the upstanding region not covered by the insulating material and extending on to the insulating material. The electrical contact can be a flanged metallic plug the flange of which is positioned on the electrically insulating material standing proud of the said surface of the region with the base of the plug positioned on the distal surface of the region. By employing a suitable metal, e.g., gold, or molybdenum, or molybdenum overlaid by gold, a rectifying contact can be made between the metal layer and the said surface of the upstanding

region to form a metal-semiconductor barrier (Schottky) diode junction. In one embodiment, suitable for employment as a mixer diode, the semiconductor body is an elongated diffused region in a substrate and the upstanding region is elongated and located wholly within the surface exposed confines of the diffused region. The contact to upstanding region is a metal strip overlying the insulating material, extending transversely across the elongated upstanding region and making rectifying contact with the said surface of that region to form a metal-semiconductor barrier diode; the device also includes a metallic film overlying the insulating material and extending into ohmic contact with opposite ends of the diffused region.

The invention also is a process for fabricating a semiconductor device, including the steps of forming an insulating oxide layer on a surface of a monocrystalline semiconductor substrate to leave a region of that surface uncovered and surrounded by oxide material, epitaxially depositing semiconductor material on the said uncovered surface region to form a region upstanding from that surface and surrounded by contiguous oxide material forming further insulating oxide material at least on the first mentioned oxide layer, the further oxide material having an aperture leaving at least part of the surface area of the upstanding region opposite the said substrate surface, and forming a metallic contact positioned at least partly on the further layer of oxide material and covering the surface area of the upstanding region bounded by the said aperture opposite the said substrate surface, the contact making electrical connection with the upstanding region. Preferably the oxide layer defines a peripheral frame surrounding

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the uncovered region of the substrate, the extent of the oxide layer along the substrate surface having been selected to preclude growth of semiconductor material on the oxide layer. It is readily possible to form the oxide layer to a preselected thickness. This thickness can be precisely measured to within a few hundred angstroms by comparing the color of the layer to color charts, and to within a few angstroms by using interferometer techniques. These measurements may be accomplished without damage to the oxide layer. Precise measurement permits precise control of the thickness of the layer by adjustment of the process parameters. The oxide layer is then patterned by conventional photolithographic techniques to suitably expose the substrate. The oxide layer is preferably also removed in all inconsequential areas so that only a strip of the oxide layer remains to define the periphery of the exposed area of the substrate. Epitaxial material can then be deposited over the areas of the semiconductor substrate exposed through the oxide layer until it reaches a thickness corresponding approximately to the thickness of the oxide layer, which thickness is precisely known. The oxide layer serves as a fiducial thickness marker from which the precise thickness of the epitaxial layer can be determined by simple mechanical techniques without damage to the epitaxial layer. The parameters of the epitaxial deposition process can then be selected so as to obtain precise control over the thickness of the deposited region. Thus the ability to measure the thickness of each epitaxial layer, or randomly selected layers from a production batch, by an inexpensive and precise method, without damage to the device permits the precise control of the thickness of the epitaxial layer by adjustment of the process parameters.

In the fabrication of a Schottky diode by use of such a process, a thin, high resistivity epitaxial layer is formed on a low resistivity substrate in a confined area as described above. A second oxide film, or other insulating layer, is then deposited over the epitaxial layer. An aperture is then cut in the second oxide layer and a non-alloying metal film deposited over the aperture to form a metal-semiconductor barrier diode. Preferably the epitaxial material is high resistivity and has a thickness equal to or less than the normal depletion width of the high resistivity epitaxial material so as to provide an essentially zero series resistance and flat capacitance-voltage characteristic until the forward voltage has reached a predetermined level sufficient to reduce the depletion width to a distance less than the thickness of the epitaxial layer. Further, the epitaxial layer is preferably relatively high resistance material so as to have a low areal junction capacity.

A diode structure suitable for use in a

hybrid mixer circuit can be fabricated by diffusing an elongated low resistivity region in a monocrystalline semiconductor substrate having a high resistivity, forming an insulating oxide layer on the surface of the substrate, the oxide layer being a frame having an opening defining an elongated exposed area of the diffused region and covering the remainder of the diffused region. Semiconductor material is then epitaxially deposited on the uncovered area of the substrate surface to form an epitaxial high resistivity region in and filling the opening of the frame. A second insulating oxide layer is then formed over the first mentioned oxide layer and the epitaxial region and an elongated opening is formed only in the second oxide layer to extend transversely across the epitaxial region. Openings are formed in both oxide layers over the opposite ends of the diffused region, and a metal film is deposited on the second oxide layer to make rectifying contact with the exposed surface of the epitaxial region and ohmic contact with the said diffused region through the openings in the oxide layers. Selected portions of the metal film are removed to form one conductor extending into contact with the epitaxial region and another conductor extending into contact with the diffused region at the opposite ends thereof.

The invention also is a semiconductor device having a semiconductor region upstanding from a surface portion of a diffused region in a monocrystalline semiconductor substrate, the region being edge isolated by continuous insulating material which also overlies the diffused region, an electrical contact to the outstanding region being formed overlying the insulating material to make rectifying contact with the region and form a metal-semiconductor barrier diode junction. The diffused region can form the base region of a planar transistor, the base region being surrounded by a substrate region forming a collector region of the transistor. The base region includes an emitter region spaced from the upstanding region. Alternatively the substrate can include further diffused regions, displaced from the first mentioned diffused region, extending to the same surface of the substrate to provide emitter, base and collector regions of a planar transistor.

The invention also provides a transistor comprising a semiconductor substrate having a region of one conductivity type extending to a surface thereof and forming the collector region of the transistor. A semiconductor region of opposite conductivity type upstanding from a surface of the collector region forms the base region of the transistor, the upstanding base region being edge-isolated by continuous insulating oxide material, and an emitter region is disposed, in and extends to the surface of, the upstanding region remote from the substrate. Electrical contacts are

positioned on the insulating material and extend to the base and emitter regions of the transistor. By controlling the thickness of the oxide layer, and using this as a reference to control the thickness of the base region in the manner described above, the base region width or thickness can be precisely controlled and have a uniform resistivity across its width.

By way of example, the invention will be described in greater detail with reference to the accompanying drawings, in which:

FIGURE 1 is an enlarged, somewhat schematic sectional view of a diode embodying the present invention, the figure also serving to illustrate a method of fabrication in accordance with the present invention;

FIGURE 2 is an enlarged, somewhat schematic perspective view illustrating a step in the method of fabricating the diode illustrated in FIGURE 1;

FIGURE 3 is an enlarged, somewhat schematic plan view of a hybrid mixer;

FIGURE 4 is an enlarged, somewhat schematic plan view of one of the diodes used in the mixer of FIGURE 3 and constructed in accordance with an embodiment of the present invention;

FIGURE 5 is an enlarged, somewhat schematic sectional view taken substantially on lines 4—4 of FIGURE 3;

FIGURE 6 is an enlarged, somewhat schematic sectional view illustrating an integrated circuit fabricated using a method in accordance with the present invention;

Figure 6a is the circuit diagram of the device shown in FIGURE 6;

FIGURE 7 is an enlarged, somewhat schematic sectional view of a transistor fabricated by a method in accordance with this invention;

FIGURE 8 is an enlarged, somewhat schematic sectional view of a high speed switching device fabricated using a method in accordance with this invention; and

FIGURE 8a is an equivalent circuit diagram of the switching device of FIGURE 8.

Referring now to the drawings, and in particular to FIGURE 1, a metal-semiconductor diode, commonly referred to as a Schottky barrier, constructed in accordance with the present invention, is indicated generally by the reference numeral 10. The rectifying junction is formed between a metal film 12 and a high resistivity N-type epitaxial plug 14. The metal film 12 serves as the expanded anode contact. The epitaxial plug 14 is grown on a monocrystalline, relatively low resistivity substrate 16 and a second metallized film 18 over the opposite side of the substrate 16 serves as the cathode contact. A thermally grown oxide film 20 provides edge isolation for the epitaxial plug 14, in addition to serving as an epitaxial growth mask as hereafter described, and a relatively thick deposited

oxide film 22 increases the separation between the low resistivity substrate and the anode metal film 12 to reduce the stray capacitance of the diode as will presently be described.

The epitaxial plug 14 which forms the cathode is high resistivity material and has a precisely controlled thickness equal to or less than the depletion width calculated for the particular resistivity. The high resistivity material makes the areal junction capacity very low. If the thickness of the epitaxial material 14 is less than the depletion width, the depletion region extends all the way to the surface of the low resistivity substrate 16, leaving no undepleted epitaxial material. This results in essentially zero series resistance for the epitaxial material. Further, if the thickness of the epitaxial plug 14 is made less than the normal depletion width, the effective depletion width will then be equal to the thickness of the epitaxial material. Then the capacitance voltage characteristic will remain essentially flat until the forward voltage across the diode is sufficiently high to reduce the natural depletion width to a value less than the epitaxial thickness. Since the depletion material is very thin, there is a certain amount of auto-doping from the substrate material which occurs during the epitaxial growth. This decreases the resistivity of the epitaxial material and places an upper limit on the resistivity of the epitaxial material which can be obtained.

In fabricating the diode 10 using a process in accordance with the present invention, an oxide film is formed on the low resistivity, monocrystalline, N-type semiconductor substrate 16. The oxide is preferably thermally grown, although other types of oxides may be employed if desired or necessary to protect previous diffusions or other structure. In most cases, however, a thermal oxide may be used because the impurity redistributions occurring at the high temperatures do not affect subsequent device behavior and are therefore not important. The thickness of the oxide film is chosen to be substantially equal to the desired thickness of the epitaxial plug 14 and the thickness may be precisely determined by nondestructive techniques to within error limits far more precise than are required. For example, the thickness of the oxide can be determined by visual inspection for color to within about ± 100 angstroms, and can be determined to within a few angstroms by using conventional interferometer techniques. The important aspect is that the oxide film can be measured in this manner without damage to the oxide so that the thickness can be monitored at an intermediate point in the fabrication of the device.

Next, the oxide film is patterned as illustrated in FIGURE 2, using conventional photolithographic techniques so as to remove parts of the oxide film and expose the sub-

strate 16 in the predetermined areas in which the epitaxial layer or plug 14 is to be deposited. It is important that all excess oxide be removed except that necessary to peripherally define the area in which the epitaxial plug is to be deposited and that necessary to prevent shorting of the active region of the device. It is important to remove all excess oxide which is not required to define the periphery of the preselected area so as to prevent spurious growth of the epitaxial material upon the surface of the oxide. In general, it is believed that spurious epitaxial growth on the surface of the oxide 20 is prevented by reason of the fact that the epitaxial material migrates along the surface of the oxide until it finds its way to the substrate 16, unless the epitaxial material first encounters an anomaly in the surface of the oxide film 20 in which it can collect. By reducing the surface area of the oxide 20 to the minimum required to define the areas 24 and to perform whatever electrical isolation function is required of the oxide layer, the chances that the epitaxial material will take root in an anomaly are substantially reduced. It is also believed that this phenomenon results in a less rapid growth of the epitaxial layer after the epitaxial layer has reached the thickness of the oxide layer which reduces the cruciality of stopping the epitaxial deposition at a precise moment in order to obtain the desired thickness.

Next, high resistivity N-type material is epitaxially grown on the exposed surface of the semiconductor substrate 16. The epitaxial material grown in the limited area defined by the central openings 24 forms the plug 14. The excess epitaxial material 26 grown on the remaining exposed surface of the substrate 16 is of no consequence in the function of the semiconductor devices. After the epitaxial layer has been deposited, the thickness of the layer, and in particular the plug 14, may be checked using conventional mechanical profiling devices such as the machine sold under the trademark Talysurf by Taylor-Hobson, Leicester, England, a division of The Rank Organization. The profile will indicate the thickness of the epitaxial plug relative to the thickness of the oxide layer 20 which serves as the fiducial marker of known thickness to within one micron or less.

Next, the oxide layer 22 is deposited over the substrate using any suitable conventional low temperature process. A low temperature process is preferred over a thermal oxide because elevated temperature will cause diffusion into the plug 14 from the substrate and concentration of impurities in the plug at the surface. The oxide layer 22 is made as thick as possible without cracking. There are three conventional insulating layers, glassy layers, thermally grown oxides, and oxides deposited at temperatures lower than those required for

thermally grown oxides, which may be used for this purpose and all result in some in-optimum condition. For example, although the glass-like layers can be obtained in substantial thicknesses, these layers cannot be photolithographically patterned with sufficient resolution so that the junctions are limited to relatively large areas. Thermally grown oxides can be obtained in large thicknesses, and have good resolution, but the impurity redistributions occurring at elevated temperatures required for oxide growth often adversely affect other regions of the structure and are therefore undesirable. Deposited oxides have good resolution, but when formed of a sufficient thickness are of poor quality and tend to crack and develop pinholes.

Next, the oxide layer 22 is patterned by conventional photolithographic and etching techniques to open up an aperture in the oxide over the plug 14. Finally, a metallized layer is deposited over the entire substrate and patterned to form the contact 12. It is important that the metal selected for the contact be one that will form a rectifying contact with the plug 14, rather than an ohmic contact. Molybdenum is an example of a suitable metal, and gold may be used if subsequent temperatures are kept below 377°C. if the substrate is silicon. However, it is advantageous to use a layer of molybdenum and a layer of gold. The molybdenum is preferable because it does not alloy with silicon temperatures ordinarily used in manufacture, it adheres reasonably well to silicon and silicon dioxide, it does not alloy with and it not penetrated by gold, and it can be selectively applied with the evaporation and photoresist masking techniques ordinarily used in semiconductor manufacture. Gold is ideal for the top layer because it is highly conductive so that series resistance is not introduced, it adheres to molybdenum, and it can be easily bonded to with the commonly-used small gold wires without the problem of formation of AuAl_2 such as is present when aluminum is used as a contact metal.

Diodes using the configuration illustrated in FIGURE 1 and the above described method have been fabricated in which the epitaxial plugs 14 ranged from about 0.020 to about 0.024 mil deep and were about 1.0 mil in diameter, the diameter of the circular oxide ring 20 was about 10.0 mils, and the deposited oxide films 22 were about 8,000 angstroms thick, thereby providing a total oxide thickness of about 13,000 angstroms. The junction diameter between the metal 12 and epitaxial plug 14, that is the diameter of the hole cut in the deposited oxide layer 22, was slightly less than 1.0 mil. The diodes were tested in packages having a capacity of about 0.16 picofarad. Using these packages, the typical device parameters were:

Forward Voltage at 10mA	~ 0.85 v
Reverse Voltage at 10 μ A	~ 11 v
Total Zero Bias Capacitance at 1 MHz	~ 0.35 pf
Series Resistance	~ 17 ohms

5 Subtracting package capacitance, the total junction capacitance was about 0.19 pf. The series resistance was higher than expected, as was the zero bias capacitance, but the higher values may be explained by the auto-doping effect. The devices were designed around 10 3.0 ohm-cm epitaxial material, so that the depletion regions would be about 0.02 mil. Lower resistivity material would result in a narrowed depletion region, so that a higher areal capacity and higher series resistance 15 would appear. It is difficult to measure the

resistivity of very thin epitaxial material because of mechanical problems, so the resistivity must be back-calculated from device parameters. Carrying out this calculation the epitaxial resistivity accounting for the observed capacity and resistance is about 0.1 to 0.5 ohm-cm.

In addition, microwave mixer diodes have also been fabricated using this technique. The electrical parameters obtained in this case were:

Forward Voltage at 10mA	~ .85 v
Reverse Voltage at 10 μ A	~ 14 v
Total Zero Bias Capacitance at 1 MHz	~ .8 pf
Noise Figure at 8.3 GHz	~ 8—10 db
Rectified Current	~ 0.2—0.4 mA

The higher zero bias capacity for these devices is the result of higher package capacity.

35 Referring now to FIGURE 3, an X-band hybrid mixer circuit for mixing a 9 GHz incoming signal with an 8.5 GHz local oscillator to produce a 500 MHz IF frequency is indicated generally by the reference numeral 40 50. The hybrid mixer circuit is formed by metallized strip lines deposited directly on a high resistivity silicon or intrinsic gallium arsenide substrate with a metallized ground plane formed over the opposite surface. The particular configuration and operation of the hybrid mixer circuit 50 is known in the art and therefore does not, per se, constitute a part of the present invention. In general, interconnecting strip lines 56, 57, 58 and 59 50 form a 3 db hybrid conductor pattern where the input signals are mixed, transformed and applied to two diode structures 60 which are located at the ends of one-quarter wavelength filter sections 61 and 62 so as to 55 prevent X-band energy from reaching the IF amplifier stage.

The diodes 60 are constructed in accordance with this invention and one diode is illustrated in FIGURES 4 and 5. As can be seen in FIGURE 5, the high resistivity silicon or intrinsic gallium arsenide substrate 64 has a metallized ground plane 66 on one surface. The diode 60 is comprised of a diffused region 68 having a configuration as 60 shown in dotted outline in FIGURE 4 which provides low resistivity for ohmic contact with a strip line as will presently be described. An oxide film 70, preferably thermally grown, is formed over the substrate 64 to a thickness corresponding to the thickness desired of the high resistivity epitaxial plug which is to be 70 deposited. The oxide film 70 is patterned by

photolithographic techniques to form a peripheral frame defining an elongated slot 72 as can best be seen in dotted outline in FIGURE 4. A high resistivity epitaxial layer 74 is then deposited over the exposed surface of the substrate around the silicon oxide frame 70 and within the elongated opening 72 to form an elongated epitaxial plug 74a. A low temperature oxide film 76 is then deposited over the substrate and is patterned and etched using a standard photolithographic technique to form one elongated slot 78 extending transversely across the elongated epitaxial plug 74a. It is important that the period of time during which the oxide is exposed to the etchant be controlled so that the first oxide layer 70 will not also be etched away. A second photolithographic and etching procedure is then performed to cut openings 80 and 82 through both oxide layers 70 and 76 to expose the opposite ends of the diffused region 68.

A metal film is then deposited over the substrate and is patterned to form the strip lines 61a and 61b, respectively. The strip lines 61a and 61b must be of the type which will make ohmic contact with the low resistivity diffused region 68 while making a rectifying contact with the high resistivity epitaxial plug 74a. This metal may be molybdenum or gold, but is preferably a layer of each as previously described. It will be appreciated that this technique permits an extremely small junction area, defined by the square 84, between a metal and a high resistivity semiconductor of controlled thickness and controlled impurity while at the same time providing a surface oriented structure on an intrinsic substrate capable of carrying high frequency strip lines.

Referring now to FIGURE 6, an integrated circuit fabricated by the method of the present invention is indicated generally by the reference numeral 100. The circuit 100 includes a transistor 102 and a metal-semiconductor diode 103. Both the transistor and the diode have a planar configuration. An equivalent circuit of the device 100 is shown in FIGURE 6a. The transistor 102 is of conventional construction and comprises an N-type collector diffusion 104 which is made in a P-type substrate 106, a P-type base region 108 diffused into the collector region 104, and finally an N-type emitter region 110 diffused into the base region. An N-type region 112 is diffused at the same time that the N-type collector region 104 is diffused, and a lower resistivity N-type region 114 is diffused when the emitter region 110 is diffused. During the diffusion processes, an oxide film 116 is thermally grown on the silicon substrate 106 the thickness of which can be precisely determined. The oxide film 116 may then be increased in thickness if necessary, but in any event serves as the fiducial thickness marker from which the thickness of the epitaxial layer which is to be deposited can be controlled. The oxide layer 116 is then patterned to form an opening 118 over the surface of the N-type region 112 and to remove the oxide in all areas where epitaxial material formed on the substrate 106 will be of no consequence. It will be noted, however, that the oxide film 116 completely covers the N-type region 112 and the N-type collector region 104 of the transistor 102, although the two areas are separated. Next, an epitaxial layer 120 is formed on the substrate. As previously described, the epitaxial material is deposited only on the exposed surface of the P-type substrate 106 and does not grow on the oxide layer 116. An epitaxial plug 120a of predetermined thickness is formed in the opening 118, and the thickness can be precisely determined and controlled from the fiducial thickness marker provided by the oxide film. A second low temperature oxide layer 122 is then formed over the entire substrate and pattern to expose contact areas over the epitaxial plug 120a, the low resistivity N-type region 114, the base region 108, the emitter region 110, and the collector region 104 as illustrated. A metallized film is then deposited over the entire substrate and patterned to provide interconnecting conductors and expanded contacts. The metallized film must be selected so as to make ohmic contact with the relatively low resistivity semiconductor regions while making rectifying contact with the high resistivity epitaxial plug 120a. Examples of the metals which may be used are gold and molybdenum, or layers of each as heretofore described.

Thus the metallized films 124—127 form the conductors illustrated by corresponding

reference numerals in the schematic circuit diagram of FIGURE 6a. The diode 103 has a rectifying junction between the metal film strip 124 and the epitaxial plug 120a. The epitaxial plug 120a may have a high resistivity and controlled thickness so as to have the advantages heretofore described. The lower resistivity N-type regions 112 and 114 reduce the series resistance of the diode and provide ohmic contact with the conductor 125 as heretofore described.

Referring now to FIGURE 7, a PNP transistor constructed in accordance with the present invention is indicated generally by the reference numeral 150. The transistor 150 is fabricated on a low resistivity P-type substrate 152. A metallized collector contact 154 is deposited on one surface of the substrate. A P-type epitaxial layer 156 of high resistivity is formed over the other surface of the substrate 152. An oxide layer 158 is grown over the substrate to the desired thickness to provide a fiducial thickness marker and is then patterned to form a frame defining an opening 160 and expose a predetermined area of the P-type epitaxial layer 156. An N-type epitaxial layer 162 is then deposited over the substrate and forms an epitaxial plug 162a of a thickness which can be precisely determined from the thickness of the oxide layer and which can therefore be precisely controlled. Another oxide film 164 is then deposited over the substrate, preferably at a low temperature, and a P-type emitter region 166 diffused through an opening cut by photolithographic techniques in the oxide film. The depth of the emitter diffusion 166 may be very shallow and may be precisely controlled so as to retain control of the base width of the transistor. The oxide film 164 is again pattern by photolithographic and etching techniques to expose the base region 162a and the emitter region 166 and a metallized film deposited over the substrate. The metallized film is then patterned by conventional photolithographic and etch techniques to leave expanded base and emitter contacts 168 and 170.

If desired, the emitter region may also be formed epitaxially using the same process as is used to form the base region to provide an edge isolated transistor. Also, the transistor can have a planar configuration merely by making contact through the oxide layers 158 and 164 to the collector region 156.

Figures 8 and 8a illustrate a device 200 comprising a PNP transistor and a Schottky diode fabricated in a single body of semiconductor material. This device is also disclosed in the Specification of copending Application No. 56041/68 (Serial No. 1154892) divided out of the present Application. The device 200 is comprised of a metallized film 202 which serves as the collector

contact, a low resistivity P-type substrate 204, and a higher resistivity P-type epitaxial layer 206. An N-type base region 208 is formed in the epitaxial layer 206 and then a P-type emitter region 210 is diffused into the base region 208, using conventional diffusion techniques. The oxide film over the substrate, and in particular that portion of the oxide film over the base region 208, can be precisely measured. The oxide film 212 is then patterned by photolithographic and etching techniques to provide a window frame about an opening 214 over the base region 208. An epitaxial layer 216 is then formed over the surface of the substrate and forms an epitaxial plug 216a within the opening 214. The thickness of the epitaxial layer 216 may be precisely controlled by reference to the thickness of the oxide layer 212. A second oxide layer 218 is formed over the entire substrate, preferably by oxidative techniques, rather than thermal techniques, so as to keep the temperature at a sufficiently low temperature as not to materially disturb the diffusions previously established in forming the base and emitter regions 208 and 210. The oxide is then patterned using conventional photolithographic and etching techniques to expose the surface of the epitaxial plug 216a, the base region 208 and the emitter region 210 and a metallized film deposited over the surface of the substrate. When the metallized film is patterned by photolithographic and etching techniques, an anode contact 220 for the diode, a base contact 222 and an emitter contact 224 remain. It is important that the metallized film forming the three contacts be such as to provide a rectifying junction between the metal and the high resistivity N-type epitaxial plug 216a while at the same time forming an ohmic contact with the lower resistivity base and emitter regions 208 and 210. Molybdenum and/or gold may be used for this purpose. Then by merely connecting the anode contact 220 to the collector contact 202 the circuit illustrated in FIGURE 8a is provided. In FIGURE 8a the corresponding conductors are designated by corresponding reference numerals. In operation, the metal-semiconductor diode formed between the metallized contact 220 and the epitaxial plug 216a has a lower forward conduction voltage than does the junction between the collector region 206 and base region 208 so that the collector-base junction of the transistor can never become forward biased regardless of the magnitude of the signal used to drive the base.

Although preferred illustrative embodiments of the invention have been described in detail, it is to be understood that various changes, substitutions and alterations can be made in the embodiments described without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A semiconductor device including a body of monocrystalline semiconductor material and a distinct region of monocrystalline semiconductor material comprising an epitaxial deposit on and upstanding from a plane surface portion of the said body, the upstanding region being edge isolated by continuous insulating material which leaves uncovered at least part of the surface of the upstanding region opposite the said surface of the body, and an electrical contact to the upstanding region, the contact covering the surface area of the upstanding region not covered by the insulating material and extending on to the insulating material. 70
2. A semiconductor device according to Claim 1, in which the electrical contact is a flanged metallic plug, the flange of which is positioned on electrically insulating material standing proud of the said surface of the region with the base of the plug positioned on the said surface of the region. 75
3. A semiconductor device according to Claim 1 or Claim 2, in which the contact is a metal layer making rectifying contact with the said surface of the region to form a metal-semiconductor barrier diode junction. 80
4. A semiconductor device according to Claim 3, in which the metal layer is composed of gold, or of molybdenum, or of molybdenum overlaid by gold. 85
5. A semiconductor device according to Claim 4, in which the upstanding region and the semiconductor body are composed of N-type silicon. 90
6. A semiconductor device according to any one of Claims 3—5, in which the upstanding region has higher resistivity than and like conductivity-type as the body of semiconductor material. 95
7. A semiconductor device according to any one of Claims 1—6, in which the body of semiconductor material is a region of or on a substrate of a semiconductor material. 100
8. A semiconductor device according to any one of Claims 3—5, in which the semiconductor body is a diffused region in a semiconductor substrate, the diffused region being overlaid by the said insulating material. 105
9. A semiconductor device according to Claim 8, in which the upstanding region has like conductivity-type as and higher resistivity than the diffused region. 110
10. A semiconductor device according to Claim 9, including an ohmic contact to the said diffused region, the ohmic contact being positioned on and extending through the insulating material. 115
11. A semiconductor device according to Claim 10, in which the diffused region includes a region of lower resistivity than and like conductivity-type to the diffused region, the ohmic contact being attached to the said lower resistivity region. 120



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contact, a low resistivity P-type substrate 204, and a higher resistivity P-type epitaxial layer 206. An N-type base region 208 is formed in the epitaxial layer 206 and then a P-type emitter region 210 is diffused into the base region 208, using conventional diffusion techniques. The oxide film over the substrate, and in particular that portion of the oxide film over the base region 208, can be precisely measured. The oxide film 212 is then patterned by photolithographic and etching techniques to provide a window frame about an opening 214 over the base region 208. An epitaxial layer 216 is then formed over the surface of the substrate and forms an epitaxial plug 216a within the opening 214. The thickness of the epitaxial layer 216 may be precisely controlled by reference to the thickness of the oxide layer 212. A second oxide layer 218 is formed over the entire substrate, preferably by oxidative techniques, rather than thermal techniques, so as to keep the temperature at a sufficiently low temperature as not to materially disturb the diffusions previously established in forming the base and emitter regions 208 and 210. The oxide is then patterned using conventional photolithographic and etching techniques to expose the surface of the epitaxial plug 216a, the base region 208 and the emitter region 210 and a metallized film deposited over the surface of the substrate. When the metallized film is patterned by photolithographic and etching techniques, an anode contact 220 for the diode, a base contact 222 and an emitter contact 224 remain. It is important that the metallized film forming the three contacts be such as to provide a rectifying junction between the metal and the high resistivity N-type epitaxial plug 216a while at the same time forming an ohmic contact with the lower resistivity base and emitter regions 208 and 210. Molybdenum and/or gold may be used for this purpose. Then by merely connecting the anode contact 220 to the collector contact 202 the circuit illustrated in FIGURE 8a is provided. In FIGURE 8a the corresponding conductors are designated by corresponding reference numerals. In operation, the metal-semiconductor diode formed between the metallized contact 220 and the epitaxial plug 216a has a lower forward conduction voltage than does the junction between the collector region 206 and base region 208 so that the collector-base junction of the transistor can never become forward biased regardless of the magnitude of the signal used to drive the base.

Although preferred illustrative embodiments of the invention have been described in detail, it is to be understood that various changes, substitutions and alterations can be made in the embodiments described without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A semiconductor device including a body of monocrystalline semiconductor material and a distinct region of monocrystalline semiconductor material comprising an epitaxial deposit on and upstanding from a plane surface portion of the said body, the upstanding region being edge isolated by continuous insulating material which leaves uncovered at least part of the surface of the upstanding region opposite the said surface of the body, and an electrical contact to the upstanding region, the contact covering the surface area of the upstanding region not covered by the insulating material and extending on to the insulating material.

2. A semiconductor device according to Claim 1, in which the electrical contact is a flanged metallic plug, the flange of which is positioned on electrically insulating material standing proud of the said surface of the region with the base of the plug positioned on the said surface of the region.

3. A semiconductor device according to Claim 1 or Claim 2, in which the contact is a metal layer making rectifying contact with the said surface of the region to form a metal-semiconductor barrier diode junction.

4. A semiconductor device according to Claim 3, in which the metal layer is composed of gold, or of molybdenum, or of molybdenum overlaid by gold.

5. A semiconductor device according to Claim 4, in which the upstanding region and the semiconductor body are composed of N-type silicon.

6. A semiconductor device according to any one of Claims 3—5, in which the upstanding region has higher resistivity than and like conductivity-type as the body of semiconductor material.

7. A semiconductor device according to any one of Claims 1—6, in which the body of semiconductor material is a region of or on a substrate of a semiconductor material.

8. A semiconductor device according to any one of Claims 3—5, in which the semiconductor body is a diffused region in a semiconductor substrate, the diffused region being overlaid by the said insulating material.

9. A semiconductor device according to Claim 8, in which the upstanding region has like conductivity-type as and higher resistivity than the diffused region.

10. A semiconductor device according to Claim 9, including an ohmic contact to the said diffused region, the ohmic contact being positioned on and extending through the insulating material.

11. A semiconductor device according to Claim 10, in which the diffused region includes a region of lower resistivity than and like conductivity-type to the diffused region, the ohmic contact being attached to the said lower resistivity region.



12. A semiconductor device according to Claim 1, in which the semiconductor body is an elongated diffused region in a substrate and the upstanding region is elongated and located wholly within the area of the surface where the diffused regions is exposed, the contact to the upstanding region is a metal strip overlying the insulating material, extending transversely across the elongated upstanding region and making rectifying contact with the said surface of that region to form a metal-semiconductor barrier diode, and including a metallic film overlying the insulating material and extending into ohmic contact with opposite ends of the diffused region.

13. A semiconductor device according to any one of Claims 9—11, in which the substrate includes further diffused regions, displaced from the first-mentioned diffused region, extending to the same surface of the substrate to provide emitter, base and collector regions of a planar transistor.

14. A semiconductor device according to Claim 9 or Claim 10, in which the diffused region is the base region of planar transistor, the base region being surrounded by a substrate region forming the collector region of the transistor, and the base region includes an emitter region spaced from the said upstanding region.

15. A semiconductor device according to any one of the preceding claims in which the upstanding region has a thickness not greater than the normal depletion width of the material of that region.

16. A semiconductor device according to Claim 7, in which the said upstanding region has a conductivity-type opposite to the conductivity-type of the said substrate region.

17. A semiconductor device according to Claim 1 or Claim 2, in which the body of semiconductor material is a region of one conductivity type in a semiconductor substrate and forms the collector region of a transistor, the upstanding region has opposite conductivity-type and forms the base region of the transistor, an emitter region in and extending to the said surface of the upstanding region, and a further electrical contact to the emitter region positioned on the insulating material.

18. A process for fabricating a semiconductor device, including the steps of forming an insulating oxide layer on a surface of a monocrystalline semiconductor substrate to leave a region of that surface uncovered and surrounded by oxide material, epitaxially depositing semiconductor material on the said uncovered surface region to form a region upstanding from that surface and surrounded by contiguous oxide material, forming further insulating oxide material at least one the first mentioned oxide layer, the further oxide material having an aperture leaving at least part of the surface area of the upstanding

region opposite the said substrate surface, and forming a metallic contact positioned at least partly on the further layer of oxide material and covering the surface area of the upstanding region bounded by the said aperture opposite the said substrate surface, the contact making electrical connection with the upstanding region.

19. A process according to Claim 18, the oxide layer defining a peripheral frame surrounding the said uncovered region, the extent of the oxide layer along the said substrate surface having been selected to inhibit growth of semiconductor material on the oxide layer.

20. A process according to Claim 18 in which the said contact is formed in the shape of a plug having a flange positioned on the further oxide material.

21. A process according to any one of Claims 18—20, the metallic contact making rectifying contact with the said opposite surface of the upstanding region to form a metal-semiconductor barrier diode.

22. A process according to Claim 21, the metallic contact comprising gold, molybdenum, molybdenum overlaid by gold.

23. A process according to Claim 18, wherein prior to the steps recited, first and second spaced regions of one conductivity-type are formed by diffusion into one surface of a monocrystalline semiconductor substrate of opposite conductivity-type, the first and second regions having impurity concentrations suitable for a collector region, a base region of the said opposite conductivity-type is formed by diffusion in the said first region, third and fourth regions of the said one conductivity-type are formed by diffusion in limited portions of the said base region and the said second region, respectively, the third and fourth regions having impurity concentration suitable for an emitter region; and wherein a first insulating oxide layer of known thickness is formed over the said one surface of the substrate and predetermined portions of the oxide layer are removed to leave the said first region, the base and emitter regions, the said second and fourth regions covered by the oxide layer except for an opening formed over and exposing a limited area of the said second region spaced from the fourth region, epitaxially depositing a layer of semiconductor material of the said one conductivity type and having higher resistivity than the said second region on the exposed portions of the said substrate surface, the epitaxial layer having a predetermined thickness relative to that of the first oxide layer, forming a second insulating oxide layer over the said substrate surface and making openings in that oxide layer to provide access to the said epitaxial layer, the said first, third, and fourth regions and the base regions, depositing a metallic film over the second layer to make contact with the epitaxial layer to

form a metal-semiconductor barrier diode and to make ohmic contact with the said first, third, fourth and base regions, and removing selected parts of the metallic film to form

conductors extending from the said first, third, fourth and base regions and from the said epitaxial layer.

24. A process according to Claim 18, the substrate being of one conductivity type and the epitaxially deposited region having an opposite conductivity type; and in which following the said epitaxial deposition a region of the said one conductivity type is formed by diffusion in a limited portion of the said epitaxial region, and a metal film is formed on a second insulating oxide layer overlying the first mentioned oxide layer, the epitaxial region and the diffused region, selected parts of the metal film being removed to form conductors making ohmic contact with the epitaxial region and the diffused region respectively through apertures in the second oxide layer.

25. A process according to Claim 18, in which prior to the steps recited a first region of one conductivity type and having an impurity concentration suitable for a base region is formed by diffusion into one surface of a region of monocrystalline substrate of opposite conductivity-type and having an impurity concentration suitable for a collector region, and a second region of the said opposite conductivity-type is formed by diffusion into a limited area portion of the first region, the second region having an impurity concentration suitable for an emitter region; and in which a first insulating oxide layer of known predetermined thickness is formed over the said one surface of the substrate, the said oxide layer having an opening therein leaving exposed a surface area of the said first region spaced laterally from the said second region, epitaxially depositing semiconductor material of higher resistivity than and of like conductivity type to the said first region in the said opening to form the said upstanding region, forming a second insulating oxide layer overlying the first-mentioned oxide layer and depositing a metal film over the second oxide layer to make rectifying contact with the epitaxial region to form a metal-semiconductor barrier diode and to make ohmic contact with the said first and second regions, and removing selected parts of the metal film to form conductors extending from the said first, second and epitaxial regions.

26. A process according to Claim 18, wherein, prior to the steps recited, an elongated low resistivity diffused region is formed in the substrate, the latter having high re-

sistivity; and wherein the oxide layer is a frame having an opening defining an elongated exposed area of the diffused region and covering the remainder of the diffused region, the epitaxial region is formed in the opening of the frame and has a high resistivity; a second insulating oxide layer is formed over the first-mentioned oxide layer and the epitaxial region and an elongated opening is formed only in the said second oxide layer to extend transversely across the said epitaxial region; openings are formed in both oxide layers over the opposite ends of the said diffused region; a metal film is deposited on the second oxide layer to make rectifying contact with the exposed surface of the epitaxial region and ohmic contact with the said diffused region through the openings in the oxide layers; and in which selected portions of the metal film are removed to form one conductor extending into contact with the epitaxial region and another conductor extending into contact with the said diffused region at the opposite ends thereof.

27. A process according to any one of Claims 24—27, in which the semiconductor material is silicon and the contacts are formed of gold, molybdenum or molybdenum overlaid by gold.

28. A process according to any one of Claims 18—28, in which the epitaxial region has a thickness substantially equal to or less than the depletion width of the semiconductor material used to form the epitaxial region.

29. A method of manufacturing a metal-semiconductor barrier diode substantially as described herein with reference to and as illustrated by Figs. 1 and 2 of the accompanying drawings.

30. A method of manufacturing a hybrid mixer substantially as described herein with reference to and as illustrated by Figs. 3—5 of the accompanying drawings.

31. A method of manufacturing a combination metal-semiconductor barrier diode-transistor device substantially as described herein with reference to and as illustrated by Fig. 6 or Fig. 8 of the accompanying drawings.

32. A method of manufacturing a planar transistor substantially as described herein with reference to and as illustrated by Fig. 7 of the accompanying drawings.

ABEL & IMRAY,
Chartered Patent Agents,
Quality House,
Quality Court,
Chancery Lane,
London, W.C.2.

