CLAIMS

1. A differential mixed-signal logic processor, comprising:

a plurality of mixed-signal multiplier branches for multiplication of an analog value *A* and a *N*-bit digital value *B*, each of the plurality of mixed-signal multiplier branches include:

a first capacitor connected across a second capacitor and a third capacitor to provide a differential output across the second and third capacitors,

wherein a capacitance of the first capacitor is equal to half a capacitance of the second and third capacitors.

2. The differential mixed-signal logic processor of claim 1, further comprising:

a positive supply node connected to a first end of the first capacitor;

a negative supply node connected to a second end of the first capacitor.

3. The differential mixed-signal logic processor of claim 1, further comprising:

a first set of switches comprising a first, a second, and a third switch, each having a first end coupled to the positive supply node; and

a second set of switches comprising a fourth, a fifth, and a sixth switch, each having a first end coupled to the negative supply node.

4. The differential mixed signal logic processor of claim 1, wherein second ends of the first and fourth switches are connected to a positive input voltage, wherein second ends of the second and fifth switches are connected to a negative input voltage, wherein a second end of the third switch is connected to the first end of the second capacitor and to a positive output node, and wherein a second end of the sixth switch is connected to the first end of the third capacitor and to a negative output node.

5. The differential mixed-signal logic processor of claim 4, wherein second ends of the second and third capacitors are connected to ground.

6. The differential mixed-signal logic processor of claim 4, wherein the first and second switches provides complimentary inputs to the positive supply node, and wherein the fourth and fifth switches provide complimentary inputs to the negative supply node.

7. The differential mixed-signal logic processor of claim 4, wherein the differential mixed-

signal logic processor is configured to compute a dot product between an analog value vector and a digital value vector.

8. The differential mixed-signal logic processor of claim 7, wherein the differential mixed-signal logic processor is comprised in a system having at least one sensor and a memory device, wherein the analog value vector is received from the at least one sensor and the digital value is received from the memory device.

9. The differential mixed-signal logic processor of claim 7, wherein a sample mode samples the analog value vector using ~~the~~ a single branch-dedicated capacitor in each of the plurality of mixed-signal multiplier branches to store a sample value.

10. The differential mixed-signal logic processor of claim 4, wherein a capacitance of the first capacitor is equal to half a capacitance of any of the second and third capacitors.

11. The differential mixed-signal logic processor of claim 4, wherein capacitor-wise, each of the plurality of mixed-signal multiplier branches include only the three dedicated capacitors.

12. The differential mixed-signal logic processor of claim 4, wherein the various modes of the differential mixed-signal logic processor comprises a reset mode, a sample mode~~, a merge mode~~, and an accumulate mode.

13. The differential mixed-signal logic processor of claim 4, wherein during an accumulation mode of the differential mixed-signal logic processor, the positive supply node and the positive output node are charge shared, and the negative supply node and the negative output node are charge shared.

14. The differential mixed-signal logic processor of claim 4, wherein during a reset mode of the differential mixed-signal logic processor, the positive supply node and the negative supply node have a same potential.

15. The differential mixed-signal logic processor of claim 4, wherein the first and second switches form a first switch pair, and the fourth and fifth switches form a second switch pair, and wherein the switches in each of the first and second switch pairs are complimentary to each other

in either supplying one of the positive input voltage or the negative input voltage at a given time.

16. The differential mixed-signal logic processor of claim 4, further comprising:

a positive supply rail connected to the positive output node; and

a negative supply rail connected to the negative output node,

wherein the positive and negative supply rails are deployed for a multiplier and accumulator operation.

17. The differential mixed-signal logic processor of claim 4, wherein a charge-sharing operation is performed to connect the positive supply rail to the positive output node, and the negative supply rail to the negative output node.

18. The differential mixed-signal logic processor of claim 1, wherein the multiplication of the analog value *A* and the *N*-bit digital value *B*, wherein the N-bit digital value *B* is calculated $B = 2^{N-1}b_{N-1} + 2^{N-1}b_{N-2} \ldots + 2^{0}b_{0}$, where b_n is a binary value at an n-th bit position.

19. A method for forming a differential mixed-signal processor, comprising:

arranging each a plurality of mixed-signal multiplier branches for multiplication of an analog value and a *N*-bit digital value *B* to include a first capacitor connected across a second capacitor and a third capacitor to provide a differential output across the second and third capacitors,

wherein a capacitance of the first capacitor is equal to half a capacitance of the second and third capacitors.

20. The method of claim 19, further comprising arranging the each of the plurality of mixed-signal multiplier branches to have a positive supply node connected to a first end of the first capacitor, and a negative supply node connected to a second end of the first capacitor.