CLAIMS

1.A memory, comprising:

a substrate, on which first fins and second fins are separately disposed, wherein at least two first fins are disposed between adjacent second fins, a spacing between the adjacent first fins is smaller than a spacing between the first fin and the second fin; a surface of the substrate is provided with an isolating structure comprising a first isolating structure and a second isolating structure, the first isolating structure is disposed between the adjacent first fins, and the second isolating structure is disposed between the first fin and the second fin; a dielectric layer covers tops of the first fins, side wall surfaces of the first fins exposed by the first isolating structure, tops of the second fins and side wall surfaces of the second fins exposed by the second isolating structure; wherein in a direction perpendicular to the extending direction of a word line, a depth of the first isolating structure is smaller than a depth of the second isolating structure;

work function layers disposed on a surface of the dielectric layer, wherein the work function layers comprise a first work function layer covering the whole surface of the dielectric layer and a second work function layer which is disposed on the first work function layer on side walls where the at least two first fins are opposite, wherein in a direction parallel to an arrangement direction of the first fins and the second fins, the first work function layer and the second work function layer on the side walls where the at least two first fins are opposite are provided with a first thickness, the first work function layer on side walls where the first fins face towards the second fins is provided with a second thickness, and the first thickness is greater than the second thickness; and

a conductive layer disposed on surfaces of the work function layers, wherein the conductive layer is the word line.

2.The memory of claim 1, wherein in a direction where the substrate points to the first fins, the dielectric layer and the first isolating structure are enclosed into a first filling region

in an area where the adjacent first fins are opposite, and the first filling region is filled up with the work function layers.

3.The memory of claim 1, wherein a gap is formed between the work function layers on the side walls where the at least two first fins are opposite.

4.The memory of claim 1, wherein materials of the first work function layer are identical with materials of the second work function layer.

5.The memory of claim 1, wherein the first thickness is in a range of 5 nm to 50 nm, and the second thickness is in a range of 2 nm to 30 nm.

6.The memory of claim 1, wherein difference between the first thickness and the second thickness is in a range of 3 nm to 30 nm.

7.The memory of claim 1, wherein work functions of the work function layers are greater than a work function of the conductive layer.

8.The memory of claim 7, wherein materials of the work function layers include titanium nitride, cobalt or nickel.

9.A manufacturing method of a memory, comprising:

providing a substrate, on which first fins and second fins are separately disposed, wherein at least two first fins are disposed between adjacent second fins, a spacing between the adjacent first fins is smaller than a spacing between the first fin and the second fin; a surface of the substrate is provided with an isolating structure comprising a first isolating structure and a second isolating structure, the first isolating structure is disposed between the

adjacent first fins, and the second isolating structure is disposed between the first fin and the second fin;

forming a dielectric layer on tops of the first fins, side wall surfaces of the first fins exposed by the first isolating structure, tops of the second fins and side wall surfaces of the second fins exposed by the second isolating structure;

forming work function layers on a surface of the dielectric layer, wherein the forming the work function layers comprises: forming a first work function layer on the whole surface of the dielectric layer; forming a second work function layer which is disposed on the first work function layer on side walls where the at least two first fins are opposite; wherein in a direction parallel to an arrangement direction of the first fins and the second fins, the first work function layer and the second work function layer on the side walls where the at least two first fins are opposite are provided with a first thickness, the first work function layer on side walls where the first fins face towards the second fins is provided with a second thickness, and the first thickness is greater than the second thickness; and

forming a conductive layer on surfaces of the work function layers, wherein a work function value of the conductive layer is smaller than work function values of the work function layers;

wherein the forming the second work function layer comprises:

forming a sacrificial layer on a surface of the first work function layer;

removing the sacrificial layer in an area where the adjacent first fins are opposite;

forming the second work function layer on the surface of the first work function layer in the area where the adjacent first fins are opposite; and

removing the sacrificial layer in an area where the first fin is opposite to the second fin.

10.The manufacturing method of the memory of claim 9, wherein in a direction where the substrate points to the first fins, the dielectric layer and the first isolating structure are enclosed into a first filling region in an area where the adjacent first fins are opposite;

wherein the forming the work function layers comprise:

forming the work function layers on the whole surface of the dielectric layer until the first filling region is filled up.