package 102 can be tested prior to assembly, which improves manufacturing yields and reduces the cost.

The number and location of the stacked integrated circuit die 136 and the base integrated circuit die 104 is an example only and other configurations are possible. In each case multiple die may be stacked within the packages.

Referring now to FIG. 2, therein is shown a cross-sectional view of an integrated circuit packaging system 200 with package-on-package stacking, in a second embodiment of the present invention. The cross-sectional view of the integrated circuit packaging system 200 depicts a base package 202 having the base integrated circuit die 104 mounted on the component side 106 of the substrate 108.

The substrate 108, such as a laminate substrate or ceramic substrate, has the system side 110 with the vias 112 coupling the contacts 114 on the system side 110 to the contacts 114 on the component side 106. The base integrated circuit die 104 may be mounted on the component side 106 by the adhesive 116, such as a die attach material.

The electrical interconnects 118, such as bond wires, may couple the base integrated circuit die 104 to the contacts 114 on the component side 106. The stacked interconnects 126, such as solder balls, solder columns, or stud bumps, may be mounted on the contacts 114 of the component side 106 as well. A molded base package body 204 may encapsulate the base integrated circuit die 104, the electrical interconnects 118, the stacked interconnects 126, and a portion of the component side 106. None of the contacts 114 on the component side 106 remain exposed but the top of the stacked interconnects 126 may protrude through the molded base package body 204 for further connection.

The system interconnects 122, such as solder balls, solder bumps, solder columns, or stud bumps, may be formed on the contacts 114 of the system side 110 of the substrate 108. The system interconnects 122 may be electrically connected to the contacts 114 on the component side 106, the base integrated circuit die 104, or the combination thereof.

A top package 206 may be coupled to the substrate 108 of the base package 202 through the stacked interconnects 126 by the through silicon via interposer 128, such as an integrated circuit die, having the through silicon vias 130 coupled ~~to~~on the stacked interconnects 126, which are on the substrate 108. The through silicon via interposer 128 may have the active side 132 and the back side 134. The active side 132 of the through silicon via interposer 128 may include integrated circuits (not shown).

The stacked integrated circuit die 136 may be mounted on the active side 132 by the

adhesive 116. The electrical interconnects 118 may couple the stacked integrated circuit die

The top package 124 may include the stacked interconnects 126, such as solder balls, solder columns, or stud bumps. The through silicon via interposer 128, such as an integrated circuit die having the through silicon vias 130 may be coupled to the stacked interconnects 126. The through silicon via interposer 128 may have the active side 132 and the back side 134. The active side 132 of the through silicon via interposer 128 may include integrated circuits (not shown).

The stacked integrated circuit die 136 may be mounted on the active side 132 by the adhesive 116. The electrical interconnects 118 may couple the stacked integrated circuit die 136 to the through silicon vias 130 on the active side 132. The resulting circuit may electrically connect the stacked integrated circuit die 136, the through silicon via interposer 128, the base integrated circuit die 304, the system interconnects 122, or a combination thereof.

The top package body 138 may be formed by molding an epoxy molding compound to encapsulate the stacked integrated circuit die 136, the electrical interconnects 118, as well as the active side 132 and the vertical sides 140 of the through silicon via interposer 128. The top package body 138 leaves the back side 134 of the through silicon via interposer 128 exposed.

Referring now to FIG. 4, therein is shown a cross-sectional view of an integrated circuit packaging system 400 with package-on-package stacking, in a fourth embodiment of the present invention. The cross-sectional view of the integrated circuit packaging system 400 depicts the base package 102 with a top package 402 ~~coupled~~ attached to the contacts 114 on the component side 106 of the substrate 108 by the stacked interconnects 126.

The top package 402 may include the stacked interconnects 126, such as solder balls, solder columns, or stud bumps. The through silicon via interposer 128, such as an integrated circuit die, having the through silicon vias 130 may be ~~coupled~~ attached to the stacked interconnects 126. The through silicon via interposer 128 may have the active side 132 and the back side 134. The active side 132 of the through silicon via interposer 128 may include integrated circuits (not shown).

A stacked integrated circuit die 404, such as a flip chip integrated circuit die, may be mounted on the active side 132 by chip interconnects 406. An underfill material 408 may be applied between the active side 132 and the stacked integrated circuit die 404. The stacked integrated circuit die 404 may be coupled through the through silicon vias 130 on the active side 132. The resulting circuit may electrically connect the stacked integrated circuit die 404,

What is claimed is:

1. A method of manufacture of an integrated circuit packaging system comprising:

forming a top package including:

providing a through silicon via interposer having a through silicon via,

coupling a stacked integrated circuit die to the through silicon via, and

~~testing the top package~~ forming a top package body on the stacked integrated circuit die and the through silicon via interposer with a back side of the through silicon via interposer exposed from the top package body;

attaching a stacked interconnect directly on and between the through silicon via and a substrate; and~~;~~

forming a base package including:

~~providing a substrate,~~

coupling a base integrated circuit die to the substrate, and

~~testing the base package; and~~

~~coupling a stacked interconnect between the top package and the base package~~

forming a molded base package body encapsulating the stacked interconnect, a top portion of the stacked interconnect exposed and protruding from the molded base package body.

2. The method as claimed in claim 1 ~~further comprising~~ wherein forming the top package body includes molding an epoxy ~~a~~ molding compound on the stacked integrated circuit die and the through silicon via interposer.

3. The method as claimed in claim 1 further comprising:

forming a stacked integrated package containing the stacked integrated circuit die; and

coupling an electrical interconnect between the stacked integrated package and the through silicon via interposer.

4. The method as claimed in claim 1 wherein forming the top package includes:

coupling an additional through silicon via interposer to the through silicon via interposer by an interposer interconnect~~; and~~

~~forming a molding compound on the through silicon via interposer, the additional through silicon via interposer, and the interposer interconnect including leaving a back side of the through silicon via interposer exposed~~.

5. The method as claimed in claim 1 wherein coupling the stacked interconnect between the top package and the base package includes forming an electrical connection among the stacked integrated circuit die, the through silicon via interposer, the base integrated circuit die, or a combination thereof.

6. A method of manufacture of an integrated circuit packaging system comprising:

forming a top package including:

providing a through silicon via interposer having a through silicon via including providing integrated circuits on the through silicon via interposer,

coupling a stacked integrated circuit die to the through silicon via, and

~~testing the top package;~~ forming a top package body on the stacked integrated circuit die and the through silicon via interposer with a back side of the through silicon via interposer exposed from the top package body;

attaching a stacked interconnect ~~to~~ directly on and between the through silicon via and a substrate; and

forming a base package including:

~~providing a substrate having a component side and a system side,~~

coupling a base integrated circuit die to a component side of the substrate including coupling a contact on the component side to the base integrated circuit die, and

~~testing the base package; and~~

~~coupling a stacked interconnect between the top package and the base package including coupling solder balls, solder columns, or stud bumps between the through silicon via and the contact on the component side~~ forming a molded base package body encapsulating the stacked interconnect, a top portion of the stacked interconnect exposed and protruding from the molded base package body.

7. The method as claimed in claim 6 ~~further comprising~~ wherein forming ~~a molding compound~~ the molded base package body includes forming the molded base package body ~~-~~ on the ~~stacked~~ base integrated circuit die and the substrate ~~through silicon via interposer including leaving a back side exposed~~.

8. The method as claimed in claim 6 further comprising:

forming a stacked integrated package containing the stacked integrated circuit die including molding an integrated package body enclosing the stacked integrated circuit die; and

coupling an electrical interconnect between the stacked integrated package and the through silicon via interposer.

9. The method as claimed in claim 6 wherein forming the top package includes:

coupling an additional through silicon via interposer to the through silicon via interposer by an interposer interconnect including forming a through silicon via interposer stack; and

forming a molding compound on the through silicon via interposer, the additional through silicon via interposer, and the interposer interconnect including leaving a back side of the through silicon via interposer exposed.

10. The method as claimed in claim 6 wherein coupling the stacked interconnect between the top package and the base package includes forming an electrical connection among the stacked integrated circuit die, the through silicon via interposer, the base integrated circuit die, a system interconnect or a combination thereof.

11. An integrated circuit packaging system comprising:

a top package including:

a through silicon via interposer having a through silicon via, ~~and~~

a stacked integrated circuit die coupled to the through silicon via, and

a top package body on the stacked integrated circuit die and the through silicon via interposer with a back side of the through silicon via interposer exposed from the top package body;

a stacked interconnect attached directly on and between the through silicon via and a substrate; and~~;~~

~~forming~~ a base package including:

~~a substrate, and~~

a base integrated circuit die coupled to the substrate~~;~~, and

~~a stacked interconnect between the top package and the base package~~

a molded base package body encapsulating the stacked interconnect, a top portion of the stacked interconnect exposed and protruding from the molded base package body..

12. The system as claimed in claim 11 ~~further comprising~~ wherein the top package body includes an epoxy ~~a~~ molding compound ~~formed~~ molded on the stacked integrated circuit die and the through silicon via interposer.

13. The system as claimed in claim 11 further comprising:

a stacked integrated package contains the stacked integrated circuit die; and

an electrical interconnect between the stacked integrated package and the through silicon via interposer.

14. The system as claimed in claim 11 wherein the top package includes:

an additional through silicon via interposer coupled to the through silicon via interposer by an interposer interconnect~~; and~~

~~a molding compound on the through silicon via interposer, the additional through silicon via interposer, and the interposer interconnect includes a back side of the through silicon via interposer exposed~~.

15. The system as claimed in claim 11 wherein the stacked interconnect between the top package and the base package includes an electrical connection among the stacked integrated circuit die, the through silicon via interposer, the base integrated circuit die, or a combination thereof.

16. The system as claimed in claim 11 further comprising:

an integrated circuit on an active side of the through silicon via interposer;

a contact on ~~the~~a component side of the substrate coupled to the base integrated circuit die; and

solder balls, solder columns, or stud bumps coupled between the through silicon via and the contact on the component side.

17. The system as claimed in claim 16 ~~further comprising~~ wherein ~~a molding compound~~ the molded base package body is on the ~~stacked~~ base integrated circuit die and the ~~through silicon via interposer includes a back side of the through silicon via interposer exposed~~ substrate.

18. The system as claimed in claim 16 further comprising:

a stacked integrated package contains the stacked integrated circuit die includes the stacked integrated circuit die enclosed by an integrated package body; and

an electrical interconnect between the stacked integrated package and the through silicon via interposer.

19. The system as claimed in claim 16 wherein the top package includes:

an additional through silicon via interposer coupled to the through silicon via interposer by an interposer interconnect includes a through silicon via interposer stack formed; and

a molding compound on the through silicon via interposer, the additional through silicon via interposer, and the interposer interconnect includes a back side of the through silicon via interposer exposed.

20. The system as claimed in claim 16 wherein the stacked interconnect between the top package and the base package includes an electrical connection among the stacked integrated circuit die, the through silicon via interposer, the base integrated circuit die, a system interconnect or a combination thereof.