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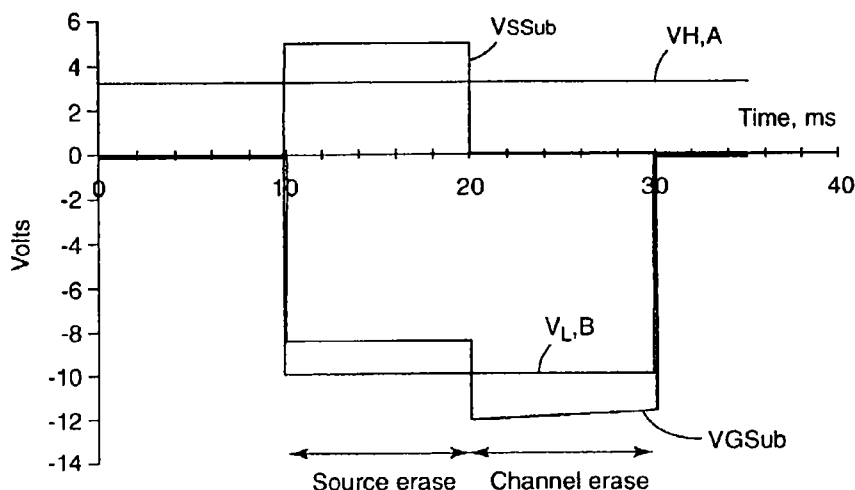
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(54) Title: METHOD AND APPARATUS FOR ERASING FLASH MEMORY



(57) Abstract: Method and apparatus for the erase of non-volatile memory in which holes trapped in the tunnel oxide are reduced. To avoid stress induced leakage current (SILC), which occurs when holes become trapped in the tunnel oxide of a flash memory, the following erase method is proposed. The erase is divided into a source erase (5 volt at source, -10 volt at the gate) followed by a channel erase (0 volt at source and -12 to -15 volt at the gate). The increased negative voltage (-12 to -15) can either be statically supplied by a voltage source or be dynamically generated by a "negative gate bootstrap" or capacitive voltage boosting. For boosting, the transition from source erase to channel erase (switching source rapidly in a fraction of a millisecond from 5 volt to 0 volt) capacitively couples the gate to approximately -15 volt. Boosting is improved, when the parasitic capacitance of the word line drivers is low compared to the capacitance between the source and the control gate of the memory transistor; and is additionally improved, when the drain leakage of the word line drivers is low (GIDL: gate induced drain leakage). Advantageously the word line drivers are provided with LDD (lightly doped drain) and a low k dielectric gate spacer.



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