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(54) Title: METHOD AND APPARATUS FOR DISTRIBUTING A CYCLE CLOCK TO A PLURALITY OF BUS NODES IN A BUS
BRIDGE

(57) Abstract

A bus bridge (20) for interconnecting a plurality of buses (30) which includes a plurality of bridge portals (22), each of which is coupled to a respective one of the buses (30), a plurality of switching subsystems (80, 100, 122, 140, or 150), each of which is coupled to a respective one of the bridge portals (22). The plurality of switching subsystems (80, 100, 122, 140, or 150) collectively constitute a switching system (24) which interconnects the plurality of bridge portals (22). The bus bridge (20) further includes a plurality of cycle clock subsystems (83, 103, 123), each of which is operatively associated with a respective bridge portal (22) and the respective switching subsystem (80, 100, 122, 140, or 150) coupled thereto. Each cycle clock subsystem (83, 103, 123) includes a cycle clock generator (92, 110) which generates a cycle clock, and a cycle counter (90, 112, 121) which receives the cycle clock at a reset input thereof, and which produces a cycle counter output which constitutes a common timing reference for the respective switching subsystem (80, 100, 122, 140, or 150) and the respective bridge portal (22). The bus bridge (20) is preferably an IEEE 1394 serial bus bridge. Various specific implementations of the switching subsystems and bridge portals are disclosed.

