CLAIMS

1. An apparatus, comprising:

a first plurality of memory subblocks of a memory block;

a second plurality of memory subblocks of the memory block;

a first select gate control line associated with the first plurality of memory subblocks, the first select gate control line coupled to a first plurality of select gate switches of the first plurality of memory subblocks, the first plurality of select gate switches coupled to a source;

a second select gate control line associated with the second plurality of memory subblocks, the second select gate control line coupled to a second plurality of select gate switches of the second plurality of memory subblocks, the second plurality of select gate switches coupled to the source;

a first select gate drain control line associated with a first memory subblock of the first plurality of memory subblocks, the first select gate drain control line coupled to a select gate drain switch of the first memory subblock of the first plurality of memory subblocks;

a second select gate drain control line associated with a second memory subblock of the first plurality of memory subblocks, the second select gate drain control line coupled to a select gate drain switch of the second memory subblock of the first plurality of memory subblocks; and

a plurality of memory access lines, each memory access line of the plurality of memory access lines associated with each memory subblock of the first plurality of memory subblocks and each memory subblock of the second plurality of memory subblocks.

2. The apparatus of claim 1, wherein each memory subblock of the first plurality of memory subblocks includes a plurality of strings, each string of the plurality of strings including a first select gate switch coupled to a signal line and a second select gate switch included in the first plurality of select gate switches.

3. The apparatus of claim 2, further comprising:

a control unit configured to selectively enable the first plurality of select gate switches.

4. The apparatus of claim 1, further comprising:

a plurality of select gate control lines, each select gate control line of the plurality of select gate control lines associated with a respective one of the first plurality of memory subblocks.

5. The apparatus of claim 1, wherein the first select gate control line is configured to be active responsive to a read operation being performed on a memory subblock of the first plurality of memory subblocks and the second select gate control line is configured to be inactive responsive to the read

operation being performed on the memory subblock of the first plurality of memory subblocks.

6. The apparatus of claim 1, wherein the first plurality of memory subblocks and the second plurality of memory subblocks include a same number of memory subblocks.

7. The apparatus of claim 1, wherein the apparatus is included in a memory.

8. An apparatus, comprising:

a first select gate source control line associated with a first plurality of memory subblocks;

a second select gate source control line associated with a second plurality of memory subblocks;

a plurality of source gate drain control lines each associated with a respective memory subblock of the first plurality of memory subblocks;

a memory subblock of the first plurality of memory subblocks including a first plurality of select gate source switches, each select gate source switch of the first plurality of select gate source switches coupled to the first select gate source control line and configured to be enabled responsive to receipt of an asserted select gate control signal, the memory subblock of the first plurality of memory subblocks further including a plurality of select gate drain switches, each select gate drain switch of the first plurality of select gate drain switches coupled to a source gate drain control line of the plurality of source gate drain control lines and configured to be enabled responsive to receipt of an asserted select gate drain control signal;

a memory subblock of the second plurality of memory subblocks including a second plurality of select gate source switches, each select gate source switch of the second plurality of select gate source switches coupled to the second select gate source control line and configured to be enabled responsive to receipt of the asserted select gate source control signal; and

a control unit coupled to the first and second select gate source control lines and configured to provide the select gate source control signal to each select gate source switch of the first plurality of select gate source switches using the first select gate source control line responsive to a read operation associated with the memory subblock of the first plurality of memory subblocks, and to provide the select gate source control signal to each select gate source switch of the second plurality of select gate source switches using the second select gate source control line responsive to a read operation associated with the memory subblock of the second plurality of memory subblocks.

9. The apparatus of claim 8, wherein the memory subblock of the first plurality of memory subblocks further includes a plurality of select gate drain switches, each select gate drain switch of the plurality of select gate drain switches configured to be enabled responsive to receipt of a select gate

drain control signal and wherein the control unit is configured to provide the select gate drain control signal to each select gate drain switch of the plurality of select gate drain switches responsive to the read operation associated with the memory subblock of the first plurality of memory subblocks.

10. The apparatus of claim 8, wherein the memory subblock of the first plurality of memory subblocks is a first memory subblock of the first plurality of memory subblocks, the apparatus further comprising a second memory subblock of the first plurality of memory subblocks, the second memory subblock of the first plurality of memory subblocks including a third plurality of select gate source switches, each select gate source switch of the third plurality of select gate source switches coupled to the first select gate source control line and configured to be enabled responsive to receipt of the select gate source control signal.

11. The apparatus of claim 8, wherein the memory subblock of the first plurality of memory subblocks is configured to provide a first capacitive load during the read operation associated with the memory subblock of the first plurality of memory subblocks and the memory subblock of the second plurality of memory subblocks is configured to provide a second capacitive load during the read operation associated with the memory subblock of the second plurality of memory subblocks, the first capacitive load greater than the second capacitive load.

12. The apparatus of claim 8, further comprising:

a memory access line coupled to a plurality of memory cells of the memory subblock of the first plurality of memory subblocks and a plurality of memory cells of the memory subblock of the second plurality of memory subblocks.

13. The apparatus of claim 8, wherein the apparatus is included in a three-dimensional memory array.

14. An apparatus, comprising:

a plurality of select gate source control lines, each select gate source control line of the plurality of select gate source control lines associated with a respective plurality of memory subblocks of a block;

a plurality of select gate drain control lines, each select gate drain control line of the plurality of select gate drain control lines associated with a respective memory subblock of the respective plurality of memory subblocks of the block associated with one of the plurality of select gate source control lines; and

a memory access line associated with each memory subblock of the block, the memory access line substantially parallel to each select gate source control line of the plurality of select gate source control lines.

15. The apparatus of claim 14, further comprising:

a control unit configured to selectively provide a select gate source control signal on each select gate source control line of a plurality of select gate source control lines during a read operation based on a memory subblock of the plurality of memory subblocks associated with the read operation.

16. The apparatus of claim 15, wherein the control unit is further configured to selectively provide a select gate drain control signal on each select gate drain control line of a plurality of select gate drain control lines during the read operation based on the memory subblock of the plurality of memory subblocks associated with the read operation.

17. The apparatus of claim 14, wherein each memory subblock of the block is selectively coupled to a same set of signal lines.

18. A method, comprising:

providing, during a read operation, a first control signal on a first select gate source control line to enable select gate source switches of a first plurality of memory subblocks of a block;

providing, during the read operation, a second control signal on a second select gate source control line to disable select gate source switches of a second plurality of memory subblocks of the block;

providing a third control signal on a first select gate drain control line to enable select gate drain switches of a first memory subblock of the first plurality of memory subblocks; and

providing a fourth control signal on a second select gate drain control line to disable select gate drain switches of a second memory subblock of the first plurality of memory subblocks.

19. The method of claim 18, wherein providing, during a read operation, the first control signal on a first select gate source control line to enable select gate source switches of a first plurality of memory subblocks of a block comprises:

for each memory subblock of the first plurality of memory subblocks of the block, coupling a plurality of strings to a source.

20. The method of claim 18, wherein providing, during the read operation, the second control signal on a second select gate source control line to disable select gate source switches of a second

plurality of memory subblocks of the block causes coupling of a capacitive load in series with a junction capacitance of a select gate source switch.

21. The method of claim 18, further comprising:

applying a first voltage to a memory cell of each memory subblock of the first plurality of memory subblocks associated with a row, and

applying a second voltage lower than the first voltage to a plurality of memory cells of each memory subblock of the plurality of memory subblocks not associated with the row.

22. The method of claim 18, wherein providing, during a read operation, the first control signal on a first select gate source control line to enable select gate source switches of a first plurality of memory subblocks of a block comprises:

providing the first control signal using a control unit, the control unit located in the block.

23. The method of claim 18, wherein the first plurality of memory subblocks includes a first number of memory subblocks and the second plurality of memory subblocks includes a second number of memory subblocks greater than the first number of memory subblocks.

24. A method, comprising:

selectively providing a respective control signal on each select gate source control line of a plurality of select gate source control lines to enable select gate source switches of a plurality of memory subblocks of a block during a read operation, each select gate source control line of the plurality of select gate source control lines parallel to at least one memory access line of the block and each select gate source control line of the plurality of select gate source control lines associated with a respective plurality of memory subblocks of the plurality of memory subblocks of the block; and

selectively providing a respective control signal on each select gate drain control line of a plurality of select gate drain control lines to enable select gate drain switches of a respective memory subblock of the plurality of memory subblocks of the block during the read operation, each select gate drain control line of the plurality of select gate drain control lines parallel to the at least one memory access line of the block and each select gate drain control line of the plurality of select gate drain control lines associated with a respective memory subblock of the respective memory subblocks associated with a select gate source control line of the plurality of select gate source control lines.

25. The method of claim 24, wherein selectively providing a respective control signal on each select gate source control line of a plurality of select gate source control lines to enable select gate source switches of a plurality of memory subblocks of a block during a read operation comprises:

providing the respective control signal on at least one select gate source control line of the plurality of select gate source control lines to disable select gate source switches of memory subblocks of the plurality of memory subblocks associated with the at least one select gate source control line.

26. The method of claim 25, wherein providing the respective control signal on at least one select gate source control line of the plurality of select gate source control lines to disable select gate source switches of memory subblocks of the plurality of memory subblocks associated with the at least one select gate source control line causes coupling of each capacitive load of a plurality of capacitive loads in series with a junction capacitance.

27. The method of claim 24, wherein

each select gate drain control lines of the plurality of select gate drain control lines parallel to the at least one memory access line of the block.